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Feasible Power Loss Analysis and Estimation of Auxiliary Resonant DC Link Assisted Soft-Switching Inverter with New Zero Voltage Vector Generation Method

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ABSTRACT

The purpose of this paper is to improve power conversion efficiency of three-phase soft-switching voltage-source inverter with an auxiliary resonant dc link (ARDCL) snubber circuit. Firstly, the operating principle of ARDCL snubber circuit is described. Secondly, this paper proposes an effective generation method of zero voltage vector for three-phase voltage-source soft-switching inverter in which power losses in the ARDCL snubber circuit can be reduced. In particular, zero voltage holding interval in the inverter DC busline can be controlled due to the new generation scheme of zero voltage vector. Thirdly, a simulator for power loss analysis, which includes switching and conduction loss characteristics based on actual system, is developed. The validity of developed simulator is proved with experimental results. Finally, power efficiency of three-phase inverter is estimated according to high carrier frequency by using the simulator.

Keywords: Soft-Switching Inverter, Auxiliary Resonant DC Link, Zero Voltage Hold New Zero Voltage Vector Generation Method, Power Loss Estimation

1. Introduction

In recent years, soft-switching power conversion circuits and system technologies have attracted special interest as next generation power converters, which can achieve efficiency improvement in high-frequency switching and lower electromagnetic noises[1-4].

In general, soft-switching power conversion circuit topologies can be roughly classified into three categories; resonant DC link snubber, resonant AC link snubber and auxiliary resonant commutated snubber. Of these, resonant DC Link (RDCL) snubber topology can be applied to small and medium scale power systems due to its simple circuit operation and few circuit components. A novel prototype version of active RDCL snubber circuit has been proposed and a soft-switching inverter with this RDCL snubber circuit has been discussed previously[5]. However, in those conventional topologies, conduction power loss within RDCL snubber circuit leads to decreasing of total power conversion efficiency.

In this paper, in order to improve the power loss within the Auxiliary Resonant DC Link (ARDCL) snubber circuit, an effective new generation method of zero voltage vector is proposed. This new generation method decreases the operating times of ARDCL snubber circuit by controlling the zero voltage interval of dc busline. As a consequence, power loss within ARDCL snubber circuit is decreased

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and total power efficiency of three-phase inverter is increased.

The effectiveness of the new zero voltage vector generation method is proved from theoretical and experimental point of view. Theoretical analysis is performed with a simulator, which contains actual device data. Measured power efficiency of actual system is compared with theoretical power efficiency calculated by the simulator. Power loss and power efficiency estimations are also performed for three-phase soft-switching inverter in high carrier frequency range.

2. Auxiliary Resonant DC Link Circuit

2.1 Circuit Description

Figure 1 illustrates a new prototype version of auxiliary resonant DC link (ARDCL) snubber circuit for three-phase soft-switching voltage-source inverter[5]. The circuit topology shown in Fig. 1 consists of a resonant inductor L_r, two resonant capacitors; main resonant snubber capacitor C_{r1} and energy storage capacitor C_{r2}, three active switching power devices; S_{a1} as a voltage clamped-active switch, S_{a2} for charging and discharging the energy stored in the resonant capacitor C_{r1}, S_{a3} for charging and discharging as well as holding the energy charged in the C_{r2}, in addition, the equivalent switching device corresponding to the inverter bridge arm switching device S_{INV}/D_{INV}, and load current DC source I_O. DC supply voltage is kept to Vs. Resonant initial current is designed to be suitable for the load current. In practice, the enclosed area with a dotted line is incorporated into a conventional three-phase hard-switching voltage source PWM inverter.

2.2 Operation Theory

Figure 2 indicates the equivalent operating circuit for each mode. The proposed ARDCL snubber circuit operation for different mode is described below. Operating waveforms and gate pulse sequences. Every switching device is treated as an ideal device herein.

►**MODE 0** ($t_0<t<t_1$): Initial value of each circuit component is specified so as to be $v_{Cr1}=V_S$, $v_{Cr2}=0$, $i_{Lr}=0$. Load current flows through S_{a1} or D_{a1} in this mode. Each circuit component keeps the initial value,

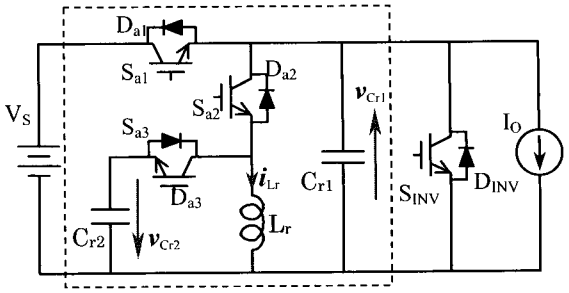


Fig. 1. Auxiliary resonant DC link snubber circuit.

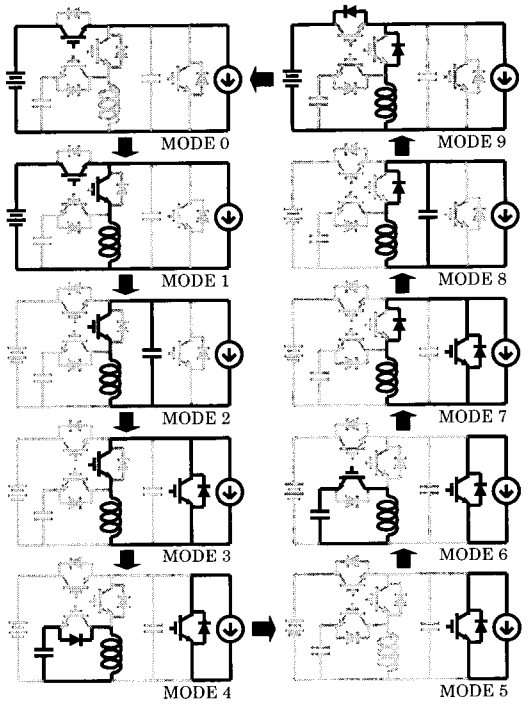


Fig. 2. Equivalent circuit of ARDCL snubber circuit.

and the operation of ARDCL snubber does not start at this point.

$$i_{Lr}=0,\quad v_{Cr1}=V_S,\quad v_{Cr2}=0$$

►**MODE 1** ($t_1<t<t_2$): The operation of ARDCL snubber starts by turning on S_{a2} under ZCS condition in order to change the switching state of the inverter. As the resonant inductor current i_{Lr} increases linearly with initial resonant current value I_i, S_{a1} is turned off under ZVS condition.

$$i_{Lr}=\frac{V_S}{Z_1}\sin\omega_1(t-t_1),\quad v_{Cr1}=V_S,\quad v_{Cr2}=0$$

where, $\omega_1 = 1/\sqrt{L_r C_{r1}}$, $z_1 = \sqrt{L_r/C_{r1}}$

►**MODE 2** ($t_2<t<t_3$): By turning off S_{a1}, the first resonant operation due to L_r and C_{r1} starts and DC busline voltage v_{Cr1} decreases to zero and i_{Lr} increases to I_p.

$$i_{Lr} = \frac{V_S}{Z_1}\sin\omega_1(t-t_2) + (I_i + I_o)\cos\omega_1(t-t_2) - I_o,$$

$$v_{Cr1} = V_S\cos\omega_1(t-t_2) - z_1(I_i + I_o)\sin\omega_1(t-t_2),$$

$$v_{Cr2} = 0$$

where, I_i: Initial resonant current, I_o: DC busline current.

►**MODE 3** ($t_3<t<t_4$): In this mode, all the main switches in three phase soft-switching inverter are turned on, to make commutation current flow within the three-phase full bridge.

$$i_{Lr} = I_p, \quad v_{Cr1} = 0, \quad v_{Cr2} = 0$$

where, I_p: Maximum value of resonant inductor current

►**MODE 4** ($t_4<t<t_5$): The second resonant operation due to L_r and C_{r2} starts turning off S_{a2} under ZVS, auxiliary resonant capacitor voltage v_{Cr2} increases to V_p and i_{Lr} decreases to zero.

$$i_{Lr} = I_p\cos\omega_2(t-t_4), \quad v_{Cr1} = 0,$$

$$v_{Cr2} = I_p z_2\sin\omega_2(t-t_4),$$

where, $\omega_2 = 1/\sqrt{L_r C_{r2}}$, $z_2 = \sqrt{L_r/C_{r2}}$

►**MODE 5** ($t_5<t<t_6$): Each circuit component keeps its value at the end of mode 4. By controlling the interval of this mode, new switching pattern becomes possible. In the new switching pattern, this mode works as zero voltage vector.

$$i_{Lr} = 0, \quad v_{Cr1} = 0, \quad v_{Cr2} = V_p$$

where, V_p: Maximum voltage of second resonant capacitor.

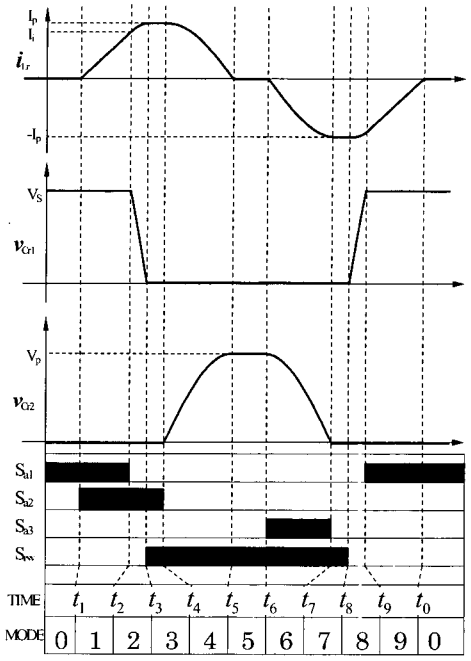


Fig. 3. Operating waveforms and gate pulse sequences

►**MODE 6** ($t_6<t<t_7$): The second resonant operation restarts turning on S_{a3} under ZVS and ZCS, v_{Cr2} decreases to zero and i_{Lr} decreases to $-I_p$ (minimum value of i_{Lr2}).

$$i_{Lr} = I_p\cos\omega_2(t-t_6), \quad v_{Cr1} = 0,$$

$$v_{Cr2} = I_p z_2\sin\omega_2(t-t_6)$$

►**MODE 7** ($t_7<t<t_8$): At the moment v_{Cr2} equals zero, S_{a3} is turned off under ZVS. It means that the switching pattern of the inverter changes to the next one. Then, S_{INV} is turned off under ZVS.

$$i_{Lr} = -I_p, \quad v_{Cr1} = 0, \quad v_{Cr2} = 0$$

►**MODE 8** ($t_8<t<t_9$): By turning off S_{a3}, the first resonant operation restarts and v_{Cr1} increases to Vs.

$$i_{Lr} = (I_i - I_o)\cos\omega_1(t-t_8) - I_o,$$

$$v_{Cr1} = z_1(I_i - I_o)\sin\omega_1(t-t_8), \quad v_{Cr2} = 0$$

►**MODE 9** ($t_9<t<t_{10}$): S_{a1} is turned on under ZVS and ZCS during i_{Lr} through D_{a1} and the operation of ARDCL snubber circuit completes at this point.

$$i_{Lr} = \frac{V_S}{z_1}\omega_1(t-t_9), \quad v_{Cr1} = 0, \quad v_{Cr2} = 0$$

From these operations, it is proved that soft-switching commutation is achieved during all switching operations in ARDCL snubber.

3. Three-Phase Soft-Switching Voltage-Source Inverter

3.1 System Description

Three-phase soft-switching voltage-source inverter using ARDCL snubber circuit is shown in Fig. 4. Table 1 indicates its design specifications and circuit parameters. This inverter system includes DC voltage source, ARDCL snubber circuit, three-phase inverter, low-pass filter, three-phase resistance load and its control system.

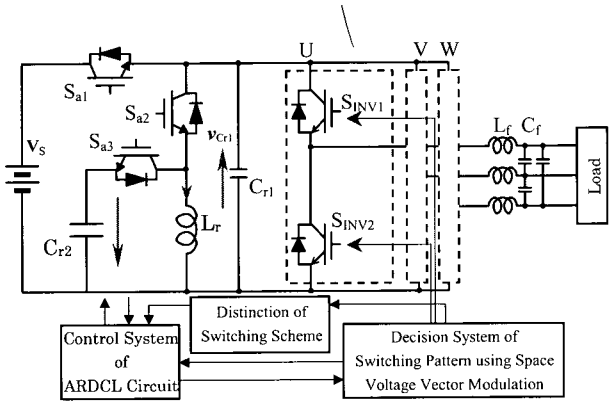


Fig. 4. Proposed three-phase soft-switching inverter.

Table 1. Design specifications of three-phase inverter.

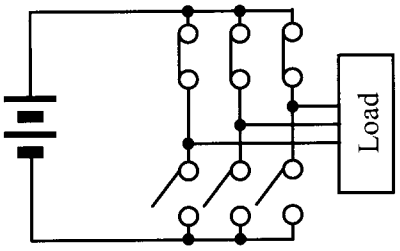
DC source voltage	V_S	200.0	[V]
Output power	P_{out}	0.95→2.2	[kW]
Output current (rms)	I_{OUT}	10.0	[A]
Carrier frequency	f_r	8.0	[kHz]
Output frequency	f_O	60.0	[Hz]
First resonant capacitor	C_{r1}	75.0	[nF]
Second resonant capacitor	C_{r2}	120.0	[nF]
Resonant inductor	L_r	10.0	[μH]
Resistive component of L_r	R_{Lr}	0.2	[Ω]
Resistive load (Y)	R_L	3.5→7.14	[Ω]
Filter inductance	L_f	580.0	[μH]
Resistive component of L_f	R_{Lf}	0.05	[Ω]
Filter capacitance	C_f	40.0	[μF]

3.2 New generation method of zero voltage vector

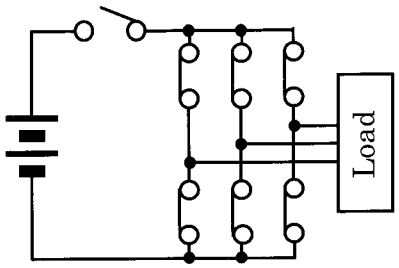
Figure 5 illustrates the equivalent circuit of three-phase soft-switching inverter. Switching pattern of Fig. 5(a) is expressed as V_Z in voltage vector, and this equivalent circuit performs the operation of zero voltage vector. In Fig. 5 (b), the zero voltage vector is defined as V_Z', and ARDCL snubber circuit keeps mode 5 and all switches are turned on. In both equivalent circuits, Fig. 5 (a) and (b), load current circulates through three-phase bridge arm. And total system provides the same effect to the load, i.e., Fig. 5 (b) can work as Fig. 5 (a). As a result, new zero voltage vector generation method becomes possible as shown in Fig. 6 (b). Fig. 6 shows the switching voltage vector during one carrier period of space voltage vector modulation.

where, T_S: One carrier period time, $T_S = 1/f_r = 125.0$ μsec.
T_O: ARDCL operating interval,
$T_O = \pi/\omega_1 + \pi/\omega_2 + (t_4 - t_3) + (t_8 - t_7) = 7.25$ μsec.

Fig. 6 (a) represents the conventional method, and Fig. 6 (b) represents the proposed method. In Fig. 6 (a), ARDCL circuit operates at every starting point of switching voltage vector.

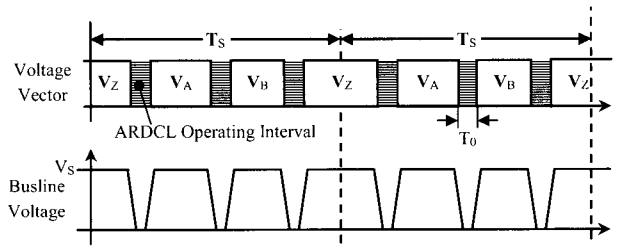


(a) Zero Voltage Vector

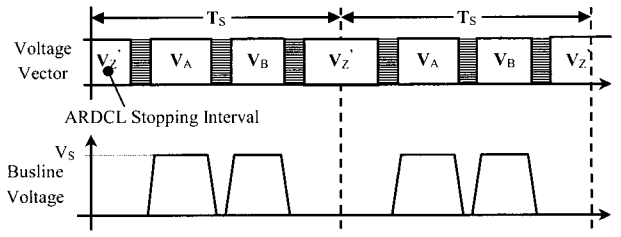


(b) ARDCL Circuit MODE5

Fig. 5. Equivalent circuit of voltage-source three-phase inverter.



(a) Conventional Method



(b) Proposed Method

Fig. 6. Switching voltage vector pattern during one time period.

Then, ARDCL needs to operate three times during T_S. On the other hand, in Fig.6 (b), ARDCL needs to operate two times during T_S, since ARDCL circuit operates when switching voltage vector changes from V_B to V_A and V_A to V_B.

Its operating principle is explained as follows.

STEP 1 (Mode 0-1) ARDCL circuit starts at the starting point of V_B.

STEP 2 (Mode 1-5) When the state of ARDCL snubber circuit changes to mode 5, ARDCL circuit stops its operation.

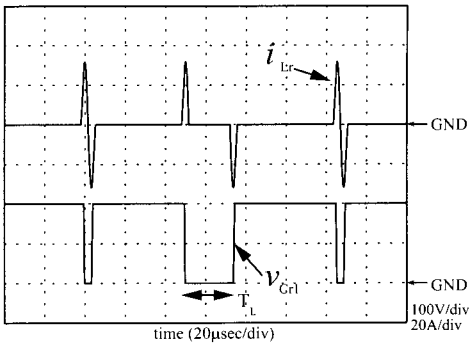
STEP 3 (Mode 5) ARDCL circuit keeps circuit state at mode 5.

STEP 4 (Mode 5-0) ARDCL circuit restarts at the starting point of V_A. The switching pattern changes to V_A.

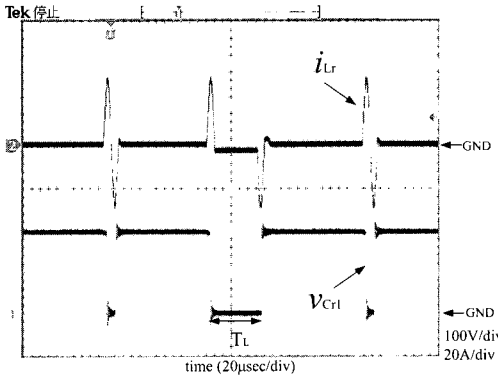
Therefore, ARDCL snubber circuit operates during $V_B \rightarrow V_Z \rightarrow V_A$. As a result, ARDCL snubber circuit needs to operate only two times during T_S.

4. Operation Waveforms

Practical simulation analysis and experiment are performed for three-phase soft-switching inverter using ARDCL circuit.



(a) Simulation results



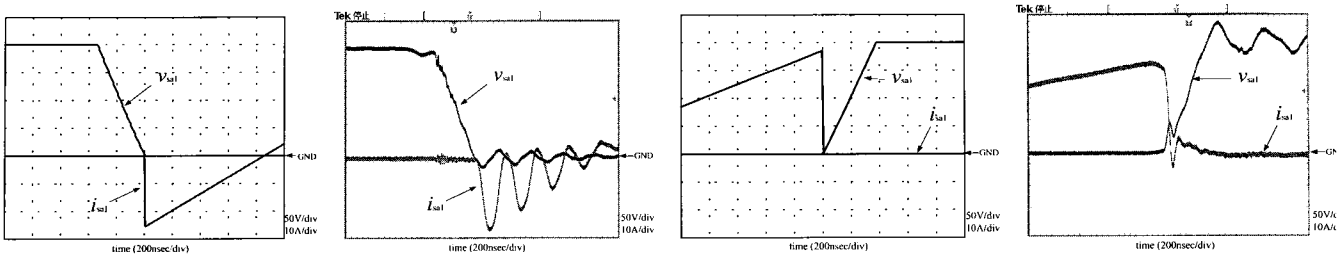
(b) Experimental results

Fig. 7. Resonant inductor current and dc busline voltage waveform.

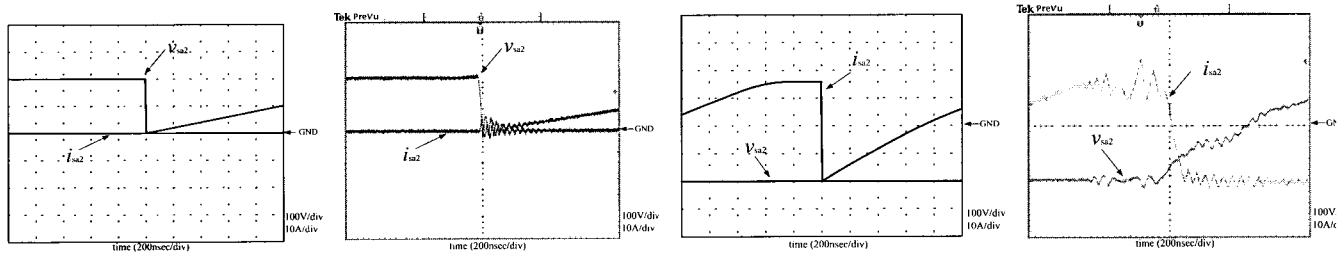
The three-phase inverter operates under space voltage vector modulation method in open loop control. Carrier frequency is 8 kHz and output line current is kept at 10A rms. Resistance load value and modulation depth is adjusted to arrange the output power and the rating of IGBT used in experimental setup is 600V-75A; CM75DU-12F.

Main resonant capacitor voltage which is the dc busline voltage waveform and resonant inductor current waveforms are illustrated in Fig. 7 (a) and (b). In Fig. 7 (a) and (b), the operation of ARDCL snubber circuit is stopped during T_L.

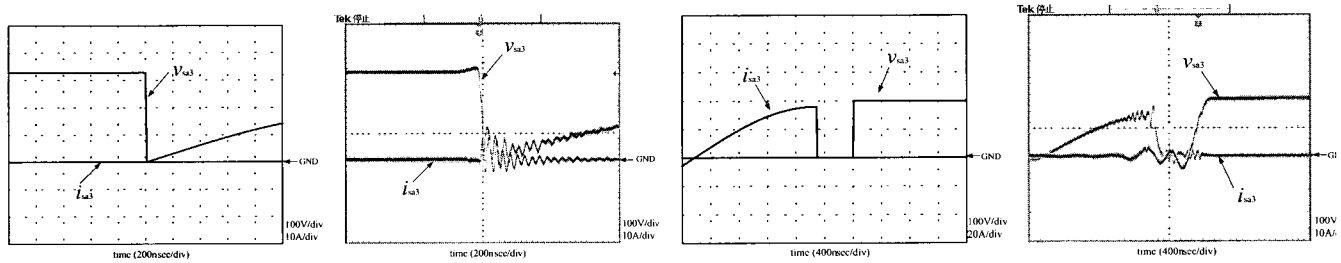
Fig. 8 represents the switching waveform of switch S_{a1}, S_{a2}, S_{a3} and S_{INV}. From these waveforms, it is clear that ZVS/ZCS soft-switching is achieved at S_{a1} turning ON / S_{INV} turning ON, ZVS soft-switching is achieved at S_{a1} turning OFF / S_{a2} turning OFF / S_{a3} turning OFF / S_{INV} turning OFF and ZCS soft-switching is achieved at S_{a2} turning ON / S_{a3} turning ON.



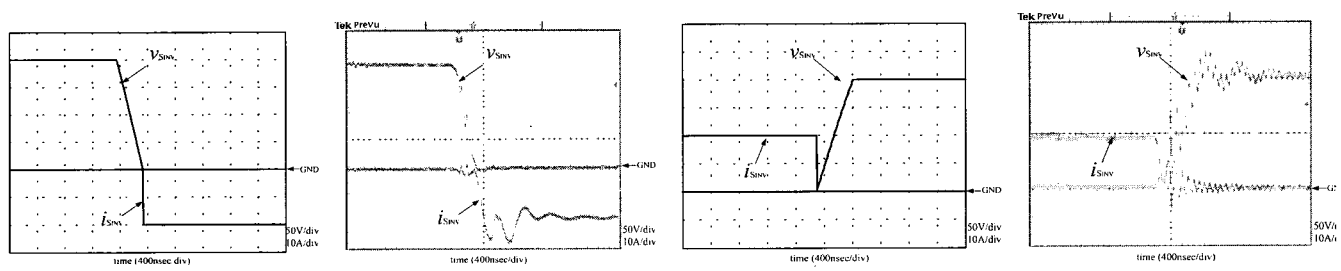
(a) S_{a1} turning on-simulation (b) S_{a1} turning on-experiment (c) S_{a1} turning off-simulation (d) S_{a1} turning off-experiment



(e) S_{a2} turning on-simulation (f) S_{a2} turning on-experiment (g) S_{a2} turning off-simulation (h) S_{a2} turning off-experiment



(i) S_{a3} turning on-simulation (j) S_{a3} turning on-experiment (k) S_{a3} turning off-simulation (l) S_{a3} turning off-experiment



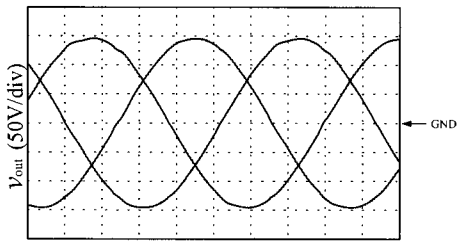
(m) S_{INV} turning on-simulation (n) S_{INV} turning on-experiment (o) S_{INV} turning off-simulation (p) S_{INV} turning off-experiment

Fig. 8. Switching waveforms ARDCL.

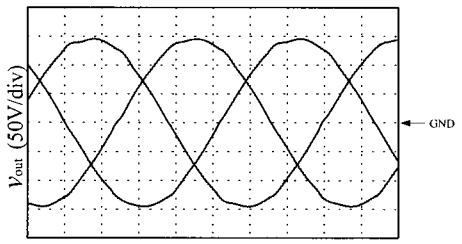
Fig. 9 (a), (b), (c) and (d) depict the line-to-line load voltage waveforms for each zero voltage vector generation scheme. In Fig. 9 (c) and (d), both output voltage waveforms have high quality. From these waveforms, it is proved that the dc busline zero voltage interval works as zero voltage vector and the simulation analysis is effective and reliable.

5. Estimation of Power Efficiency and Power Loss

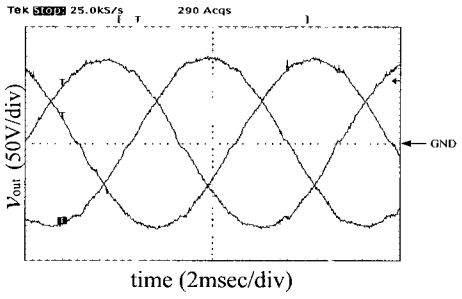
Power loss analysis of three-phase soft-switching voltage-source inverter using ARDCL snubber circuit is performed with a simulator, which considers the switching and conduction loss characteristics based on actual system.



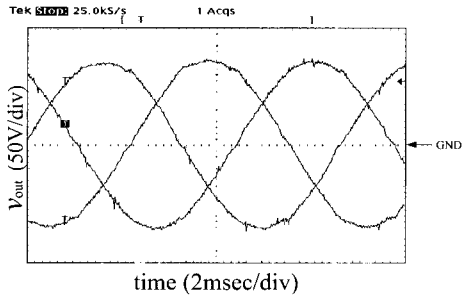
(a) Conventional method-Simulation result



(b) Proposed method-Simulation result



(c) Conventional method-experimental result



(d) Proposed method-experimental result

Fig. 9. Output line-to-line voltage waveform of soft switching three-phase inverter.

An original simulator using C programming language is developed for power loss analysis.

In this simulator, differential equation for each equivalent circuit is utilized to calculate current and voltage. In the case when voltage and current of voltage source three phase soft switching inverter are calculated, all switching devices are treated as ideal switch and each circuit component does not have resistive component.

On the other hand, when instant power loss is calculated at every simulation time interval, switching device characteristic is used. Negligible switching time error S_T is 1% herein. The maximum value of carrier frequency F_{rmax} is obtained by the equation followed.

$$S_T(\%) = (S_{on}+S_{off})/2 \times F_{rmax} \times 100 = 1.0\ (\%)$$
$$F_{rmax} = 16\ \text{kHz}$$

where, S_{on} is turn on time: S_{on}=750 nsec,
S_{off} is turn off time: S_{off}=550 nsec

5.1 Switching Loss Characteristic

This simulator deals with only ZVS turn off loss by tail current, since it is clear that there is no switching loss in the switching operation based on ZCS and ZVS/ZCS as shown in Fig. 8. That is, simulator treats turn off switching loss of Sa1, S_{a2} and S_{INV}.

Switching losses of S_{a1}, S_{a2} and S_{INV} are measured according to the dc load current I_O and collector current, since the operation of ARDCL snubber circuit depends on I_O. Fig. 10 demonstrates the switching loss characteristics with one switching operation of S_{a1}, S_{a2} and S_{INV} at the ZVS turning off according to I_O. Equation (1)~(3) is obtained by using the least square method for the data presented in Fig. 10. In the simulator, consumed power in one switching operation is stored in one second.

In the simulator, switching loss in one switching operation obtained from equations (1)~(3) is accumulated during one second as total switching loss by its switching device.

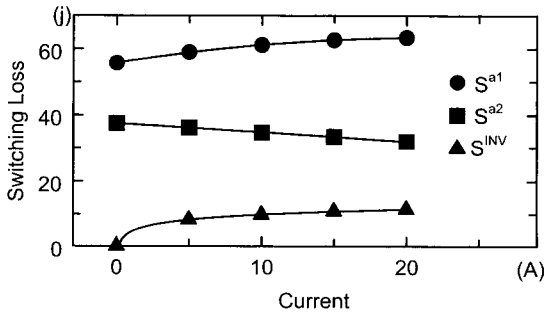


Fig. 10. Switching loss characteristic.

$$P_{Sa1\text{-}off} = \sum_{n=0}^{2} a_n \times I_o^n \quad (1)$$

$$P_{Sa2\text{-}off} = \sum_{n=0}^{2} b_n \times I_o^n \quad (2)$$

$$P_{SINV\text{-}off} = c_0 + c_1 \, ln \, I_c \quad (3)$$

where, $a_0 = 55.71$, $a_1 = 0.71$, $a_2 = -0.016$, $b_0 = 37.52$, $b_1 = -0.28$, $b_2 = -2.85\times1.0^{-4}$, $c_0 = 4.51$, $c_1 = 2.33$

5.2 Conduction Loss Characteristic

In this simulator, the voltage drop of IGBTs, diodes, resistive components of resonant inductor R_{Lr} and filter inductor R_{Lf} are considered responsible for conduction loss. At first, actual voltage drop of IGBT and diode are measured according to collector current I_C and anode current I_d

Fig. 11 shows the voltage drop characteristics of IGBT and diode.

Equations (4) and (5) are obtained by using the least square method for measured data shown in Fig. 11.

$$v_{CE} = \exp(a + b \ln I_C) \quad (4)$$

$$v_D = \exp(c + d \ln I_d) \quad (5)$$

where, $a = -0.18$, $b = 0.12$, $c = -0.36$, $d = -0.22$

In the simulator, instantaneous conduction losses by IGBT and diode are calculated from equations (4), (5) at every simulation time interval. And total conduction loss is obtained by accumulating the instantaneous conduction loss during one second.

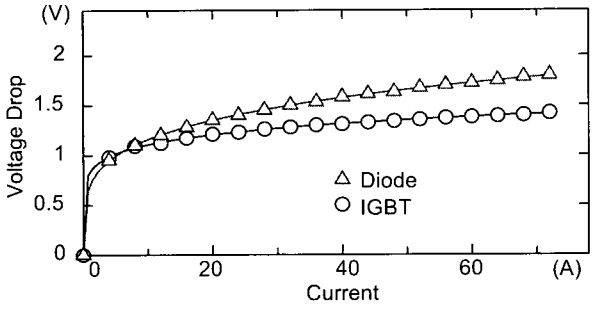


Fig. 11. Voltage drop characteristic of IGBT and Diode.

Regarding conduction loss by resonant inductor L_r and filter inductor L_f, value of R_{Lr} and R_{Lf} is measured in advance. Here, R_{Lr} is 0.2Ω, and R_{Lf} is 0.05Ω.

In the simulator, instantaneous power loss is calculated in relation to the current flowing through each reactor at every simulation time interval. Total conduction loss is obtained by total sum of conduction loss in every IGBT, every Diode, R_{Lr} and R_{Lf}.

5.3 Considerations on Power Efficiency and Power Loss Analysis

Fig. 12 shows the power efficiency of the three-phase soft-switching inverter with conventional soft-switching method and proposed soft-switching method. In all power range, power efficiency of proposed soft-switching method is higher than that of the conventional soft-switching method. Fig. 13 shows the amount of consumed power of three-phase soft-switching inverter during one second. By using new zero voltage vector generation method, dissipated power in ARDCL snubber circuit is decreased.

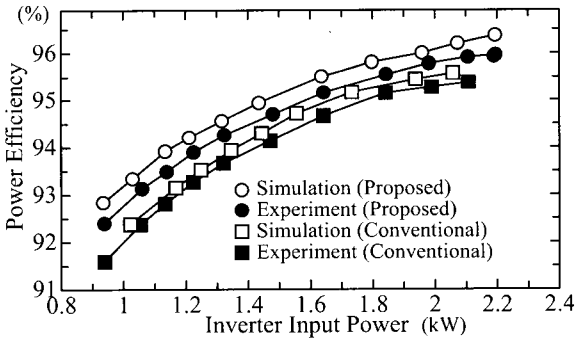


Fig. 12. Power efficiency of three-phase inverter.

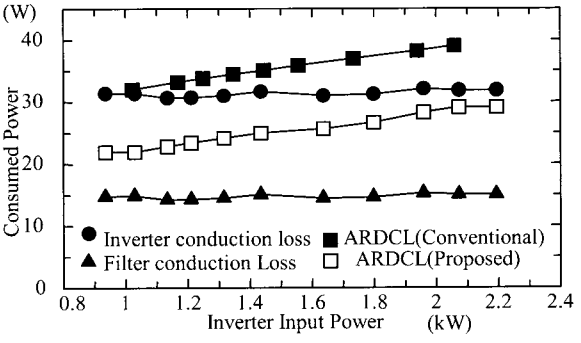


Fig. 13. Element-wise consumed power in three-phase inverter.

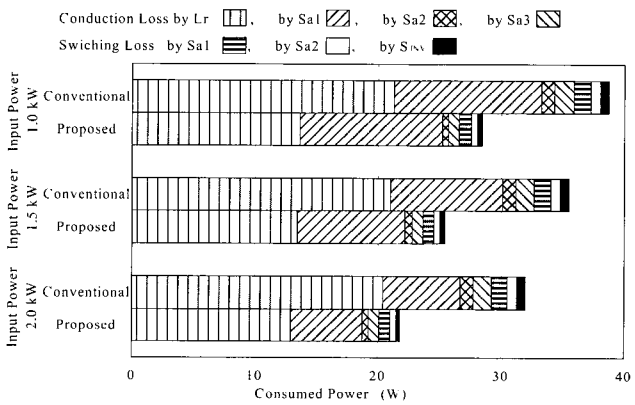


Fig. 14. Consumed power by each component of ARDCL.

Fig. 14 shows the consumed power in each component of snubber circuit for different power. In Fig. 14, consumed conduction power in S_{a1} and D_{a1} occupies most part of total power loss since S_{a1} always turns on during steady state of ARDCL snubber circuit. It means that the active switching power device that has low saturation voltage like trench gate IGBT is suitable for ARDCL circuit topology.

5.4 High Carrier Frequency Range

Power efficiency of three-phase soft-switching inverter at high carrier frequency range is estimated by the simulator. Fig. 15 shows the maximum modulation depth M_{max} for the three-phase inverter in each switching case for different carrier frequency and this modulation depth can make suitable output voltage. M_{max} is obtained from the following equation.

$$M_{max} = 1-(A_{time} \times T_0)/T_S \quad (6)$$

where, A_{time} is operating times of ARDCL during T_S.

$A_{time} = 3$ (for conventional method),

$A_{time} = 2$ (for proposed method)

Since DC busline zero voltage interval corresponds to zero voltage vector output interval as mentioned above, M_{max} is decreased in the soft-switching inverter. However, M_{max} can be improved by using the new zero voltage vector generation method. Sum of T_O in T_S decreases, since operating time of ARDCL circuit is decreased. It means that M_{max} can be increased when the new zero voltage vector generation method is applied.

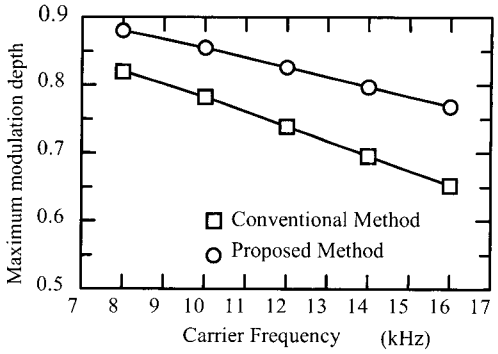


Fig. 15. Maximum modulation depth of inverter.

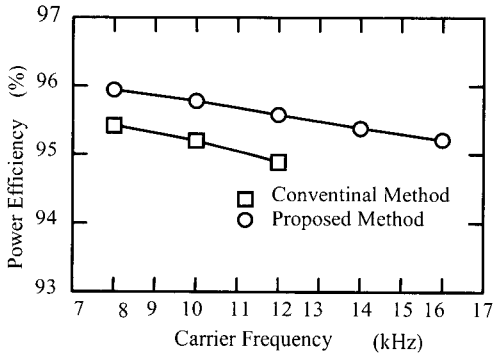


Fig. 16. Power efficiency of three-phase inverter in high frequency range.

Fig. 16 represents the power efficiency by simulation analysis for high switching frequency range. From Fig. 16, soft-switching operation is possible under 12kHz in the conventional method. On the other hand, in the proposed method by using new zero voltage vector generation method, soft-switching operation is achieved until 16kHz due to the improving of M_{max}. Besides, it is clear that power efficiency at 16kHz with proposed method has the same value at 10kHz without the proposed method. In other words, the switching frequency can be increased when the proposed zero voltage vector generation method is applied, keeping power conversion efficiency high.

From these results, the effectiveness of the new zero voltage vector generation method is proved from theoretical and experimental point of view.

6. Conclusions

In this paper, new zero voltage vector generation method, which has high power efficiency and high M_{max},

was introduced and performed for three-phase soft-switching voltage source inverter. Besides, the introduction of loss analysis on each power device in the simulator was attempted in order to evaluate the total efficiency of the three-phase voltage-source soft-switching inverter. In this proposed simulator, actual characteristics of each power device were considered. As a result, it was possible to evaluate the efficiency of the soft-switching operation accurately. Finally, the effectiveness of the proposed soft-switching method that includes zero voltage holding operation was proved on the basis of simulation and experimental results.

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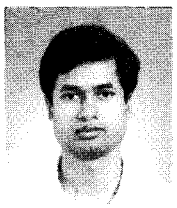

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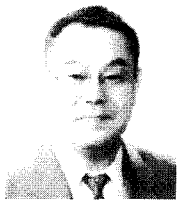

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