An Etch-Stop Technique Using Cr_2O_3 Thin Film and Its Application to Silica PLC Platform Fabrication

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ABSTRACT¾ Using Cr_2O_3 thin film, we developed a novel etch-stop technique for the protection of silicon surface morphology during deep ion coupled plasma etching of silica layers. With this technique we were able to etch a silica trench with a depth of over 20 μm without any damage to the exposed silicon terrace surface. This technique should be well applicable to fabricating silica planar lighwave circuit platforms for opto-electronic hybrid integration.

I. INTRODUCTION

Opto-electronic hybrid integration using planar lightwave circuit (PLC) platforms is a promising technology for producing high-performance optical components for optical network systems. A good PLC platform must be able to perform three functions: (1) a low-loss optical waveguide function, (2) an optical bench function to incorporate an optical device on the same substrate and prevent axis deviation, and (3) a high-frequency electrical wiring function required to drive the optical device [1]. Silica PLC platforms on silicon wafers are a good solution to meeting all the required conditions. To fabricate silica PLC platforms, deep etching of the silica layers is indispensable to forming a trench and exposing the silicon terrace on which the optical devices will be mounted. Generally reactive ion etching or ion coupled plasma (ICP) etching processes are used to etch out the thick silica layers on the terrace. In such plasma etching processes, a specific mixture of etching gases is used under some limited plasma power conditions to enhance the silica to silicon etch selectivity and minimize the damage on the exposed silicon terrace surface. However, in such conditions, the etch rate is very low and damage to the terrace surface is unavoidable.

In this letter, we report a novel etch-stop technique based on the use of Cr_2O_3 thin film to stop etching on the silicon surface during the high speed ICP etching of the silica layer. By using this technique we were able to etch silica trenches with a depth of over 20 μm with a high etch rate of about 3500 Å/min without any damage to the exposed silicon terrace surface. This technique should be well applicable to fabricating the silica PLC platforms for opto-electronic hybrid integration.

II. THE ETCH-STOP TECHNIQUE

Figure 1 shows the schematic illustration of the silica PLC platform. This platform is fabricated by a sequence of processes as follows: (1) anisotropic etching of a silicon wafer to form terraces, (2) formation of a low loss silica optical waveguide by the well known flame hydrolysis deposition (FHD) process, (3) dry etching of the thick silica layers to form a trench region and expose the terraces on which the opto-electronic devices can be mounted, (4) metal layer lift-off to

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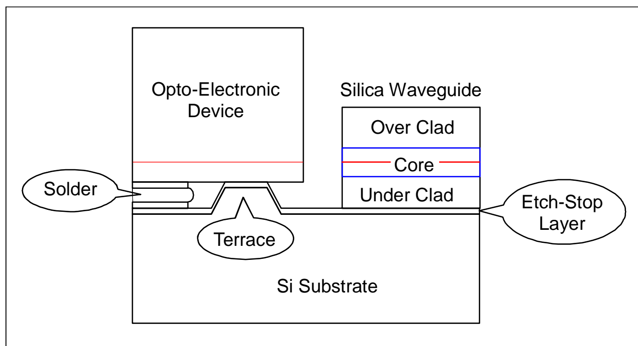

Fig. 1. Schematic illustration of the silica PLC platform structure.

Table 1. The silica ICP etching conditions.

Process items	Condition
Etching GAS (sccm)	CF_4 , 40
ICP Power (W)	800
DC Bias (V)	30
Process Pressure (mTorr)	10
Run Time (min)	60

form electrical wirings, solder pads, and wire bonding pads, (5) solder lift-off and reflow, and (6) flip-chip bonding of opto-electronic devices and wire bondings. The surface of the silicon terrace should be formed to be an exact height in reference to the silica waveguide core so that the vertical alignment of the waveguide cores of the silica PLC and opto-electronic devices can easily be achieved by contacting the surface of the device against the silicon terrace [2]. It is thus indispensable that the terrace surface must be well protected during the silica etching process.

Several attempts to put a thin film etch-stop layer on a silicon surface have been tried with materials such as alumina, alkaline slilcate glasses, titania, metal Cr, and Cr_2O_3. However, the results have been far from satisfactory because those films caused problems in the subsequent FHD process. Especially degradation of the silica waveguide layers by crystallization and/or micro-cracks in the etch-stop films were major problems. We found that only Cr_2O_3 thin film is compatible with the subsequent FHD process and that it has good etch-stop properties as well. The Cr_2O_3 etch-stop layer was prepared as follows. First, Cr metal thin film with a thickness of about 1500 Å was coated on the terrace-formed and passivated silicon wafer by RF sputtering. Then the Cr metal was oxidized in an electric furnace at 1000 °C for 1hr in air atmosphere. On the Cr_2O_3 film, the silica optical waveguide was formed by the FHD and the silica trench etching was carried out by ICP etching under the conditions listed in Table 1. The residual Cr_2O_3 etch-stop layer was not removable after the slica layers were etched, and therefore its thickness of about 2000 Å was considered in calculating the final height of the terraces.

Figure 2 shows the exposed terrace surface after the silica layers were etched on it. Fig. 2(a) shows the damaged terrace surface when etched without the etch-stop layer. The silicon terrace edge has already been etched while there still remains residual silica layers in the terrace grooves. Fig. 2(b) shows the terrace surface well protected by the Cr_2O_3 etch-stop layer even after the silica layers have been fully etched out. We successfully etched a trench with a depth of over 20 μm through silica layers to the terrace at a high etch rate of about 3500 Å/min and found neither damage on the terrace surface nor any noticeable cracks in the etch-stop layer. Sometimes very fine cracks were found only in the terrace pattern corners, but that would have a negligible effect on the function of the platform. Figure 3 shows the silica PLC platform with LD chips flip-chip bonded on the protected terrace surface. The LD operation was successful and about a –4 dBm laser output power was coupled into the silica waveguide (about a 5 dB coupling loss), proving that the Cr_2O_3 thin film etch-stop technique can be well

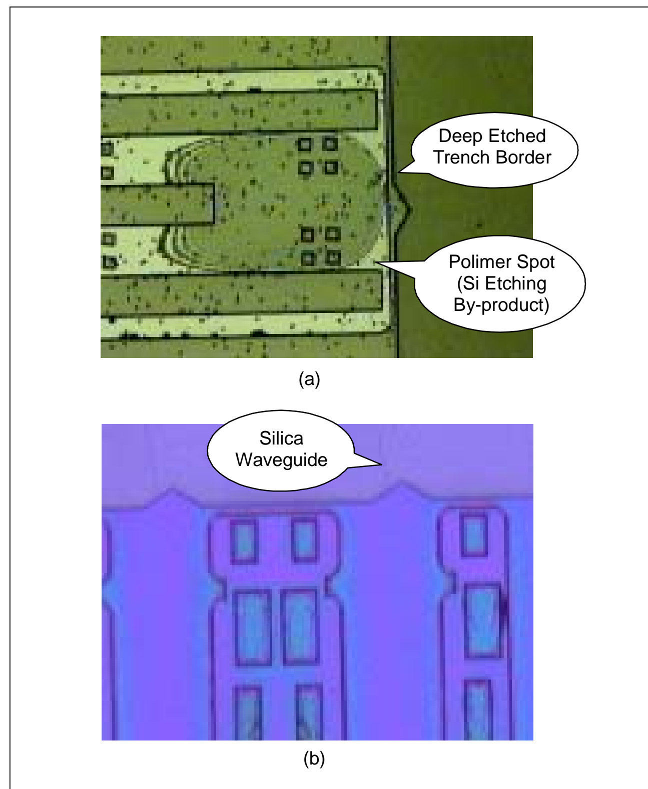

Fig. 2. The ICP etched terrace surfaces (a) without an etch-stop layer, and (b) with the Cr_2O_3 etch-stop layer. The terraces are fully exposed and only a minimal residue of silica is found on the groove floors.

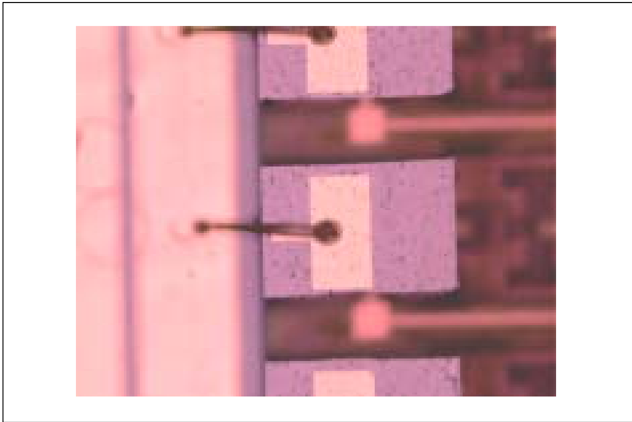

Fig. 3. The silica PLC platform on which LD chips are flip-chip bonded. The LD operation was successful and about a –4 dBm laser output power was coupled into the silica waveguide.

applied to silica PLC platform fabrication.

III. SUMMARY

We reported a novel etch-stop technique based on the use of Cr_2O_3 thin film to stop etching silicon during the high speed ICP etching of silica. We used this technique in fabricating silica PLC platforms and were able to etch a silica trench with a depth of over 20 μm without any damage to the exposed silicon terrace surface. Our study demonstrates that this technique can be well applied to fabricating silica PLC platforms for opto-electronic hybrid integration.

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