Breakdown Voltage Improvement of p-LDMOSFET with an Uneven Racetrack Source for PDP Driver IC Applications

Tae Moon Roh, Dae Woo Lee, Yil Suk Yang, Jin Gun Koo, and Jongdae Kim

ABSTRACT¾ We investigated the electrical characteristics of p-channel double-diffused MOSFETs (p-LDMOSFETs) with an uneven racetrack source (URS) and a conventional racetrack source (CRS) for PDP driver IC applications. The breakdown voltage of the p-LDMOSFET with the URS in off-state was nearly the same as the p-LDMOSFET with the CRS. However, the breakdown voltage of the p-LDMOSFET with the URS in on-state was about 30% higher than that of the p-LDMOSFET with the CRS, while the saturated drain current of the p-LDMOSFET with the URS was only about 4% lower than that of the p-LDMOSFET with the CRS.

I. INTRODUCTION

The breakdown voltage and on-resistance of lateral double-diffused MOSFETs (LDMOSFETs) can be optimized by using REduced SURface Field (RESURF) effects [1]-[7]. An LDMOSFET with a racetrack layout is commonly used in high voltage ICs with interdigitated layouts [3]. Usually, a drain with the racetrack structure of an LDMOSFET is surrounded by the source connected to the bulk for power ICs; this results in many advantages, such as electrically isolating each device and reducing edge effects on the LDMOSFETs. An LDMOSFET with a conventional racetrack source (CRS) structure inevitably has a higher current density near the rounded drain edge, because the rounded source width of the LDMOFET is wider than the rounded drain width of the device; this causes the drain current and the electric flux to be crowded toward the rounded drain edges. These current crowding and electric flux crowding effects near the rounded drain edges may cause localized heating effects as well as localized high current injection effects, resulting in lower breakdown voltage.

We propose a new p-LDMOSFET with an uneven racetrack source (URS) to handle larger current near the rounded drain edges and obtain higher breakdown voltage than conventional racetrack p-LDMOSFETs.

II. DEVICE DESIGN AND FABRICATION

Figures 1 and 2 respectively show top views and cross sections of two p-LDMOSFETs with a CRS and a URS. The p-LDMOSFET with the CRS consists of straight channel regions and rounded channel regions with only gate oxides (A-A'). In the p-LDMOSFET with the CRS, the drain current is crowded near the rounded drain edges because the source width is wider than the drain width; this leads to a reduced breakdown voltage in the device. To overcome the drain current crowding effects near the rounded drain edges, we propose a p-LDMOSFET with a URS, which, compared to the p-LDMOSFET with a CRS, consists of the same structure for the straight channel region and a different structure for the rounded channel region. The rounded channel region of the p-LDMOSFET with the URS is modified by replacing the field oxide (3 times thicker than the gate oxide) regions (B-B') on the drift region extended to the rounded source regions with some part of the gate oxide regions (A-A'); this reduces the effective rounded channel width and decreases the drain

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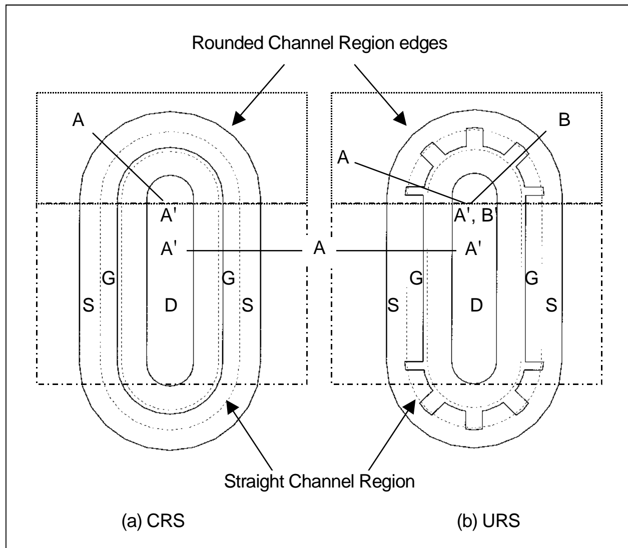

Fig. 1. Layouts of p-LDMOSFETs with different source structures: (a) Conventional racetrack source (CRS), (b) Uneven racetrack source (URS). S, D, and G represent the source, drain, and gate of the p-LDMOSFETs.

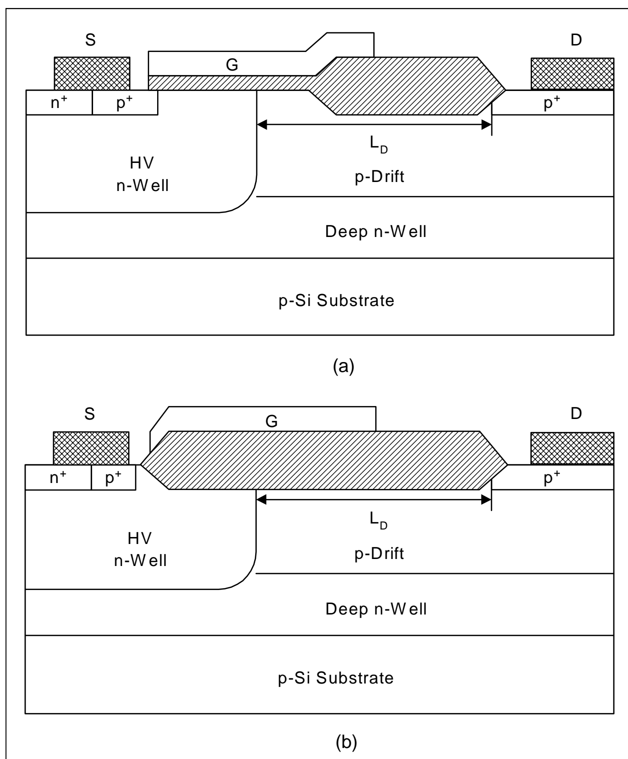

Fig. 2. Cross sections of p-LDMOSFETs of the Fig. 1: (a) A-A' and (b) B-B'.

current density near the drain edges to improve the breakdown voltage.

The p-LDMOSFETs were fabricated as follows [8]: A deep n-well for the p-LDMOSFET was implanted using phosphorus and boron and annealed to make a deep junction with a uniform doping profile on a p-type (100) silicon wafer with a 20 μm thick p-epi silicon layer. A p-drift region for the p-LDMOSFET was implemented using boron (8×10^{12} cm^{-2}). Phosphorus was implanted in the high voltage n-well region for the channel of the p-LDMOSFET and followed by annealing in N_2 ambient at 1150 °C. A field oxide of 6000 Å was grown to electrically isolate each device, and then a gate oxide of 2000 Å for the p-LDMOSFET was grown. A polysilicon of 3800 Å was deposited by low-pressure-chemical-vapor deposition, was doped in $POCl_3$ at 875 °C for 40 min and was defined using conventional photolithograpy and dry etching techniques to form a polysilicon gate. The remaining processes were the same as conventional CMOS processes. The electrical characteristics of the p-LDMOSFETs were measured by an HP4156A precision semiconductor parameter analyzer.

III. RESULTS AND DISCUSSION

Figure 3 shows I-V characteristics of p-LDMOSFETs with a CRS and a URS. The channel length (L_G), drift length (L_D), rounded channel width (W_{rou}), and straight channel width (W_{str}) of the p-LDMOSFET were 2.4 μm, 8.4 μm, 102 μm, and 200 μm, respectively. As the voltage increased, the current of the p-LDMOSFET with the URS increased more slowly than that with the CRS, resulting in higher breakdown voltage (V_{BR}) between the source and the drain and lower saturated drain current. The saturated drain current of the p-LDMOSFEET was measured at $V_{GS}=-100$ V and $V_{DS}=-50$ V.

Generally, the p-LDMOSFET with the URS has the disadvantage of a decreasing drain current due to the reduction of the effective channel width at the rounded channel region (Fig. 3). However, as the straight channel width of the p-

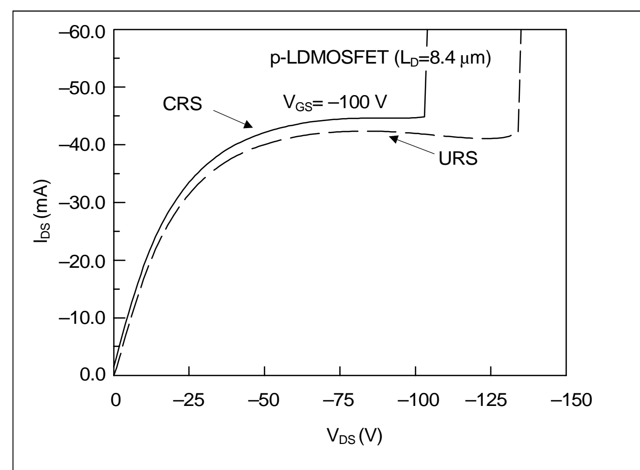

Fig. 3. I-V characteristics of p-LDMOSFETs with a CRS and a URS under gate voltage of –100 V.

LDMOSFET with racetrack structures increases, the current through the straight channel region increases while that through the rounded channel region remains constant. Therefore, if the straight channel width of the p-LDMOSFET with the URS is sufficiently wider than the rounded channel width of the p-LDMOSFET, the current reduction due to the URS of the p-LDMOSFET will be negligible even if the higher breakdown voltage remains.

Figure 4 shows the ratios of the saturated drain current of the p-LDMOSFET with the URS, I_{DS}(URS), to that of the p-LDMOSFET with the CRS, I_{DS}(CRS), as a function of W_{str}. The ratio of the I_{DS}(URS) of the p-LDMOSFET to the I_{DS}(CRS) of the p-LDMOSFET increased from 82% to 96% as the W_{str} of the p-LDMOSFET increased from 0 μm to 200 μm. This figure reveals that the saturated drain current of the p-LDMOSFET with the URS and a W_{str} of 200 μm was 4% lower than that of the p-LDMOSFET with the CRS and the same straight channel width.

Figure 5 shows the V_{BR} characteristics of p-LDMOSFETs with a CRS and a URS at off-state (V_{GS}=0 V) and on-state (V_{GS}= –100 V) as a function of W_{str}. The V_{BR}'s of the p-LDMOSFETs with the CRS and the URS at off-state and on-state did not decrease as their W_{str}'s increased from 0 μm to 200 μm. The V_{BR} of the p-LDMOSFET with the URS in off-state was nearly the same as the p-LDMOSFET with the CRS and was not influenced by the W_{str}. However, the V_{BR} of the p-LDMOSFET with the URS in on-state increased to about 30%, which is much higher than that with the CRS. In Figs. 4 and 5, compared to the p-LDMSOFET with the CRS, the V_{BR} of the proposed p-LDMOSFET with URS can increase greatly without a serious reduction in the saturated drain current of the p-LDMOSFET with the URS.

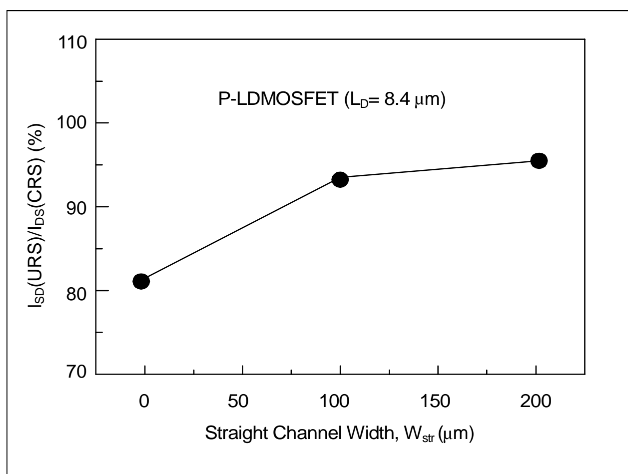

Fig. 4. The ratios of the saturated drain current of the p-LDMOSFET with the URS to that of the p-LDMOSFET with the CRS as a function of the straight channel width.

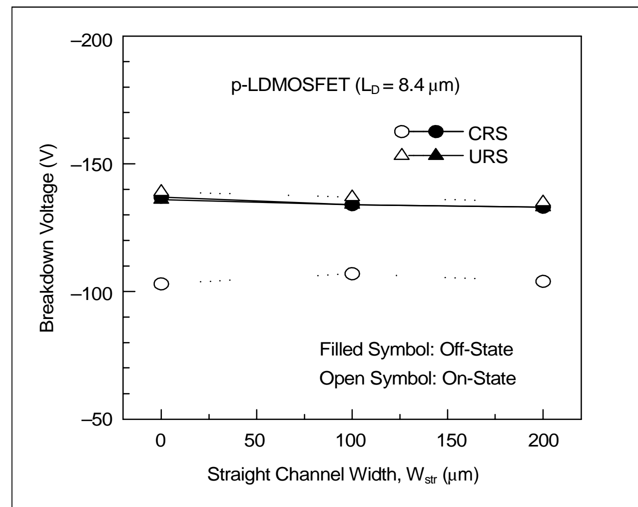

Fig. 5. Breakdown characteristics of p-LDMOSFETs with the CRS and the URS in at off-state and on-state as a function of the straight channel width.

IV. CONCLUSION

We proposed a new p-LDMOSFET with a URS and compared it to a conventional p-LDMOSFET with a CRS in order to observe the breakdown voltage characteristics. The breakdown voltages of the p-LDMOSFETs with both the CRS and the URS in an off-state were nearly the same. However, the p-LDMOSFET with the URS improved the breakdown voltage in on-state by 30%, while the saturated drain current of the p-LDMOSFET with the URS was only 4% lower than that of the p-LDMOSFET with the CRS. Our results demonstrate that the p-LDMOSFET with an uneven racetrack source can be used in PDP driver ICs with higher breakdown voltage.

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