Millimeter Wave MMIC Low Noise Amplifiers Using a 0.15 μm Commercial pHEMT Process

Byung-Jun Jang, In-Bok Yom, and Seong-Pal Lee

This paper presents millimeter wave monolithic microwave integrated circuit (MMIC) low noise amplifiers using a 0.15 μm commercial pHEMT process. After carefully investigating design considerations for millimeter-wave applications, with emphasis on the active device model and electomagnetic (EM) simulation, we designed two single-ended low noise amplifiers, one for Q-band and one for V-band. The Q-band two stage amplifier showed an average noise figure of 2.2 dB with an 18.3 dB average gain at 44 GHz. The V-band two stage amplifier showed an average noise figure of 2.9 dB with a 14.7 dB average gain at 65 GHz. Our design technique and model demonstrates good agreement between measured and predicted results. Compared with the published data, this work also presents state-of-the-art performance in terms of the gain and noise figure.

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I. INTRODUCTION

Low cost, high performance millimeter wave monolithic microwave integrated circuit (MMIC) low noise amplifiers are required for many commercial and military system applications. These include wireless LANs, car radars, and satellite communications. For the successful deployment of these services, highly reliable low-cost reproducible MMIC low noise amplifiers (LNAs) in the millimeter wave frequencies are required [1]. Thus far, millimeter wave LNA research has focused on InP-based HEMT processes. Compared to the GaAs-based pHEMT, the InP HEMT allows a reduction in the noise figure of approximately 1dB at V-band. Nevertheless, cost, manufacturability, and productivity issues have not yet been resolved. On the other hand, the higher maturity of GaAs-based pHEMT processes yields superior reliability, lower costs, and higher reproducibility of the devices over InP-based HEMT [2], [3].

Designing millimeter-wave low noise amplifiers using a commercial GaAs-based pHEMT process is more difficult than designing low frequency MMICs because the GaAs-based pHEMT process has been generally used on Ka-band applications.

First of all, accurate and verified active device models are needed. Especially, MMIC LNA designs at V-band often require smaller devices than the standard device provided by most commercial GaAs foundries. In addition, the operating frequency can be beyond the upper frequency foundries guarantee.

Thus far, millimeter wave MMIC low noise amplifiers are normally designed using scaled and extrapolated small signal/noise models of relatively large devices. Because of

scaling to smaller devices and extrapolation to higher frequencies, the use of the resultant model invariably leads to several design iterations [4], [5].

To circumvent these scaling and extrapolation problems and, thus, to predict small signal and noise parameters accurately, we used the distributed device model recently introduced by TRW [6].

Design of millimeter wave LNAs also requires accurate models of passive components and coupling and parasitic considerations in the final layout. Normally, passive models below Ka-band are fairly accurate. As frequencies approach millimeter wave, their accuracy and degree of uncertainty are generally unknown. Efficient and extensive use of commercial electromagnetic (EM) simulators can improve accuracy.

This paper presents our careful circuit design of Q- and V-band MMIC LNAs. Design considerations for millimeter wave LNAs are discussed in section II, followed by the circuit design in section III. The measured results and conclusion are presented in sections IV and V, respectively.

II. DESIGN CONSIDERATIONS FOR MILLIMETER-WAVE MMIC LNA

HEMT Modeling – MMIC LNA designs at millimeter-wave often require smaller devices than the standard devices provided for in the design rules of most GaAs foundries. Normally, large periphery devices, such as 80 μm, 120 μm, and 200 μm are standard devices provided by foundries. Foundries develop these standard models based on DC to 50 GHz measured S-parameters and DC to 40 GHz measured noise parameters. Thus, to use devices smaller than standard devices in millimeter-wave applications, we must scale and extrapolate from the standard devices. Scaling with gate width can be done by using scaling equations. Unfortunately, scaling equations are normally valid for gate widths from 75% to 125% of the original gate width [7].

We used TRW's 40-μm and 60-μm gate width pHEMTs for the V- and Q-band LNA designs, respectively. We selected these device sizes because they provided good impedance ranges for matching the circuit design at each frequency band and ultimately for wideband characteristics. The bias condition was 2V, 50% *Gmpeak*. A 40-μm device cannot be scaled accurately from a standard device model of 80-μm gate width because of scaling equation limitations. We used the distributed model shown in Fig. 1.

This model looks like a more complex approach than other traditional models, where only measured device S-parameters are used for modeling. This model uses one-fingered elementary devices from TRW, fed by lumped passive networks. Because this model was based on a long-term

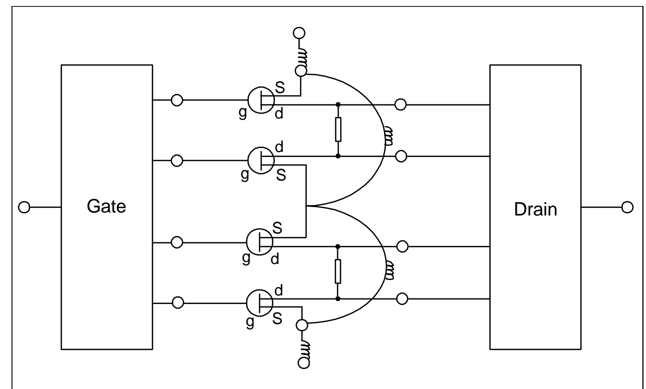

Fig. 1. Distributed model for the HEMT.

database of one-fingered elementary devices, an accurate simulation up to V-band is feasible [6].

To simulate the device's passive networks exactly, this model uses LIBRA^{TM} and SONNET^{TM} for modeling the gate distribution network, drain distribution network, and source air bridges.

The Field Effect Transistor (FET) basic theory assumes that any non-scalable effect is mainly associated with the passive structure of the electronic device, while the intrinsic region can be practically scaled in a proportional way [8], [9]. The distributed model embeds these one-fingered elementary device models within equivalent circuit networks simulating the interconnect structure of our device layouts. Using these LIBRA^{TM} models and four one-fingered elementary devices, we were able to make an accurate model up to V-band.

Figure 2 shows the calculated minimum noise figure and associated gain at 65 GHz with respect to the gate width using the distributed model. When the gate width was increased, the

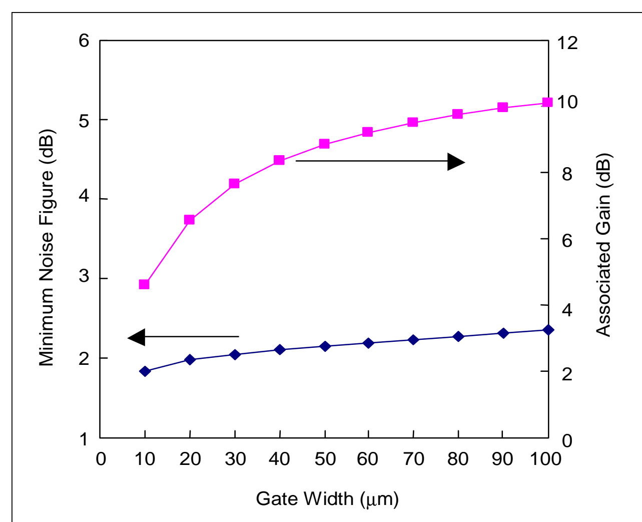

Fig. 2. Calculated gate width dependence of the minimum noise figure and associated gain at 65 GHz.

minimum noise figure and gain slightly degraded. When the gate width was decreased to less than 30 μm, the associated gain decreased rapidly. In view of achieving a high gain and a low noise figure simultaneously, we selected a gate width of 40-μm for the V-band MMIC LNA. For a 40-μm HEMT device, a minimum noise figure of 2.1 dB can be obtained at 65 GHz, with a maximum stable gain (MSG) of 8.3 dB. Similarly, we selected a gate width of 60-μm for the Q-band MMIC LNA.

Passive Component Modeling – Designing millimeter-wave amplifiers requires accurate modeling of passive components. Especially, discontinuities and transmission line coupling greatly impact the accuracy of passive components. Therefore, we analyzed all the passive components including the MIM (Metal-Insulator-Metal) capacitors and the via holes with a full wave EM analysis tool (SONNET™ software).

III. LOW NOISE AMPLIFIER CIRCUIT DESIGN

We used LIBRA™ to design two-stage low noise amplifiers to optimize the gain and noise figures in Q- and V-bands. The active and passive models described in the previous section were linked to the simulator and employed in the design.

A circuit topology for the V-band MMIC LNA is represented in Fig. 3.

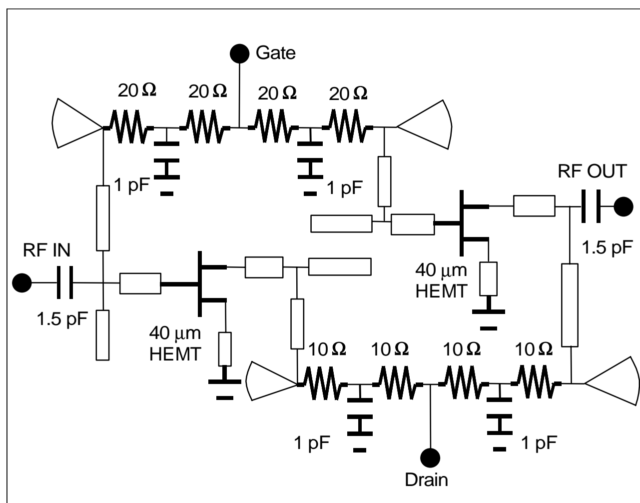

Fig. 3. Circuit topology for the V-band MMIC LNA.

A single-ended architecture using a common-source stage was chosen for the low noise figure and moderate gain. The matching circuit was designed in the following order: input, interstage, and output.

The input matching network was most important in that it determined the noise figure. Source inductive feedback was used for stabilization and to improve the input matching of the device simultaneously [10]. The feedback value of 20×80 μm was chosen to ensure a low noise figure and good input Voltage Standing Wave Ratio (VSWR).

The interstage matching circuit was designed to transform the output impedance of the first stage transistor to the optimum input impedance of the second-stage transistor. We adjusted the length of the source inductive feedback to choose the optimum input impedance of the second-stage transistor. The feedback value was chosen to ensure a low noise figure while giving a moderate gain. Our design of the coupler structure gave a direct impedance transformation between the stages and thereby reduced inaccuracy in the DC block capacitor.

We designed the output matching circuit so that it would transform the output impedance of the second-stage transistor to 50 Ω. To improve the matching bandwidth, we used an open stub.

The drain bias was applied through the on-chip 10 Ω resistors. For bias circuits, we used radial stubs because they have broadband ground characteristics and low insertion loss. Low-frequency stability R-C networks were added after the radial stub to ensure broadband stability without introducing significant noise in the pass-band. The optimization criterion for the overall two-stage amplifier was a stability factor of $K > 1$ for in-band and a sufficiently high value of $K > 10$ for out-of-band frequencies.

For the V-band design, we avoided MIM capacitors for critical RF matching and used them only for DC biasing to minimize sensitivity to process variations. For ease of on-wafer testing, the amplifier was designed to operate with one common drain and one common gate bias.

An important focus of design was the EM simulation, because the designed layout was very densely integrated to reduce the MMIC size. Although a full wave EM analysis tool analysed all the passive components, we had to calculate the coupling and parasitic of certain structures in the final design. Before the EM simulation, we divided the microstrip circuits into known structures such as Microstrip Line (MLIN), and unknown structures that were needed to EM-simulate. Using these block-level EM simulation results, the layout was completed. Then, we once more analyzed with EM all the passive structures, including the MIM capacitors and via holes. Because EM simulation is very time-consuming, it is important to divide the circuit effectively. In this circuit, we divided the circuit into three sub-blocks. For example, the input matching circuit and feedback line below the first FET, including the via hole, were entirely EM-simulated using 4-port circuits.

The LNA was fabricated in a 100 μm thick pHEMT wafer. The chip size of the amplifier was 2.2 mm×1.5 mm. A photograph of the V-band MMIC LNA is shown in Fig. 4.

After completing the EM simulation and final layout, we calculated the yield performance of the designed amplifier. To explain the yield reasonably, we used a long term database of

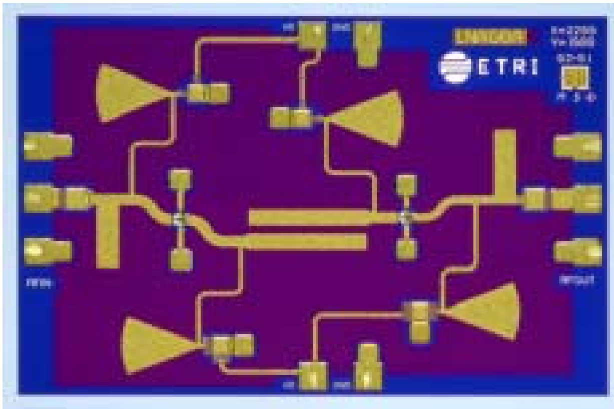

Fig. 4. Photograph of the V-band MMIC LNA.
(Die size is 2.2 mm×1.5 mm)

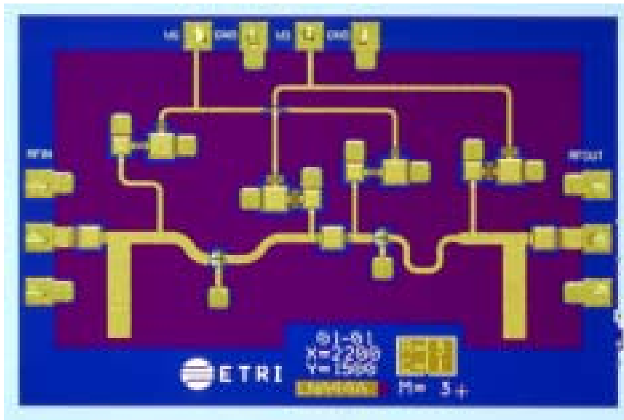

Fig. 5. Photograph of the Q-band MMIC LNA.
(Die size is 2.2 mm×1.5 mm)

one-fingered elementary devices from the 90 wafers. Inserting these values into the LIBRA simulator's discrete-value data file, we were able to calculate a realistic yield variation.

We used the same method to design the Q-band MMIC LNA, except for the interstage matching and bias network. A photograph of the Q-band LNA is shown in Fig. 5. An MIM capacitor was incorporated in the interstage matching circuit for the DC block to reduce the entire chip size. The chip size of the Q-band amplifier was 2.2 mm×1.5 mm.

IV. MEASURED RESULTS

The MMIC LNAs were fabricated with a TRW commercial 0.15 µm pHEMT process on 4-mil (100 µm) thick GaAs substrates [7].

The small signal S-parameters and noise parameters of the amplifiers were tested on-wafer. The measured and simulated small-signal gain and return loss of the V- and Q-band amplifiers are shown in Figs. 6(a) and (b), respectively.

Simulated and measured results compare very favourably over the entire frequency range. For the V-band design, the gain was higher than 14 dB from 58 to 65 GHz. The best result for the V-band amplifier demonstrated a 2.7 dB noise figure and a 16 dB gain at 65 GHz. A bandwidth of 7 GHz and a less than 1 dB gain variation vs. frequency were achieved. The Q-band amplifier also showed a high gain of 18 dB from 40 to 44 GHz. The high gain and flat response of the amplifiers is attributed to the optimum feedback and matching circuit design.

Noise measurement was performed using a noise measurement set-up. Figures 7(a) and (b) show the measured noise figure and associated gain as a function of operation frequency for V- and Q-band amplifiers, respectively. For the V-band amplifier, the noise figure was about 2.9 dB at 65 GHz and the associated gain was 14.7 dB, which corresponds to the lowest noise figure reported for 0.15-µm GaAs-based HEMT LNAs.

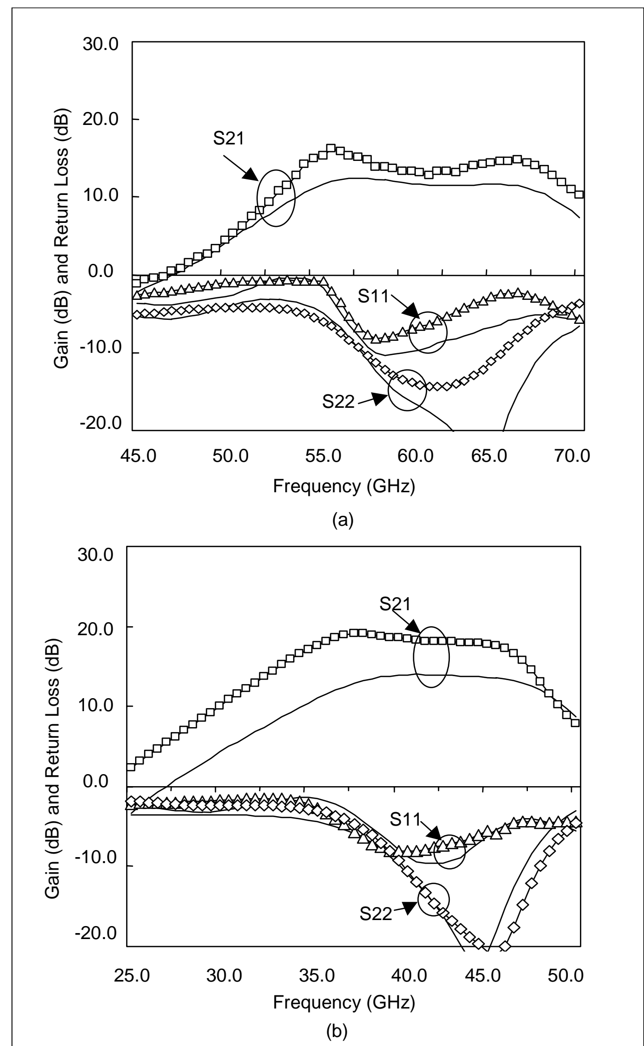

Fig. 6. Simulated and measured characteristics of (a) V- and (b) Q-band LNAs. Solid lines are for simulated characteristics.

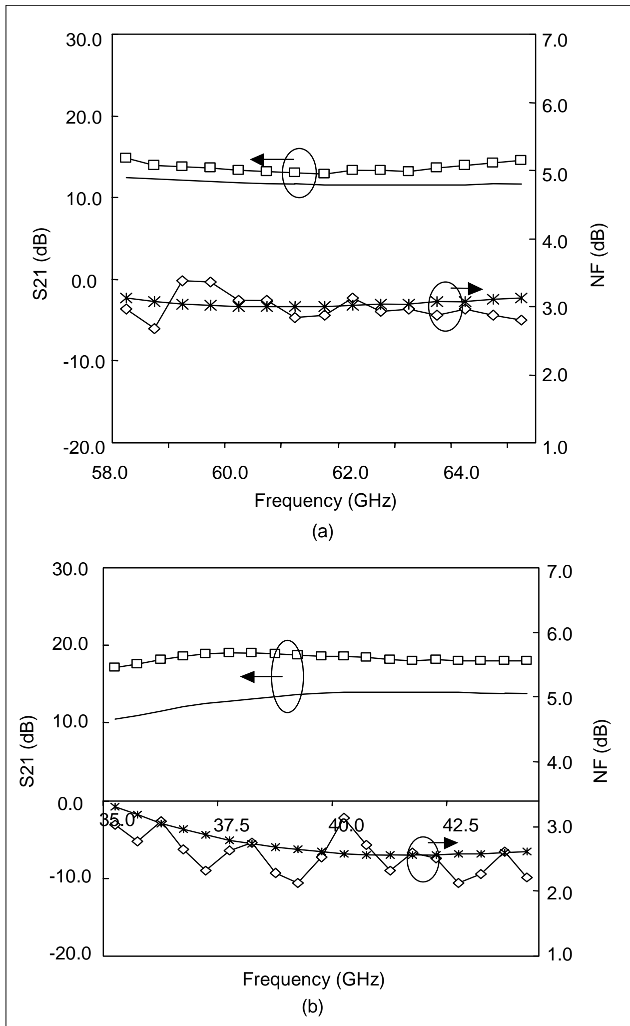

Fig. 7. Simulated and measured gain and noise characteristics of (a) V- and (b) Q-band amplifiers. Solid lines are for simulated characteristics.

A yield of above 60% (54 chips out of 90 chips) was achieved using a gain specification of 14 dB minimum and a noise figure of 3.5 dB maximum from 58 to 65 GHz. The gain and noise variation was about 1 dB from 58 to 65 GHz. Figure 6 shows the gain and noise distribution of the amplifiers from four wafers at 65 GHz. At 65 GHz, the amplifier shows a 2.9 dB average noise figure and a 14.7 dB average gain. To our knowledge, this is the best average gain and noise figure for GaAs-based MMIC LNAs using a commercial process in this frequency band. Figures 7 and 8 demonstrate that the MMIC LNA shows a reasonable noise figure, in good agreement with the predicted results. The gain is slightly higher, however, than predicted, but the gain slope and gain variation are in good agreement with the predicted results.

The Q-band amplifiers showed an average noise figure of 2.2 dB with an 18.3 dB associated average gain. The measured and simulated results show good agreement except for a difference in the magnitude of the gain.

Table 1 compares the performance of the V-band amplifier with the published data. To our knowledge, these are the best average gain and noise figures for GaAs-based MMIC LNAs in this frequency band. These values are more attractive than those achieved with more complex device technologies (for example, a 0.1-µm InP-based HEMT technology).

These results indicate that our design procedure is effective for the design of millimeter-wave MMIC low noise amplifiers.

V. CONCLUSION

This work described the design approach and performance for millimeter wave band low noise amplifiers based on a 0.15 µm pHEMT. MMIC low noise amplifiers at V-band and

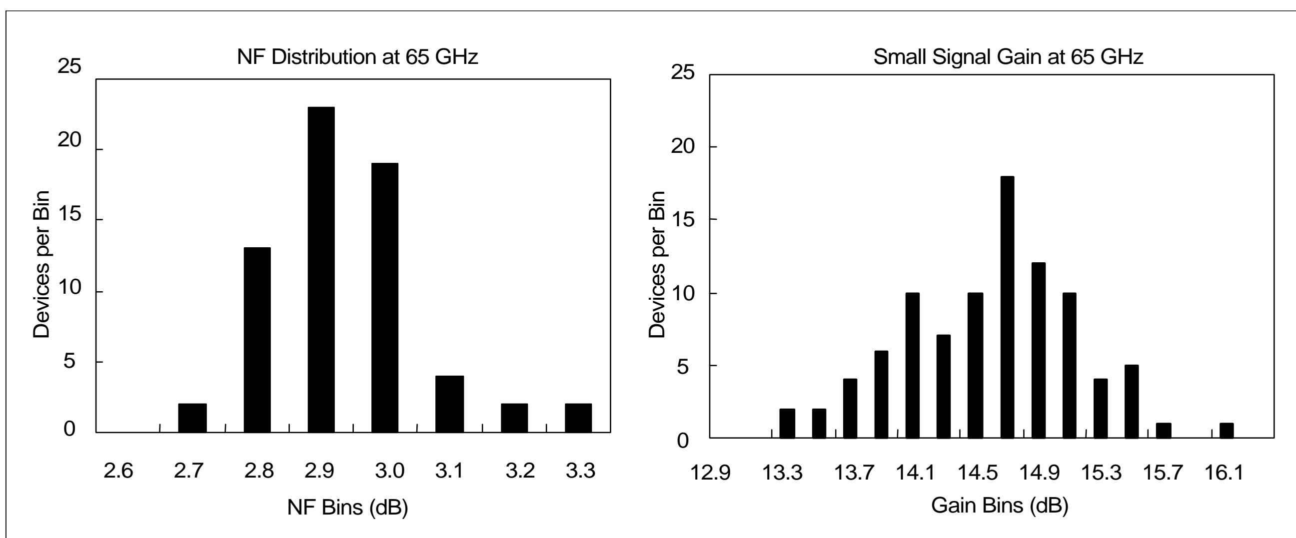

Fig. 8. Small signal gain and noise figure distribution of 90 measured V-band amplifiers at 65 GHz.

Table 1. Comparison of V-band MMIC LNA Performance: Frequency of Operation (Freq.), Process, Gate Length (Gate), Number of Stages, Gain and Noise Figure (NF) are compared for various V-band MMIC amplifiers (including the ones developed in this study).

REF	[3]	[11]	[12]	[13]	This work
Freq. (GHz)	59	61.5	62	61	65
Process	GaAs	GaAs	InP	InP	GaAs
Gate (μm)	0.15	0.15	0.1	0.10	0.15
Stage	2	2	3	2	2
Gain (dB)	9.3 (max)	10.0 (max)	24 (max)	13 (max)	14.7 (average)
NF (dB)	3.0 (min)	3.0 (min)	2.7 (min)	2.2 (min)	2.9 (average)

Q-band were fabricated and evaluated. The V-band amplifier exhibited an average gain of 14.7 dB and an average noise figure of 2.9 dB at 65 GHz. The Q-band amplifier exhibited an average gain of 18.3 dB and an average noise figure of 2.2 dB at 44 GHz.

This work demonstrates that the 0.15 μm GaAs-based commercial pHEMT technology can be successfully extended to produce low noise amplifiers required for millimeter-wave systems, provided that careful circuit design methodology and suitable device models are developed.

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