# Active-Matrix Field Emission Display with Amorphous Silicon Thin-Film Transistors and Mo-Tip Field Emitter Arrays

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**We present, for the first time, a prototype active-matrix field emission display (AMFED) in which an amorphous silicon thin-film transistor (a-Si TFT) and a molybdenum-tip field emitter array (Mo-tip FEA) were monolithically integrated on a glass substrate for a novel active-matrix cathode (AMC) plate. The fabricated AMFED showed good display images with a low-voltage scan and data signals irrespective of a high voltage for field emissions. We introduced a light shield layer of metal into our AMC to reduce the photo leakage and back channel currents of the a-Si TFT. We designed the light shield to act as a focusing grid to focus emitted electron beams from the AMC onto the corresponding anode pixel. The thin film depositions in the a-Si TFTs were performed at a high temperature of above 360 ℃ to guarantee the vacuum packaging of the AMC and anode plates. We also developed a novel wet etching process for $n^+$-doped a-Si etching with high etch selectivity to intrinsic aSi and used it in the fabrication of an inverted stagger TFT with a very thin active layer. The developed a-Si TFTs performed well enough to be used as control devices for AMCs. The gate bias of the a-Si TFTs well controlled the field emission currents of the AMC plates. The AMFED with these AMC plates showed low-voltage matrix addressing, good stability and reliability of field emission, and good light emissions from the anode plate with phosphors.**

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## I. INTRODUCTION

The field emission display (FED) has emerged as a leading contender in display technologies because it combines the best features of the cathode ray tube (CRT) and flat panels [1], [2]. Whereas in a CRT the filament emits hot electrons, in an FED the field emitter array (FEA) cathode emits cold electrons to bombard phosphors in the anode plate. The matrix addressing of FEAs is mainly a passive multiplexing in conventional FEDs, in which the driving voltage is high except for the specially processed small gate FEA by Candescent [3]. The emission currents of passive multiplexed FEAs are very sensitive to driving voltage, and this causes a problem in uniformity. While much effort has been focused on simple-matrix FEA cathodes, stability and reliability of the conventional FEA cathodes are still key problems in the commercialization of FEDs. These difficulties can be overcome by applying an active-matrix cathode (AMC) scheme [4]-[9]. The AMC has many advantages, such as low-voltage addressing regardless of the high voltage required for field emission, good pixel isolation that reduces cross-talk and fatal short failure, and good field emission uniformity and stability.

Metal-oxide-semiconductor field-effect transistor (MOSFET)-controlled Si FEAs [4], [5] and polycrystalline silicon (poly-Si) [6]-[8] and amorphous silicon (a-Si)-based FEAs [9] controlled by thin-film transistors (TFTs) have been employed in AMC architecture. However, a fully vacuum-packaged active-matrix field emission display (AMFED) with an AMC plate on glass has not been reported. The control transistor for the AMC has been MOSFET or TFT according to the substrate. The glass substrate is indispensable to the fabrication of low-price, large-

area displays. Thus, the successful implementation of an a-Si TFT in the AMC is a crucial point for the development of the FED as a competitive display device. In our study, a prototype AMFED with the AMC on a glass substrate was fabricated for the first time and demonstrated to show good display images with a low-voltage scan and data driver circuits. We designed and developed a new cathode architecture with a light shield and focusing grid including a novel a-Si TFT process for AMC plates.

## II. DEVICE AND PROCESS DESIGN FOR THE AMFED

The prototype AMFED panel consisted of an AMC plate and an anode plate of green phosphor having 64×(64×3) sub-pixels with a pitch of 450 μm by 200 μm. Figure 1 shows schematic diagrams of the AMC plate and its sub-pixel structures with display input signals. We designed the AMC sub-pixel to have an a-Si TFT as a control switch for the Mo-tip FEAs on a low-sodalime glass. In each sub-pixel, the conical Mo-tips were constructed on the drain electrode of an a-Si TFT together with a light shield (LS)/focusing grid (FG) that is described in detail below. We selected low-sodalime glass as the AMC substrate for its feasibility in the a-Si TFT process and its immunity to alkali metals. The immunity can be obtained with the help of a proper buffer layer deposited on the substrate. The low-sodalime glass also has a relatively large thermal expansion coefficient, which is necessary for frit sealing in vacuum packaging, and good vacuum durability, which is indispensable in the fabrication of FEDs. We designed the a-Si TFTs in the conventional inverted stagger structure that has been commonly used in TFT-switched liquid crystal displays (LCD) [10]. A slight modification in the a-Si TFTs from the conventional device and process architecture enabled us to fabricate a large-area AMFED for a relatively low cost.

Without further modification, the a-Si active layer in our AMC would be exposed to stray light from the front anode plate which contains phosphors, causing light-induced leakage currents and consequent deterioration of the switching properties of the a-Si TFT. Therefore, it was necessary to add a light shield on the backside of the gate electrode of our AMC; this differed from the TFT-LCD in which the gate electrode blocks the light from a back lighting unit. To remove the light-induced leakage currents, we designed our AMC to have a light shield of metal above the a-Si TFT. The light shield did not require any additional process because it could be formed through an appropriate layout with the electron extraction gate of the Mo-tip FEA. Under the normal operation of the AMC, the light shield is biased to zero or a negative volt to get rid of

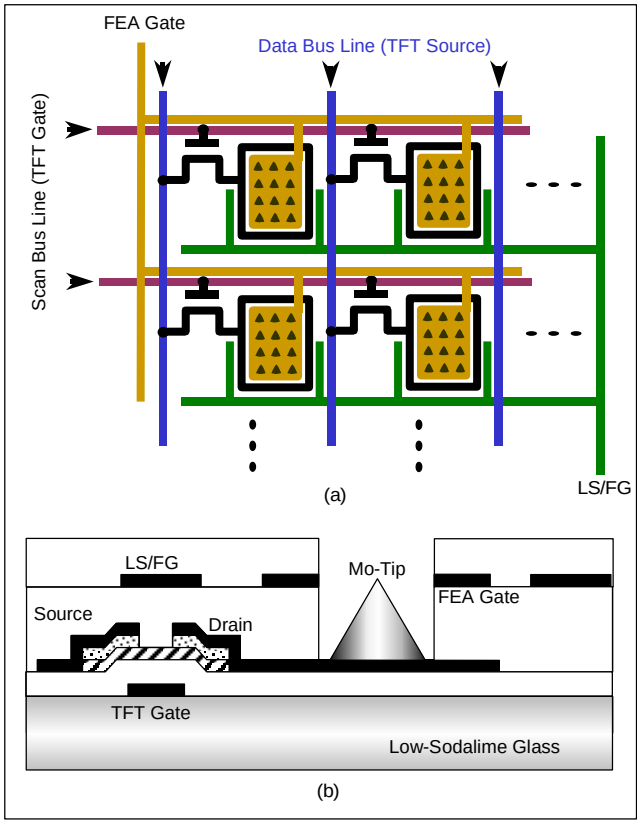


Fig. 1. Schematic diagrams of the AMC plate with display signal inputs and a cross-section of an AMC sub-pixel with an a-Si TFT and a Mo-tip FEA.

the back channel leakage currents of the a-Si TFT induced by the FEA-gate bias voltage. We intended the light shield to act as a focusing grid to focus emitted electron beams from the AMC onto the corresponding anode pixel by drawing the LS around the Mo-tip FEA as well as above the a-Si TFT.

The process design of the AMC on the glass substrate was straightforward: an a-Si TFT process followed by Mo-tip FEA formation on the drain electrode of the a-Si TFT. However, we had to consider the deposition temperature of the a-Si films from the viewpoint of the vacuum packaging process in the FED. During the vacuum sealing process, the temperature of the samples rises above the melting temperature of frit glass, around 350 °C. This high temperature process can bring about serious degradation to the electrical characteristics of an a-Si TFT fabricated by the conventional plasma-enhanced chemical vapor deposition (PECVD) process [10]. Therefore, the deposition temperature of thin films in an a-Si TFT must be high enough to prevent the samples from being damaged by the high-temperature vacuum sealing process. In our fabrication process of the AMC we kept the deposition temperature of the a-Si films above 350 °C. We also lowered the vacuum sealing temperature to below 350 °C by using an in-line laser-assisted packaging process, which resulted in

successful maintenance of the a-Si TFT performance, even after the vacuum packaging.

## III. FABRICATION PROCEDURE OF THE AMFED

The a-Si TFT process in our AMC plate followed the conventional inverted stagger structure procedure. However, to achieve a very thin active layer of below 600 Å and to minimize the number of process steps, we developed a new wet back-channel-etch (BCE) process using $CH_3COOH$, $HNO_3$, and HF solutions for the $n^+$-doped a-Si etching. The buffer layer of amorphous silicon nitride (a-$SiN_x$) was deposited by PECVD at 260 °C onto cleaned glass substrates. A 100-nm-thick Cr was sputtered and patterned to form the TFT gate and scan bus line. Then the gate a-$SiN_x$, intrinsic a-Si, and $n^+$-doped a-Si were successively deposited by PECVD at 380 °C without breaking the vacuum. The film thickness of the SiNx, intrinsic a-Si, and $n^+$-doped a-Si was 350 nm, 60 nm, and 40 nm, respectively. A 150-nm-thick Cr film was sputtered on the $n^+$-doped a-Si layer and etched to form the source/drain and data bus line. We then used the wet BCE process to remove the $n^+$-doped a-Si layer on the active channel of the a-Si TFT. The developed wet BCE technique showed a high etch selectivity of up to 15:1 between the $n^+$-doped a-Si and intrinsic a-Si while the selectivity mainly varied with the HF-volume ratio of stock solutions. The etch rate of the $n^+$-doped a-Si was easily controlled by changing the HF-volume ratio from 10 nm/min to 180 nm/min with a very high uniformity of within 5% in a 5-inch wafer. These etch properties enabled us to fabricate the BCE-processed a-Si TFT with a very thin active layer.

After the BCE process, an 800-nm-thick a-SiNx and a 200-nm-thick Cr were deposited on the sample for the FEA gate dielectric and FEA gate, respectively. The FEA gate was patterned by wet etching of the Cr film, and then a 120-nm-thick buffer a-$SiN_x$ was deposited by PECVD to prevent the peeling-off of the FEA gate and/or dielectric film from the sample during the post-evaporation process for the Mo-tips. FEA gate holes of about 1.1 μm in diameter were formed on the drain electrode of the a-Si TFT through lithography using a contact aligner and dry etching of the Cr and a-SiNx films. Al for the parting layer and Mo for the tips were evaporated onto the sample with an appropriate angle to the e-beam sources. Finally, the Mo film was lifted off by a KOH dip and conical Mo-tips remained inside the FEA gate holes. The overall tip-formation process in the AMC fabrication was optimized for elimination of the side effects on the a-Si TFTs.

For the anode plate, the green phosphor of ZnS:Cu,Al was printed using lithography on an ITO-patterned glass substrate. Several bar-type spacers made of photosensitized glass were placed on the anode plate. The height and width of the spacers were 450 μm and 100 μm, respectively. The anode plate was annealed at 430 °C in an air-ambient oven before vacuum packaging. The in-line vacuum packaging of the AMC and anode plates, including the activation process of a non-evaporable getter, was performed in a load-locked high vacuum chamber system using a continuous Nd:YAG laser. The AMC plate was kept at a temperature as low as about 300 °C during the vacuum packaging. The detailed vacuum sealing and getter activation processes were described in recent reports [11], [12].

## IV. RESULTS AND DISCUSSION

We successfully integrated a-Si TFTs with Mo-tip FEAs on a glass substrate for an AMC plate. Figure 2 shows scanning electron microscopy (SEM) images for the top view of the fabricated AMC sub-pixel and the cross-sectional view of a single Mo-tip in the FEA gate hole. The AMC sub-pixel had an a-Si TFT with an LS above it, a Mo-tip array having 400 Mo-tips, and two FGs along with the FEA gate and scan/data bus lines, in which the LS was connected with one of the two

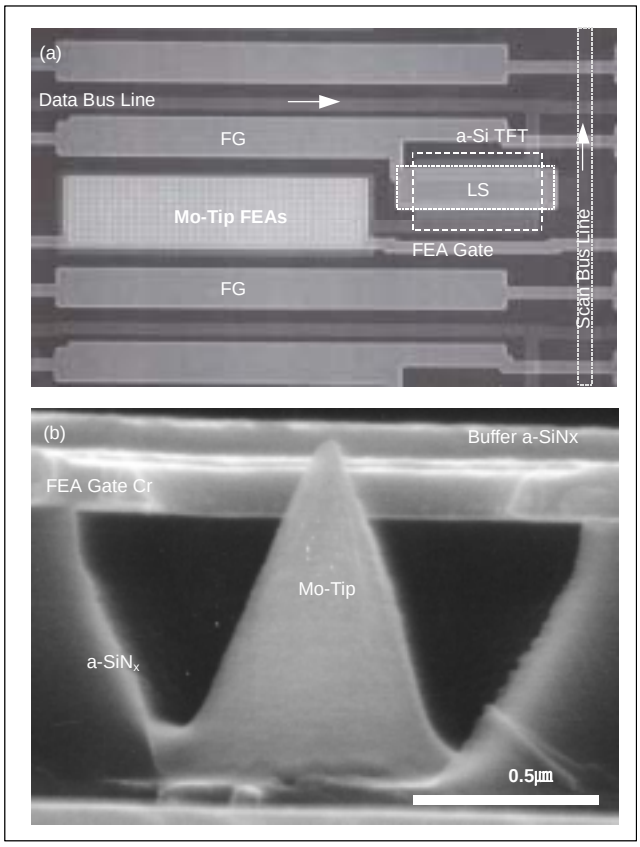


Fig. 2. SEM images for the top view of a fabricated AMC and a cross-sectional view of a single Mo-tip in the FEA gate hole.

FGs, and the scan and data bus lines terminated at the gate and source of the a-Si TFT, respectively. The Mo-tips inside the FEA gate holes had an end-radius of about 500 Å and a height of 1.0 μm. The gate length was 20 μm and the channel width was 100 μm for the a-Si TFT.

The output and transfer characteristics of the wet BCE-processed a-Si TFT with a 60-nm-thick active a-Si layer deposited at 380 °C are shown in Fig. 3. The field effect mobility and threshold voltage extracted from the saturation region of the a-Si TFT were approximately 0.15 $cm^2/V{\cdot}s$ and 9.5 V, respectively. The a-Si TFT processed at such a high temperature of 380 °C showed moderately degraded properties compared to that processed at around 300 °C with values of 0.7 $cm^2/V{\cdot}s$ and 4.5 V. However, the wet BCE and high-temperature processed a-Si TFT showed good linear and saturation behavior with a relatively high drive current of several μA (Fig. 3(b)). The devices showed little change for many hours in the transfer and output characteristics with electrical stress in the on-state biasing. These results indicate that the developed a-Si TFT can be efficiently used as a switching device for an AMC considering the required currents of about 1-10 μA per sub-pixel in FED applications.

Figure 4 exhibits the field emission characteristics of the fabricated AMC sub-pixel as functions of FEA ($V_{FG}$) and TFT gate voltages ($V_{TG}$). The field emission measurements were done under a vacuum of about $1\times10^{-6}$ Torr at room temperature and the data were plotted after an appropriate aging process for the Mo-tip FEA. The anode voltage was kept at 450 V with an AMC-to-anode spacing of about 500 μm during the measurements. The aging process at a relatively high emission current led to stable curves in the field emission plots. Moreover, the AMC device had very stable aging kinetics for field emitters with the limitation of emission currents by the a-Si TFT, and thus we could successfully activate Mo-tips to emit electrons without any tip-failure. Anode currents versus FEA gate voltage for various $V_{TG}$ are shown in Fig. 4(a). At each $V_{TG}$, the anode currents were well saturated above about 55 V

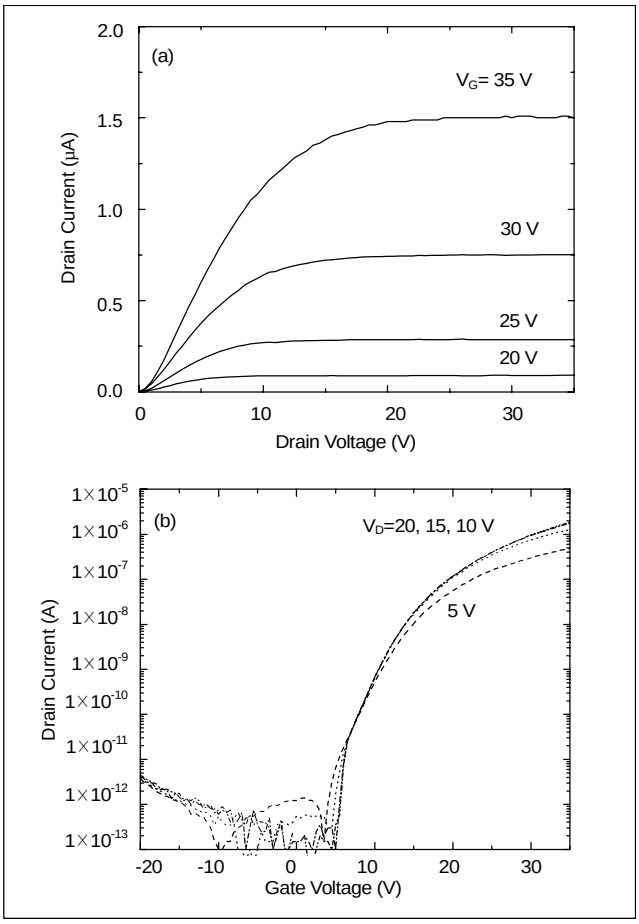


Fig. 3. Output and transfer characteristics of the a-Si TFT with a gate length of 20 μm and a channel width of 100 μm. The $V_G$ and $V_D$ denote the TFT gate and drain bias voltages, respectively.

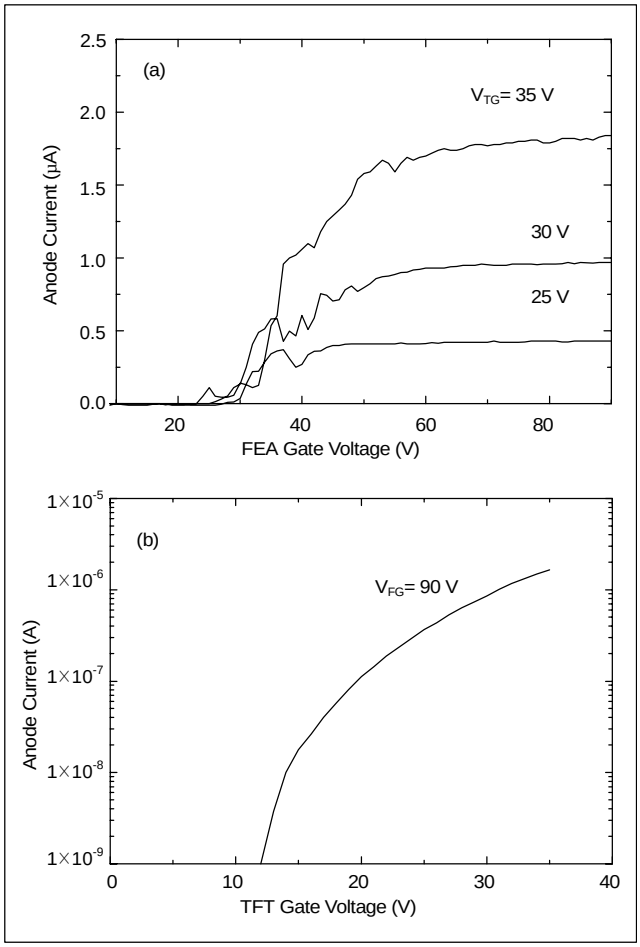


Fig. 4. Anode currents of an AMC sub-pixel at an anode voltage of 450 V: (a) as a function of the FEA gate voltage ($V_{FG}$) at various TFT gate voltages ($V_{TG}$), (b) as a function of the TFT gate voltage at a $V_{FG}$ of 90 V.

for $V_{FG}$ due to the limitation in field emission currents by the a-Si TFT. The saturated anode current was nearly identical to the drain current of the a-Si TFT operated in the saturation region for a given TFT-gate bias voltage (Fig. 3(a)). Some fluctuations in the field emission currents of the AMC sub-pixels were below the saturation region, which was due to the linear operation of the a-Si TFT. The linear region operation of the a-Si TFT was subjected to the intrinsic fluctuations of the field emission, resulting in an unstable field emission even for an AMC device. Figure 4(b) shows the switching characteristics of the AMC sub-pixels by the TFT gate at a constant $V_{FG}$ of 90 V. The off-state currents in Fig. 4(b) had some errors caused by the limitation of our measurement system at a low current level. We found that the field emission currents from the Mo-tip FEAs did nearly conform to the transfer characteristics of the a-Si TFT shown in Fig. 3(b). The TFT gate efficiently switched the anode currents for a constant $V_{FG}$, showing a high on/off ratio of above 1000 times in emission-currents by sweeping the TFT gate bias within a 30 V range.

We investigated the line-by-line field emission properties of the AMC plate with an anode plate having a blue phosphor of CaS:Pb [13] in the vacuum chamber (Fig. 5). During the tests all TFT gate lines were connected to a common bias, and each source line was selected for line emission. The light emission started at 45 V-and saturated over a 60 V-FEA-gate bias voltage for the $V_{TG}$ of 20 V. The light emission saturation for the increment of the FEA-gate bias confirmed the control of emission currents by the TFT-gate bias. Sweeping the TFT-gate bias voltage from 8 V to 20 V completely controlled the gray scale of light emissions.

We specially noted that the LS/FG was biased to zero volt during the measurements shown in Figs. 4 and 5. The LS/FG bias of 0 V resulted in the complete turn-off of field emission currents at a constant FEA-gate bias voltage. In case of the no LS/FG structure, the AMC sub-pixel was hardly turned-off by the TFT gate showing large leakage currents of above $10^{-8}$ A. Furthermore, the leakage current was still large even for the floating bias to the LS/FG. This implies that the function of the LS/FG is to prohibit the back channel of a-Si TFT turning-on by the FEA-gate bias voltage and to block the lights from the anode phosphor plate into the a-Si TFT in the AMC, resulting in a high on/off ratio for field emission currents. With the introduction of the LS/FG in the AMC architecture, we can easily achieve a high contrast AMFED addressed by a low-voltage scan and data signals through the a-Si TFT. In addition, the LS/FG biased zero or negative volt acts to focus electron beams from the cathode onto the corresponding anode pixel enhancing the color purity of the AMFED, as in the previous reports by Tang et al. [14], [15].

Figure 6 shows the first prototype AMFED panel vacuum-packaged using the in-line laser-assisted sealing process. The final pressure inside the fabricated AMFED panel was estimated to be less than $5\times10^{-6}$ Torr through an indirect

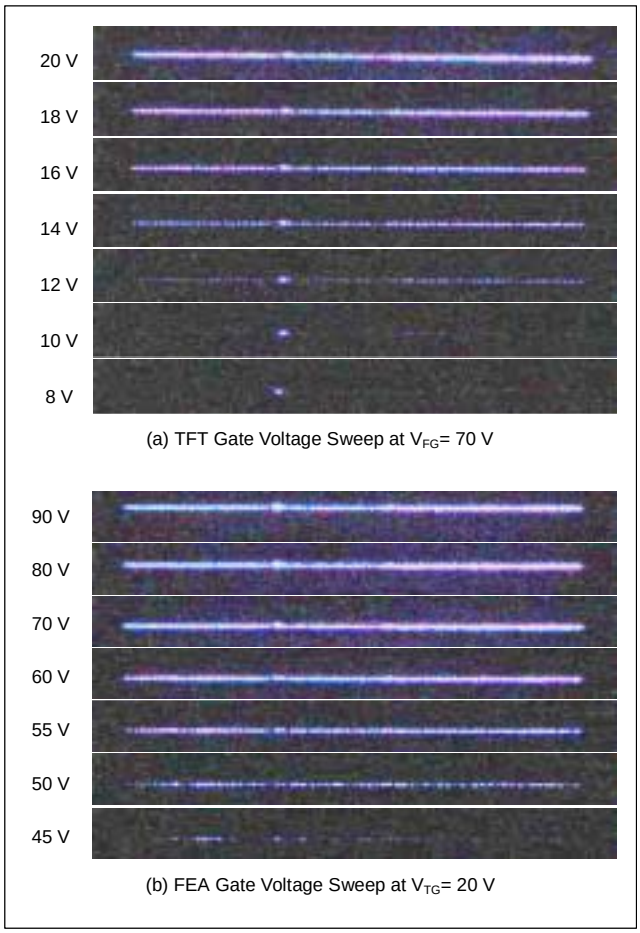


Fig. 5. Line-by-line light emissions for the AMC plate at an anode voltage of 450 V: (a) as a function of the TFT gate voltage at a $V_{FG}$ of 70 V, (b) as a function of the FEA gate voltage at a $V_{TG}$ of 20 V.

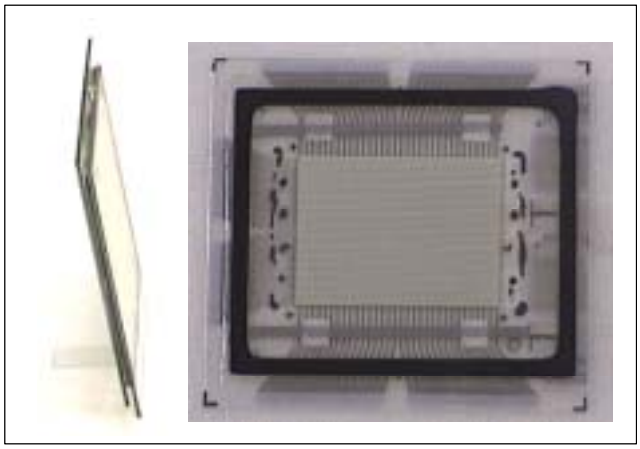

Fig. 6. Side and front photographs of the vacuum-packaged AMFED panel.

measurement method. It was done by comparing the pressure of an isolated high vacuum chamber before and after breaking the AMFED panel inside the chamber. Unlike the conventional FED, the AMFED panel has no evacuation tube and thus the in-line laser-assisted packaging process gave us an ideal flat panel display.

On the other hand, the vacuum packaging process can give rise to thermal damage to the a-Si TFT, resulting in some fatal errors in controlling field emissions. We checked the stability of the a-Si TFT and controllability of field emission currents after the laser-assisted vacuum packaging process. Figure 7 shows the transfer characteristics of the a-Si TFT in the vacuum-sealed AMC plate for a $V_D$ of 5 V. We did not find any changes in the transfer characteristics of the a-Si TFT after the vacuum packaging process, which confirms the preservation of the a-Si TFT with the packaging process. The maximum temperature of the packaging process was around 380 °C at the frit-sealing site and around 300 °C in the environment. The maximum temperature of the TFT sites during the packaging process was measured with a thermocouple to be about 330 °C, which was much lower than the deposition temperature (380 °C) of the active a-Si layer in the TFT.

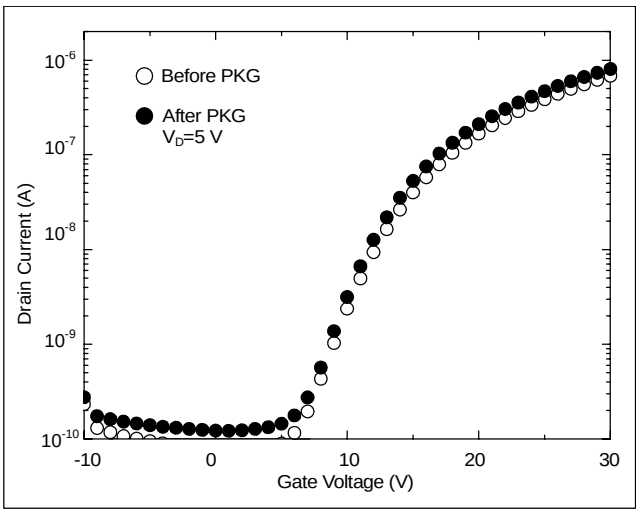


Fig. 7. Transfer characteristics of an a-Si TFT in the AMC plate before and after the vacuum packaging process.

The stability and reliability of the AMC plate was tested through a continuous-mode operation of field emissions (Fig. 8). The data points in Fig. 8 were taken from the mean values of 5 anode currents measured for 1 second with constant voltages. Figure 8(a) exhibits the field emission stability of the AMC devices compared to simple FEAs. The AMC showed very stable emission currents without any degradation, while the simple FEAs showed a large fluctuation in emission currents. This result suggests that field emission can be strongly

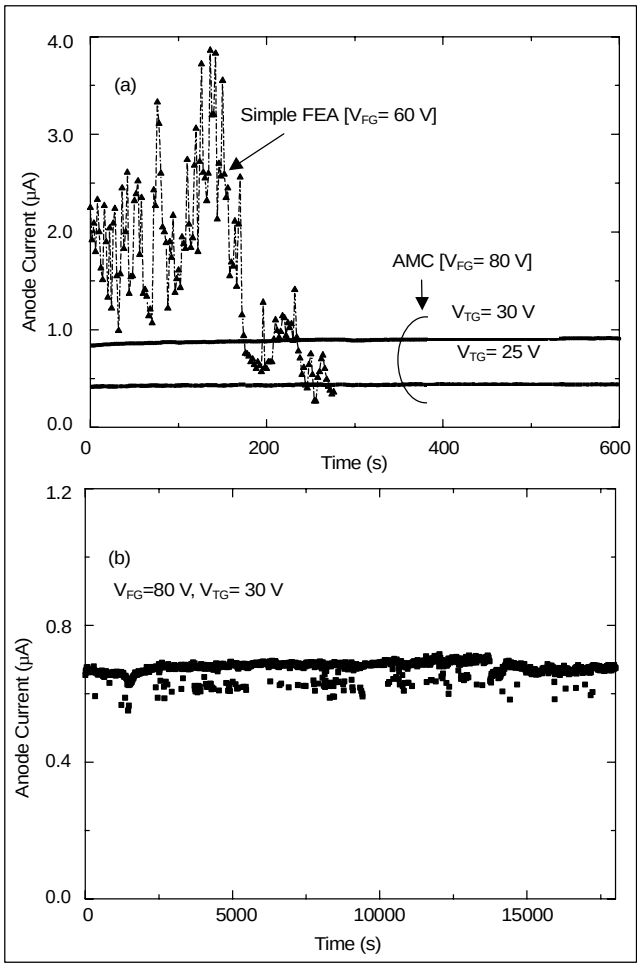


Fig. 8. Anode currents as a function of time at an anode voltage of 450 V showing (a) stability of a simple FEA and an AMC sub-pixel in a short time, and (b) reliability of an AMC sub-pixel in a relatively long time.

stabilized by an a-Si TFT in an AMC plate. The anode current of the AMC sub-pixel was maintained at the same level of over 18000 s, whereas some fluctuation deviating from the main trend of the emission current was observed. We think that the fluctuation was caused by a noisy interface between the PC and measuring units. We also confirmed that the emission currents were maintained through two days in the continuous-mode operation. In general, the FEA cathode operates in the pulse mode with a duty ratio of below 1/10, so we can say that there was no degradation for more than a 20-day pulse-mode operation. We think that there is no problem concerning reliability in integration of an a-Si TFT with a Mo-tip FEA.

Figure 9 shows a schematic signal diagram of the driving method for the fabricated AMFED panel and a displayed image on the panel. The display signals from the scan and data drivers were addressed to the gate and source of the a-Si TFT, respectively, in each sub-pixel. If the scan pulse had an amplitude of $V_s$ and a width of $t_s$ and the data pulse had $V_d$ and

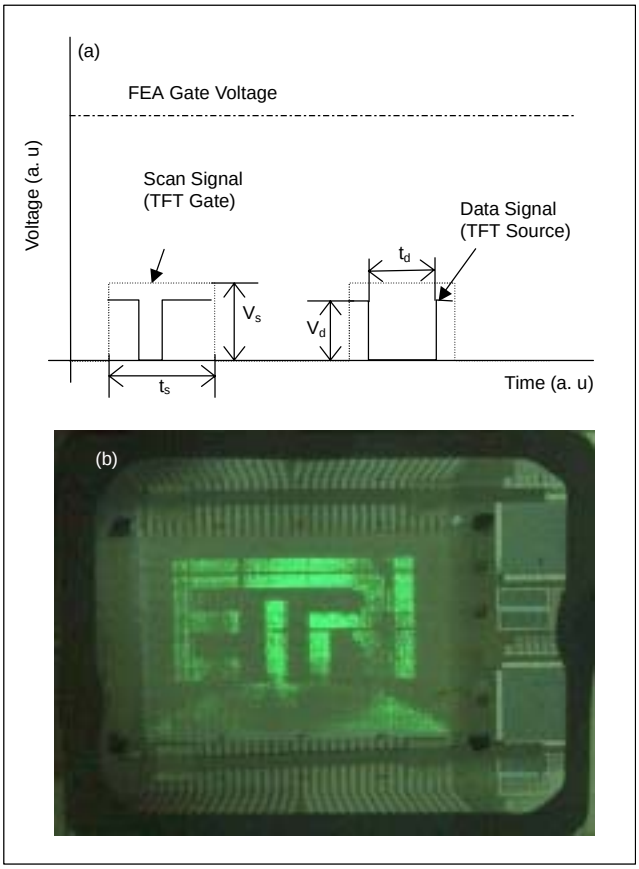


Fig. 9. Schematic signal diagram for scan and data signals with a constant FEA gate voltage and a displayed image (ETRI Logo) on the AMFED panel with a 30 V scan and data pulses.

$t_d$, then the electrons were emitted under the condition of $(V_s - V_d) > V_T$, where $V_T$ is the threshold voltage of the a-Si TFT. As a result, the scan and data signals can be lowered irrespective of a constant high voltage for field emissions, so the power consumption in driving the AMFED and the cost for integrated driver circuits can be greatly reduced. In addition, the electron emission was maintained only for $t_d$ within a given $t_s$ determined by the number of scan lines and display refresh rate. Therefore, the gray scale can be easily obtained by pulse width-modulated data signals addressed to the source of the a-Si TFT in the AMC sub-pixel. We achieved good images from the prototype AMFED with scan and data signals having a pulse amplitude of 30 V while the FEA gate and the anode plate kept constant voltages of 70 V and 400 V, respectively. Some defective points in the image shown in Fig. 9(b) were due to Mo-tip failures during the fabrication process. The fabricated AMFED successfully demonstrated good display images with a relatively high contrast ratio using low-voltage scan and data driver circuits, suggesting a technological breakthrough in FEDs.

## V. CONCLUSION

Our investigation confirmed the feasibility of AMFED technology through integration of a-Si TFTs with Mo-tip FEAs on a glass substrate. The field emission properties of the fabricated AMCs were well controlled by the TFT gate bias, showing good stability and reliability of field emissions and the possibility of low-voltage matrix addressing regardless of a high voltage for the field emission. The LS/FG in the AMC architecture gave a complete turn-off of field emission currents at a constant voltage required for field emission. In addition, the new wet BCE process and high temperature deposition of the a-Si film allowed us to fabricate inverted stagger TFTs with an ultra thin active layer and to guarantee the vacuum packaging of the AMC and anode plates using the in-line laser-assisted sealing process. The fabricated AMFED successfully demonstrated good display images with a low-voltage scan and data signals addressed to the a-Si TFT. The developed AMC technology with an in-line laser-assisted vacuum packaging process is very promising for highly stable, low-voltage driven FED applications.

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