

# A Serial Input/Output Circuit with 8 bit and 16 bit Selection Modes

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**ABSTRACT**— This paper presents a serial interface circuit that permits selection of the amount of data converted from serial-to-parallel and parallel-to-serial and overcomes the disadvantages of the conventional serial input/output interface. Based on the selected data length operating mode, 8 bit or 16 bit serial-to-parallel and 8 bit or 16 bit parallel-to-serial conversion takes place in data blocks of the selected data length.

## I. INTRODUCTION

Serial communication is one of the functions often required in the development of integrated microsystems. In most applications, when data is exchanged, a serial interface unit sends and receives bit sequences on the status of these bits to and from another unit that processes the bit sequence. The advantage of serial communication systems is the simplicity of the interconnection wire [1]-[6]. The serial input/output (SIO) unit is a serial interface used for communicating with other units [2], [3]. It is also important for low power consumption in portable applications [7], [8].

The amount of serial data is fixed in the conventional SIO. Generally, the width of the data is fixed at 8 or 16 bits [1]-[3]; an operator selects the 8 or 16 bit serial interface according to the design at issue. It is desirable, however, for an operator to be able to use a single interface and then selectively set the interface to either an 8 bit or 16 bit operating mode. Overcoming the problems of achieving a single interface with

an 8 bit or 16 bit operating mode, this paper presents a synchronous full duplex serial circuit with an 8 bit and 16 bit selection mode.

## II. THE STRUCTURE AND OPERATION OF THE PROPOSED SERIAL INPUT/OUTPUT INTERFACE

In general, an SIO circuit mainly consists of a transmit unit and a receive unit (Fig. 1). The amount of serial data is fixed in the conventional SIO, so the system cannot be reconfigured to change the amount of serial data. Thus an operator cannot use a single interface on a chip.

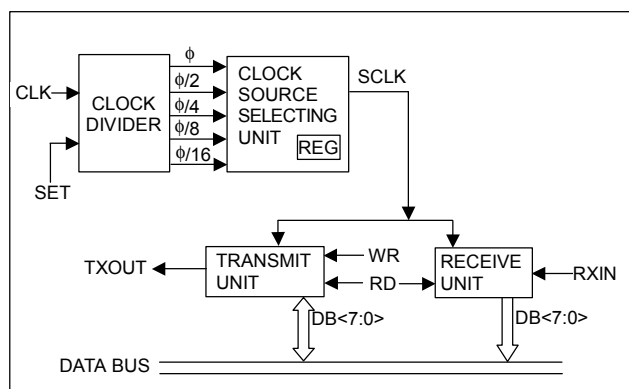


Fig. 1. A block diagram of the general 8 bit serial input/output interface circuit.

The proposed SIO interface overcomes the disadvantages of the conventional SIO interface. It provides an SIO interface which allows an operator to select between operation in different bit length modes. Figure 2 shows a block diagram of

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the proposed SIO interface circuit. The components of this figure have the same components as in the conventional serial interface circuit except for the ternary/tetrad counter and mode signal. A ternary/tetrad counter has an input signal with the selected clock SCLK, the set signal SET, and a mode signal. The mode signal indicates whether the SIO interface should operate in an 8 bit mode or a 16 bit mode. When the mode signal indicates operation in an 8 bit mode, the ternary/tetrad counter counts in mod 3 in accordance with the selected clock SCLK. When the mode signal indicates operation in a 16 bit mode, the ternary/tetrad counter counts in mod 4 in accordance with the selected clock SCLK. The amount of serial data transferred between the data bus and the transmit/receive unit is not fixed but is selectable between either 8 bit or 16 bit widths. Figure 3 shows a diagram of the transmit unit of the proposed SIO. In the 16 bit operating mode, the mode signal is logic level HIGH, the first mode-selection-enable unit transfers the serial data output from the first shift register TX1 to the serial input of the second shift register TX2. Because in the 16 bit operating mode the serial output of the first shift register TX1 is transferred by the first mode-selection-enable unit to the second shift register TX2, the parallel data input from both the first and second shift registers TX1 and TX2 is output during a predetermined period of time. In the 8 bit operating mode, the mode signal is logic level LOW, and the second shift register TX2 shifts in a logic low data stream. In the 8 bit operating mode, only the parallel data input to the second shift register TX2 is output as serial data because the first mode-selection-enable unit prevents the serial data output from the first shift register TX1 from reaching the serial input to the second shift register TX2.

Figure 4 shows a diagram of the receive unit of the

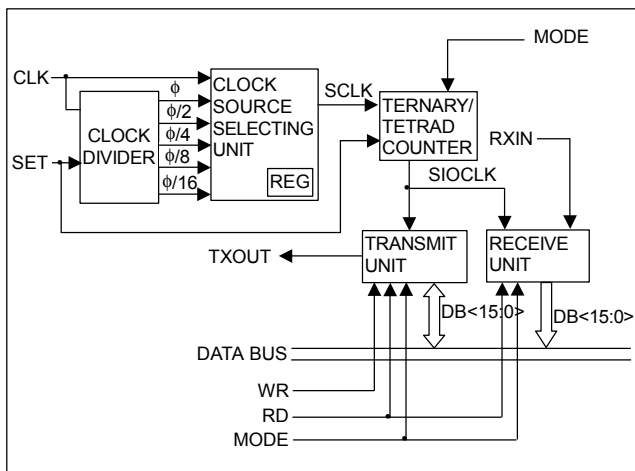


Fig. 2. The block diagram of the proposed 8/16 bit serial input/output interface circuit.

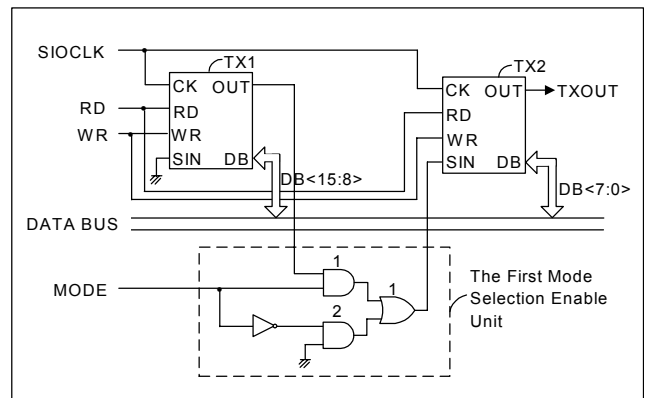


Fig. 3. The block diagram of the transmit unit of the proposed serial input/output interface circuit.

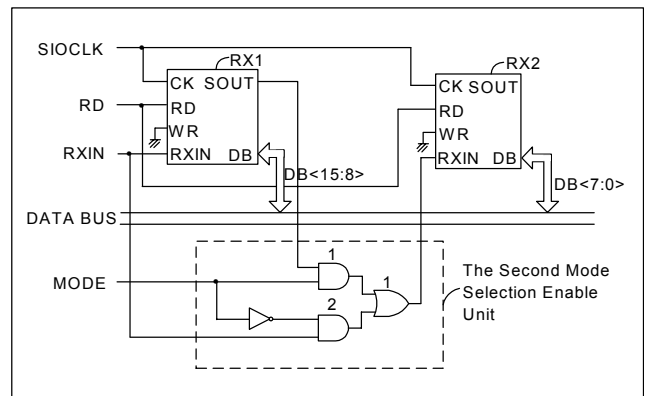


Fig. 4. The block diagram of the receive unit of the proposed serial input/output interface circuit.

proposed SIO. In the 16 bit operating mode, after 16 pulses of the operation clock SIOCLK, both the first and second receive shift registers RX1 and RX2 are filled with the same new serial data. Since the second mode-selection-enable unit transfers the serial output of the first shift register RX1 to the serial input of the second shift register RX2, the serial data filling each register is different. Then, at the end of a predetermined period of time, the first and second shift registers RX1 and RX2 transfer the data stored in parallel to the data bus. In the 8 bit operating mode, the second mode-selection-enable unit transfers the serial data input directly to the serial input of the second shift register RX2. After 8 pulses of the operation clock SIOCLK, the first and second receive shift registers RX1 and RX2 are filled with the same new serial data.

### III. SIMULATION RESULTS

The serial transmit and receive is started by setting start signals TXSet and RXSet to logic level HIGH. After one

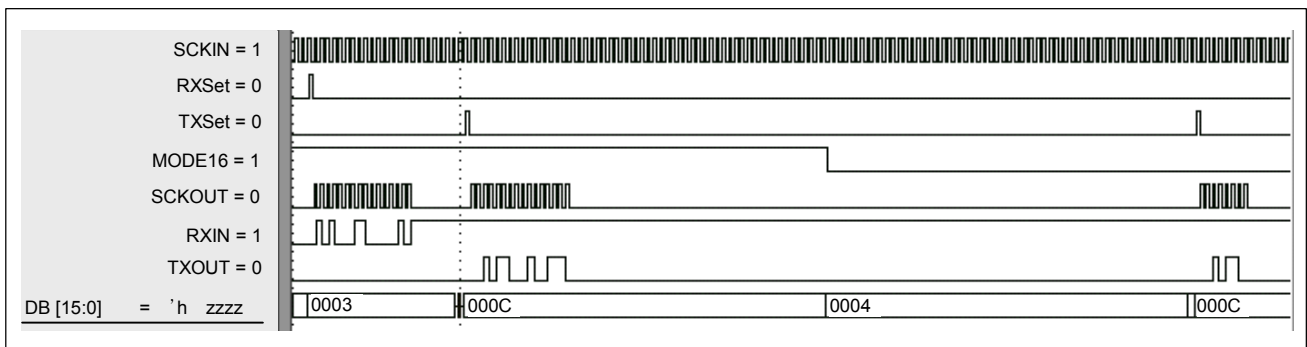


Fig. 5. The Verilog logic simulation results of 8 bit and 16 bit transmit mode operation according to the mode signal.

cycle of the Tx and Rx operation clock SCKOUT, the start signals TXSet and RXSet are cleared automatically to logic level LOW. The serial output data is outputted at the rising edge of the Tx and Rx operation clock SCKOUT and the serial input data is latched at the falling edge of the Tx and Rx operation clock SCKOUT. The first least significant bit (LSB) is sent or received in this SIO. Figure 5 shows the Verilog logic simulation result of the proposed SIO circuit. The MODE16 signal indicates the mode signal. The TXSet signal indicates the start signal for transmit. The RXSet signal indicates the start signal for receive. The operation clock SCKIN signal indicates the input clock source. The Tx and Rx operation clock SCKOUT signal indicates the transmit and receive clock. The TXOUT signal indicates the serial data output. The RXIN signal indicates the serial input data. The DB[15:0] signal indicates parallel data input. When the MODE16 signal is logic level HIGH and TXSet is enable, it indicates operation in a 16 bit transmit mode, and the parallel data 7234h in the data bus converts to the serial data according to 16 pulses SCKOUT. The parallel data is converted to the first LSB at the rising edge of the Tx and Rx operation clock SCKOUT. Thus, the serial data out stream is 0010110001001110. When the MODE16 signal is logic level LOW and TXSet is enable, it indicates operation in an 8 bit transmit mode, and the parallel data 7234h in the data bus converts to the serial data according to 8 pulses the Tx and Rx operation clock SCKOUT. Because of an 8 bit transmit mode operation, the parallel data 34h in the data bus is converted to the first LSB at the rising edge of the Tx and Rx operation clock SCKOUT. Thus, the serial data output stream is 00101100. When the MODE16 signal is logic level HIGH and RXSet is enable, it indicates operation in a 16 bit receive mode, and the serial data stream is 1010001100000101. The serial data streams convert to the parallel data according to 16 pulses the Tx and Rx operation clock SCKOUT. The serial data stream is converted to the first LSB at the falling edge of the Tx and Rx operation clock SCKOUT. Thus, the parallel data is A0C5h.

#### IV. CONCLUSION

The proposed Serial Input/Output interface can operate in either an 8 bit parallel-to-serial and serial-to-parallel conversion mode or a 16 bit parallel-to-serial and serial-to-parallel conversion mode according to the mode signal. We implement the 8/16 bit SIO interface circuit on a single chip with a ternary/tetrad counter and a first/second mode-selection-enable unit. The maximum operation clock is about 70 MHz at a 0.6  $\mu\text{m}$  design rule. Our system improves integration and efficiency by placing the serial interface circuit on a single chip.

#### REFERENCES

- [1] *SH7040 Series Hardware User Manual*, Hitachi, Rev. 2.0 Preliminary, 1996.
- [2] *TP3052, TP3053, TP3054, TP3057, Enhanced Serial Interface CODEC/Filter COMBO Family Datasheet*, National Semiconductor, 1996.
- [3] Seongmo Park, Seongmin Kim, Igkyun Kim, Kyungjin Byun, Jin Jong Cha, and Hanjin Cho, "A Single-Chip Video/Audio Codec for Low Bit Rate Application," *ETRI J.*, vol. 22, no. 1, Mar. 2000, pp. 20-29.
- [4] *IEEE Standard Microcontroller System Serial Control Bus*, IEEE Std. 1118-1990, 1991.
- [5] Jorge A. Polar Seminario and Carlos A. dos Reis Filho, "FPGA Prototype of a Serial Interface Circuit," *Electronics, Circuits and Systems*, vol. 3, 1998, pp. 419-422.
- [6] Charles E. Nunnally and David R. Anderson, "Interrupt Driven Serial Input/Output," *Proc. of Southeastcon*, 1981, pp. 803-805.
- [7] Tae Moon Roh, Dae Woo Lee, Yil Suk Yang, Jin Gun Koo, and Jongdae Kim, "Breakdown Voltage Improvement of p-LDMOSFET with an Uneven Racetrack Source for PDP Driver IC Applications," *ETRI J.*, vol. 24, no. 4, Aug. 2002, pp. 328-331.
- [8] Jongdae Kim, Tae Moon Roh, Sang-Gi Kim, Il-Yong Park, Yil Suk Yang, Dae-Woo Lee, Jin-Gun Koo, Kyoung-Ik Cho, and Young Il Kang, "A Novel Process for Fabricating High Density Trench MOSFETs for DC-DC Converters," *ETRI J.*, vol. 24, no. 5, Oct. 2002, pp. 333-340.