논문 2002-11-5-06

Thermopile sensor with SOI-based floating membrane and its output circuit

Sung Jun Lee[*,**], Yun Hi Lee[*], Sang Hi Suh[**], Tae Yoon Kim[***], Chul Ju Kim[****], and Byeong Kwon Ju[*]**

Abstract

In this study, we fabricated thermopile infrared sensor with floating membrane structure. Floating membrane was formed by SOI(Silicon On Insulator) structure. In SOI structure, silicon dioxide layer between top silicon layer and bottom silicon substrate was etched by HF solution, then membrane was floated over substrate. After membrane was floated, thermopile pattern was formed on membrane. By insertion of SOI technology, we could obtain thermal isolation structure easily and passivation process for sensor pattern protection was not required during fabrication process. Then, the amplifier circuit for thermopile sensor was fabricated by using 1.5㎛ CMOS process. The voltage gain of fabricated amplifier was about two hundred.

Key words : *SOI, thermopile, floating membrane, amplifier*

1. Membrane formation using SOI(Silicon On Insulator) structure

In fabrication of thermal sensor like thermopile sensor, for reducing thermal loss of sensing part, the method which fabricate thin membrane with substrate under sensing part is the most frequently used[1-2]. The representative example is the formation of the insulator membrane structures like $Si_3N_4/SiO_2/Si_3N_4$(NON) or $SiO_2/Si_3N_4/SiO_2$(ONO) sandwich layer. But, in order to make this membrane structure, after sensor patterns are formed on substrate, finally, back-side or front-side of substrate must be etched for a long time and then, it is not easy to solve passivation problem for protecting sensor patterns already formed on substrate.

In this study, we proposed the novel membrane structure instead of general thermal isolation structures such as NON or ONO by etching of silicon wafer. Proposed method for membrane formation is to use SOI(Silicon On Insulator) structure. Figure 1 shows the fabrication process of floating membrane using SOI structure. SOI structure with 15㎛-thick upper silicon is formed through bonding of bare silicon wafer and silicon wafer with 1㎛-thick silicon dioxide and reducing of silicon thickness. Chromium layer for etch mask is deposited on upper silicon and patterning for definition of membrane structure and dry etching of chromium were executed. By dry etching of upper silicon with chromium etch mask, the shape of floating membrane is made and membrane is floated by wet etching of buried oxide with HF solution between two silicon layers. Chromium layer deposited for etch mask is removed by HF solution in the wet etching process and finally, only silicon

* Display and Nano devices Lab., KIST.
** Electronic Material and Device Research Center, KIST.
*** Thermometrics Technology Ltd.
**** School of Electrical Engineering, University of Seoul
<접수일자 : 2002년 5월 31일>

membrane remains. Figure 2 shows the photographs of floating membrane observed by optical microscope and SEM(Scanning Electron Microscope).

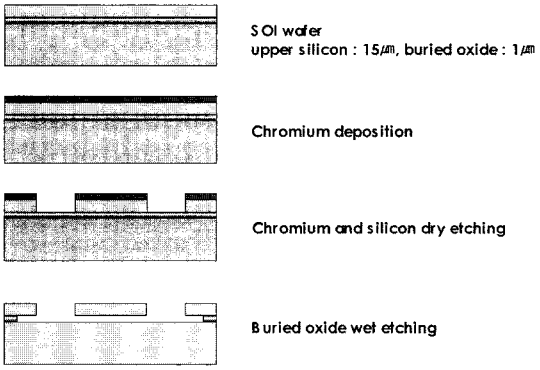
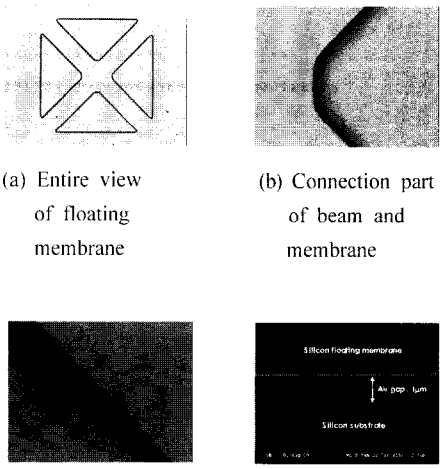


Fig. 1. Fabrication process of floating membrane using SOI structure.



(a) Entire view of floating membrane

(b) Connection part of beam and membrane

(c) Side view of beam

(d) Cross sectional view of floating membrane

Fig. 2. Floating membrane fabricated by SOI structure.

2. Fabrication of thermopile infrared sensor on SOI-based floating membrane structure

We formed thermopile pattern on floating membrane structure fabricated by SOI structure. The fabrication process and process conditions of thermopile sensor formed on SOI-based membrane structure are presented in figure 3 and table 1.

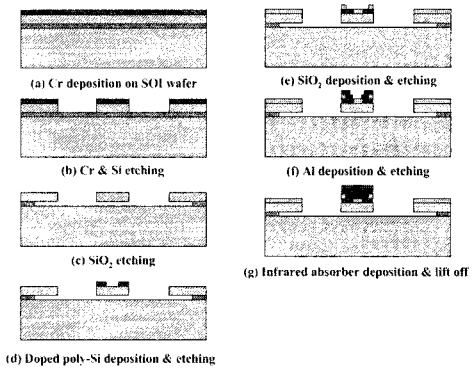


Fig. 3. Fabrication process of thermopile sensor with SOI-based floating membrane structure.

First, 3000Å-thick chromium layer for etch mask of silicon was deposited on SOI structure with upper silicon of 15㎛ and buried oxide of 1㎛. For pattern formation of floating membrane and supporting beam, first mask process was achieved and after chromium etching, silicon was dry etched by RIE. To float defined membrane structure, we removed buried oxide under silicon with HF solution. And, 1500Å-thick thermal oxide was grown on silicon membrane for electrical and thermal isolation with other films.

$$\Delta V = (\alpha_1 - \alpha_2) N \Delta T \qquad (1)$$

(where α_1, α_2 : Seebeck coefficient of two thermocouple materials, N : the number of thermocouple pair, ΔT : the temperature difference between two junctions of thermopile)

As shown in equation 1, output voltage of thermopile sensor is largely influenced by the difference of Seebeck coefficient of two thermocouple materials. So, materials such as Bi-Sb[3], chromel-alumel[4] and copper-constantan, with large difference of Seebeck coefficient between two materials, were largely applied as thermocouple material, but, as the compatibility problem with semiconductor process had occurred, semiconductor materials were

developed and therefore, we selected doped polycrystalline silicon and aluminum as thermocouple material in this fabrication.

Table 1. Fabrication process condition of thermopile infrared sensor with SOI-based floating membrane.

	Process	Condition
1	Cr deposition	Thickness : 3000Å
2	1st mask process & Cr etching	Wet etching : Cr 7 etchant
3	Si etching	RIE : 150W, SF_6 = 10sccm
4	SiO_2 etching	Wet process : HF solution
5	Thermal oxidation	Furnace(dry oxidation) : 1100℃, 50min.
6	Poly-Si deposition & $POCl_3$ doping	Poly-Si thickness : 3500Å Annealing : 850℃, 20min.
7	2nd mask process & poly-Si etching	RIE : 150W, SF_6 = 10sccm
8	SiO_2 deposition	Thickness : 5000~6000Å
9	3rd mask process & SiO_2 etching	Wet etching : BOE -> 6min.
10	Al deposition	thickness : 1500~2000Å ->Thermal evaporator
11	4th mask process & Al etching	H_3PO_4 : HNO_3 : CH_3COOH : D.I.Water = 16 : 1 : 1 : 2 (boiled at 40℃)
12	5th mask process & infrared absorber deposition	Cr oxide absorber sputtering -> 80W, Ar : N_2 = 30sccm : 15sccm, room temperature
13	Lift off	PR remover

Polycrystalline silicon was deposited on membrane and first thermocouple pattern was formed by diffusion of phosphorus impurity and mask process. For electrical isolation between two thermocouple materials and formation of contact hole, sputter oxide of 5000Å was deposited and third mask process was executed. Aluminum, which is both second thermocouple material and electrode pad, was deposited with thickness of 2000Å by thermal evaporator and fourth mask process was proceeded. After junction between n type doped polycrystalline silicon and aluminum is formed, annealing process for ohmic contact was performed at nitrogen ambient of 500℃ during 30min. and we could obtain total resistance of 140 kΩ from thermopile. By the final mask process, the sputtering of chromium oxide at low vacuum and lift-off process, infrared absorption part was completed. Figure 4 shows the features of realized thermopile infrared sensor.

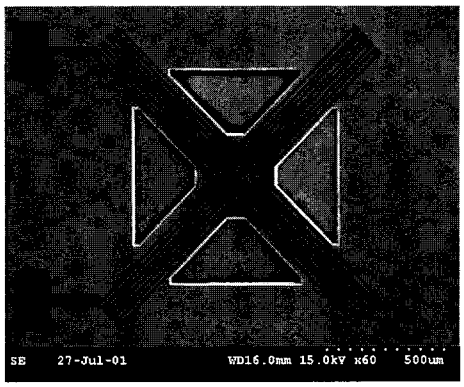


Fig. 4. SEM view of thermopile sensor formed on floating membrane using SOI structure.

When the infrared generated from black body source of 70℃(343K) was irradiated into thermopile sensor on SOI structure, compared with reference voltage in the room temperature, ΔV value of 0.043V was produced.

In fabrication process of thermopile sensor, after fabrication of floating membrane, thermopile pattern was formed on that, consequently, beam and membrane should have been located in upper position more than 15㎛ from substrate. During coating process of photo resist for mask process, this structure cause photo resist to be non-uniformly coated in edge of beam, therefore, thermopile pattern was influenced by etchant permeated into uncoated part of photo resist. Special problems in process were not appeared except for this phenomenon and it is thought that the damage problem of thermopile pattern by non-uniform

coating of photo resist will be solved by extension of beam width.

Through the fabrication of membrane structure by SOI structure and formation of thermopile pattern on membrane structure, we could fabricate thermopile sensor without passivation process[5] and it is expected that if the oxide thickness in SOI structure are increased, responsivity deterioration by thermal loss will be better improved.

3. Design and fabrication of amplifier circuit for thermopile sensor using CMOS process

Because the thermopile sensor generates output signal as voltage by Seebeck effect, it has advantage that the implementation of output circuit is simpler than other kinds of thermal sensor. In this study, we studied basic research for implementation of integrated thermopile sensor. The amplifier circuit for output signal processing of thermopile sensor were designed from combination of transistor and capacitor components and it was fabricated by CMOS process and estimated.

Figure 5 is the amplifier circuit for amplification of output signal generated from thermopile sensor. Figure 6 is the simulation result by parameters extracted from HSPICE after completion of amplifier layout. Because this amplifier circuit was fabricated by CMOS MPC(Multi Project Chip) process carried out in ISRC(Inter-university Semiconductor Researcher Center), we determined the gate width and length(W/L) of each transistor suitable for minimum line width(1.5㎛) of MPC process.

From the simulation result of figure 6, we knew that output characteristic has almost linear tendency to input and the voltage gain of output signal is about more than one thousand. Therefore, it is expected that this circuit will play a adequate role as amplifier for voltage amplification before transmission of output signal generated from thermopile sensor into next processing part.

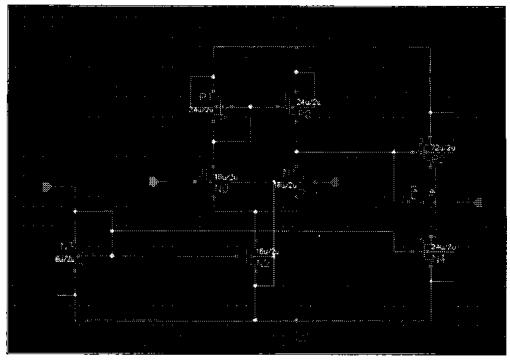


Fig. 5. Schematic diagram of amplifier circuit for output amplification of thermopile sensor.

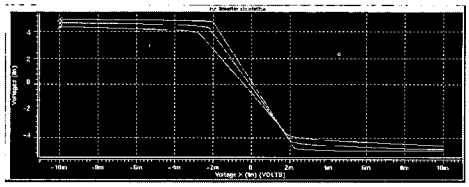


Fig. 6. HSPICE simulation result of amplifier circuit by completed layout.

Figure 7 is the package photograph of amplifier chip fabricated by CMOS process. Also, the photograph of figure 8 shows the structure of fabricated amplifier. The CMOS MPC process performed in the ISRC have the minimum line width of 1.5㎛ and the total number of mask used in process was eleven. The mask sequence was presented in figure 9.

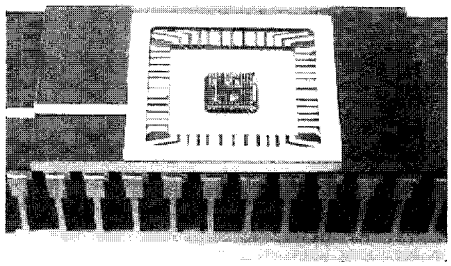


Fig. 7. Amplifier chip fabricated by 1.5㎛ CMOS process.

To measure the output characteristic on amplifier shown in figure 8, we composed of measurement system using oscilloscope, power supply, bread

board and function generator. The feature of measurement system is the same as figure 10. DC voltage came out from power supply was put into the V_{DD} of amplifier circuit and the output voltage was observed by oscilloscope when the DC voltage was took into the input part of amplifier.

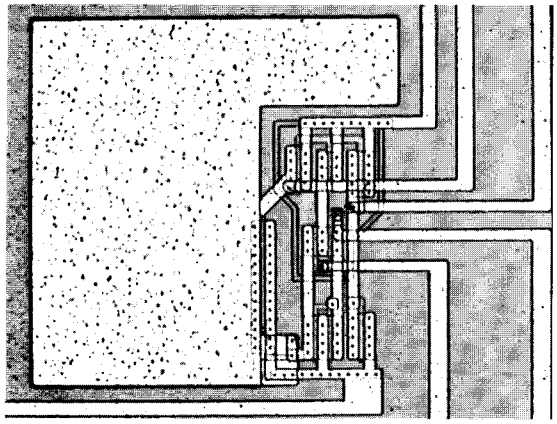


Fig. 8. Optical photograph of fabricated amplifier.

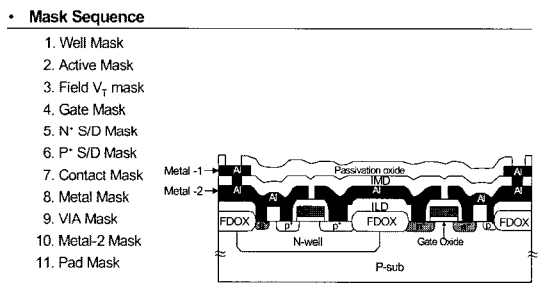


Fig. 9. Mask sequence of ISRC 1.5㎛ CMOS MPC process.

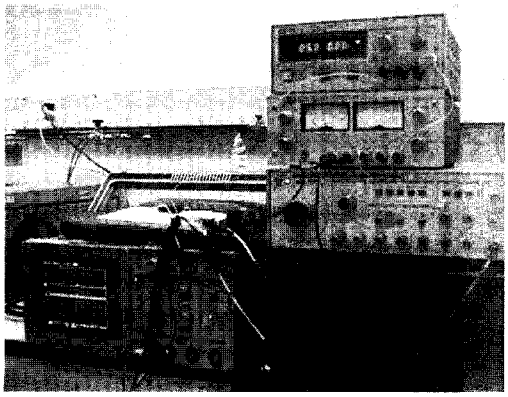


Fig. 10. Measurement system for output observation of fabricated circuit.

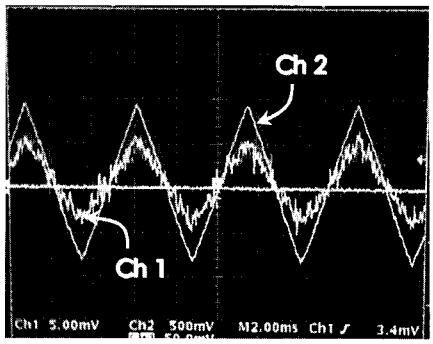


Fig. 11. Output characteristic of amplifier. (Ch 1 : input, Ch 2 : output)

From observation result of figure 11 using oscilloscope, we could know the amplification property of amplifier circuit and its voltage gain was about two hundred, which is smaller than simulation result.

From now on, for amplification of DC voltage signal came out from thermopile infrared sensor, first, we confirmed the linear amplification property of amplifier using HSPICE simulation and determined W/L parameter on each MOS transistor device of amplifier circuit. And, through Cadence tool, we completed the layout of amplifier with minimum line width of 1.5㎛ and finally, fabricated the amplifier by CMOS process. It is thought that this circuit is applicable to the stable amplification of output signal of thermopile sensor.

4. Conclusions

For fabrication of thermal sensor, generally, after sensor patterns are formed on substrate, thermal isolation structures such as cantilever, membrane are fabricated. But, passivation process for protection of sensor pattern must be performed and other problems accompanying passivation are occurred. Therefore, in this study, we introduced the novel membrane formation technology using SOI structure. As the membrane structure is fabricated and then, thermopile patterns are formed on that, the passivation process for protection of sensor pattern was not required any more. It is expected that we

will be able to reduce the thermal loss into substrate through the thickness change of membrane and buried oxide.

Finally, we designed amplifier for output circuit of thermopile infrared sensor and fabricated them using 1.5㎛ CMOS process. The voltage gain of fabricated amplifier was shown about two hundred. It was thought that this difference of simulation and measurement result was caused by error between capacitor parameter used in simulation and real capacitor value in fabricated device.

References

[1] H. Baltes, O. Paul, Sensors Mater.8(6), pp. 409-421, 1996.

[2] M. Muller, W. Budde, R. Gottfried, A. Hubel, R. Jahne, H. Kuck, Sensors & Actuators A, Vol. 54, pp. 601-605, 1996.

[3] F. Volklein, A. Wiegand and V. Baier, "High Sensitivity Radiation Thermopiles made of Bi-Sb-Te Films", Sensors & Actuators A, Vol. 29, pp. 87-91, 1991.

[4] Kwang Sik Oh, Hyun Duk Cho, Jin Sup Kim, Yong Hyun Lee, Jong Hyun Lee, Jung Hee Lee and Se IL Park, "Uncooled Metallic Thin Film Thermopile Infrared Detector", Journal of KITE, Vol. 37, SD, No. 2, pp. 97-104, 2001.

[5] Sung Jun Lee, Byeong Kwon Ju, Yun Hi Lee, Sang Hi Suh, Tae Yoon Kim, Myung Hwan Oh, Chul Ju Kim, "A Study on Fabrication of Thermopile Sensor with Floating Membrane Structure using SOI Wafer", 11th Proceedings of Infrared Image Sensor Conference, pp. 58-64, 2000.

著 者 紹 介

이 성 준(李成俊)
1972년 8월 28일
1995년 서울시립대학교 전자공학과 졸업(학사)
1997년 서울시립대학교 전자공학과 졸업(석사)
2002년 서울시립대학교 전자공학과 졸업(박사)
현재 삼성 전기 중앙연구소/Optical MEMS team
주관심 분야 : MEMS, 센서, 액츄에이터

이 윤 희(李允熙)
1963년 2월 5일
1985년 고려대학교 물리학과(학사)
1987년 고려대학교 물리학과(석사)
1995년 고려대학교 물리학과(박사)
1987년 포항공대 연구원
1988~1994년 한국과학기술연구원 정보전자부 연구원
1994년~2002 한국과학기술연구원 정보재료소자연구센터 책임연구원
현재 고려대학교 물리학과 교수
주관심 분야 : CNT, ELD

김 태 윤(金 泰 潤)
1960년 3월 20일
1984년 한양대학교 무기재료공학과(학사)
1993년 고려대학교 전자공학과(석사)
현재 써모메트릭스 테크놀로지 상무
주관심 분야 : Thermopile sensor

김 철 주 (金 鐵 柱)
1947년 2월 3일생
1973년 한양대학교 공과대학 전기공학과 졸업(공학사)
1981년 일본 Tokai 대학교 졸업(공학석사)
1984년 일본 Tokai 대학교 졸업(공학박사)
현재 서울시립대학교 전자공학과 교수
주관심 분야 : TFT, SOI, MEMS, Ferroelectrics

서 상 희(徐相熙)
1974년 서울대학교 공과대학 금 속공학과 졸업 (학사)
1976년 한국과학기술원 재료공학과 졸업 (석사)
1982년 Northwestern 대학 재료공학과 졸업 (박사)
1984-1985년 Stanford 대학 재료공학과 객원 교수
1976년-현재 한국과학기술연구원 정보 재료·소자 연구센터, 책임연구원
주관심 분야 : 화합물 반도체 성장, 적외선 센서, 패키징

주 병 권 (朱 炳 權)
1962년 12월 2일생
1986년 서울시립대학교 공과대학 전자공학과 졸업(공학사)
1988년 서울시립대학교 공과대학 전자공학과 졸업(공학석사),
1995년 고려대학교 공과대학 전자공학과 졸업 (공학박사)
현재 KIST 정보재료·소자연구센터 선임연구원
주관심 분야 : FED, OELD, CNT, Bonding, Packaging, MEMS