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Improvement of the Contrast Ratio and Reduction of the Reset Period by Current Controlled Ramp Wavefrom

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Abstract

The voltage controlled ramp(VCR) waveform has recently been introduced in the reset period prior to addressing for plasma display. However, this method results in the oscillation of the gap voltage when the ramp rate is increased so as to reduce reset period. In this paper a current controlled ramp(CCR) waveform method in the reset period is suggested. This method can suppress the oscillation of gap voltage under the condition of shorter ramp time. Moreover, the reset time can be reduced by about 30 % compared with the VCR method under the same background luminance.

Keywords : AC PDP, current controlled ramp waveform and reset period

1. Introduction

Plasma display panel(PDP) is a flat panel display which utilizes gas discharge. Fig. 1 shows the principle structure of a discharge cell in an ac PDP. The size of a discharge cell is about 0.3 mm×1 mm×0.15 mm in height. The tri-primary colors(R, G, B) are obtained from R, G and B phosphors excited by vacuum ultra-violet photons emitted from gas discharge. Many efforts have been made to improve the luminance, luminous efficiency and image quality and to realize the low cost of AC PDP in order to compete with other technologies [1-5].

The voltage controlled ramp(VCR) waveform in reset period, as shown in Fig. 2, has recently been used prior to addressing for plasma display. With low ramp rate waveform, VCR scheme allows lower addressing voltage, larger manufacturing tolerance and lower light emission from the reset cycle, which lead to improvement in the dark room contrast ratio[6-9].

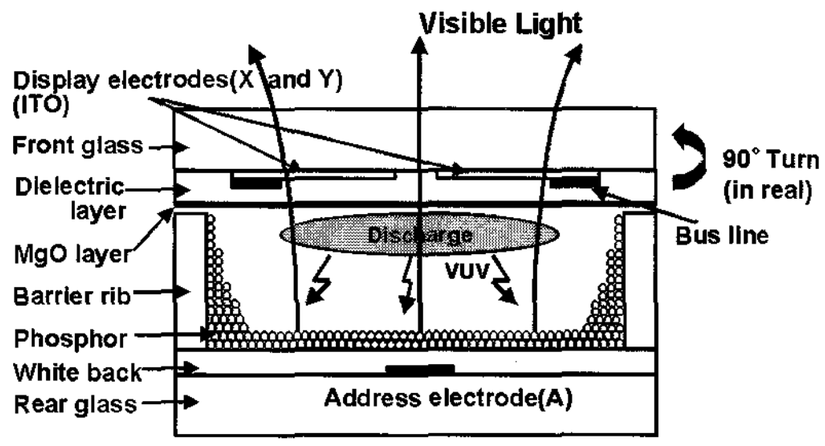

Fig. 1. Principle structure of a discharge cell in AC PDP.

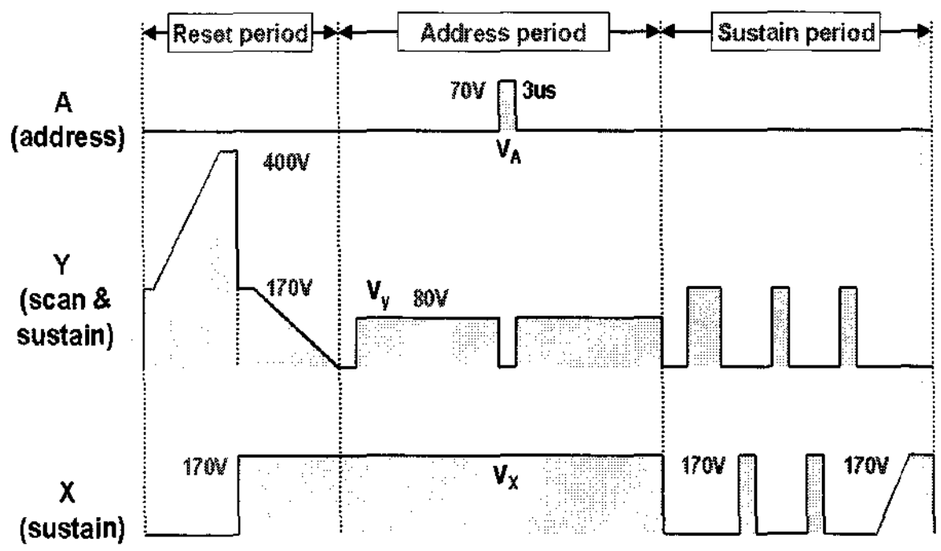

Fig. 2. Schematic diagram of driving waveform.

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Table 1. Specification of 7-in AC PDP.

Front panel		**Rear panel**	
ITO width	380 μm	Address electrode width	80 μm
ITO gap	60 μm	White back thickness	15 μm
Bus width	70 μm	Rib height	130 μm
Dielectric thickness	30 μm	Rib pitch	360 μm
MgO thickness	5000 Å	Rib width	60 μm
Working gas : He+Ne(30 %)+Xe(4 %)		Phosphor thickness	30 μm

Table 2. Specification of the high sensitivity light dececter.

Item	**Specification**	**Unit**
Active area size	1.5Φ	mm
Spectral response range	400-1000	nm
Photo sensitivity	0.5	A/W
Temperature stability of gain	±2.5	%
Gain of APD	30	
Gain of Amplifier	1.0×10^5	V/A
Max. incident photo energy	6.0	μW
Min. detectable limit	0.8	nW

However, the low ramp rate waveform increases the reset period. As a result, the display luminance decreases as sustain period decreases. If high ramp rate is adopted to reduce the reset period, the gap voltage in some wrong discharge cells may show somewhat oscillatory behavior caused by discharge current growth[7]. These oscillations can become unstable and cause highly undesirable addressing failure.

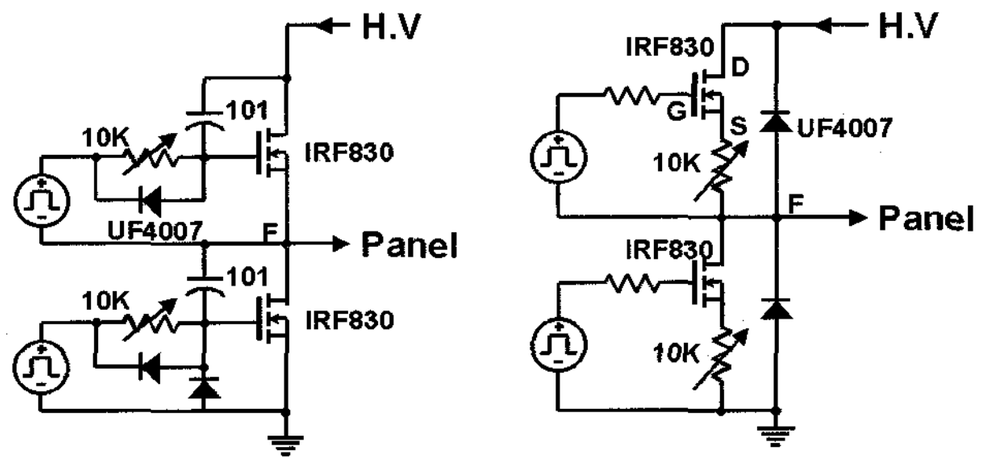
Therefore, in order to improve these problems, we have suggested the current controlled ramp(CCR) waveform which can control the discharge current instead of the voltage controlled ramp(VCR). We, then, investigated the contrast ratio and the discharge characteristics of CCR method compared with VCR method through experiments.

2. Experimental

Table 1 shows the specification of 7-inch test model PDP in this study with VGA resolution. The total number of scan line is 60.

The background and display luminance of the samples is detected by the luminance colorimeter(BM-7, Topcon Co.). In order to accurately detect the emitting light, a highly sensitive light detector is used. The highly sensitive light detector consists of avalanche photo-diode (APD), temperature compensate bias circuit and low noise I-V amplifier circuit. Its specification is shown in Table 2.

Fig. 2 shows the general driving waveforms used in this study. In order to make the same driving conditions as a large AC PDP over diagonal size of 40 inch, the width of scan pulse is designed as 3 μs. The address period is about 1ms and total period is 2 ms. With this waveform, the contrast ratio can be detected as a parameter of ramp up and down time within the range of 20 μs and 150 μs.



(a) (b)

Fig. 3. Schematic diagram of driving circuit for generating ramp voltage waveform. (a) Voltage controlled circuit (b) Current controlled circuit.

The driving circuit has low impedence with about 150 ns pulse rising time during the address and sustain period.

Fig. 3(a) shows the schematic diagram of VCR

generating circuit. The ramp waveform with constant slope can be generated by this circuit. In this case, the slope can be controlled by the variable resistor on n channel FET(IRF830) gate and capacitor between drain and gate.

Fig. 3(b) shows the schematic diagram of CCR generating circuit. The variable resistor is placed between n channel FET(IRF830) source and panel, and it is connected to the floating ground(F) on 12 V voltage source. In order to turn on the FET, about 3~4 V between gate(G) and source(S) is needed. When 12 V is applied between FET gate and source, FET is turned on. However, when the discharge occur in discharge cells the voltage drop occurs both side of variable resistor by the discharge current. In order to make a ramp rate of 2.5 V/μs during the ramp up period, the variable resistance value is needed 1.5 kΩ in 7 inch panel driving. In this case, if the discharge current of 5.3 mA passes through the variable resistor, a voltage drop of 8 V occur of both sides of the variable resistor. Consequently, only 4 V is applied between FET gate(G) and source(S). When 3~4 V is not maintained between n channel FET gate(G) and source(S), the FET is turned off. As a result, the ramp waveform can be generated throuth the current limit process and RC time-constant in the circuit.

3. Results and Discussion

In order to estimate the effect of CCR, PSPICE (Professional Simulation Program with Integrated Circuit Emphasis) simulation study was done for both VCR and CCR methods.

Fig. 4 shows the result of PSPICE simulation for both VCR and CCR method. As shown in Fig. 4(a), the discharge cell of AC PDP was modeled as a well-known positive-resistance discharge cell[10]. For both VCR and CCR method, the sustain voltage is assumed as 180 V and the setup voltage is assumed as 450 V, and also it is assumed that the zenor diode has breakdown voltage of 210 V which is almost the same as the real breakdown voltage of discharge cell.

As shown in Fig. 4(c), it can be observed that the slope of CCR voltage is controlled by limiting the discharge current, automatically. However, in the case of VCR, as shown in Fig. 4(b), the constant voltage slope is maintained regardless of the discharge current, which causes, the discharge current of CCR to be lowered compared with that of VCR method during the reset period. This in turn leads to the decrease in the background luminance.

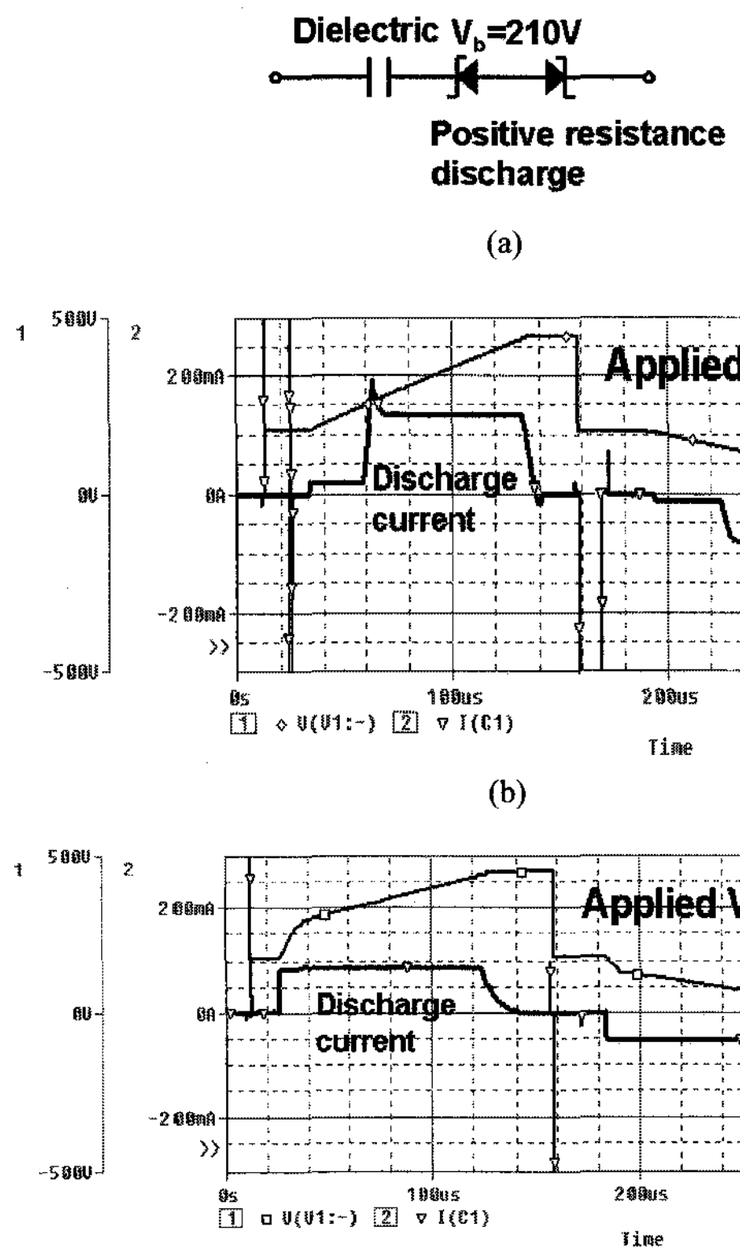


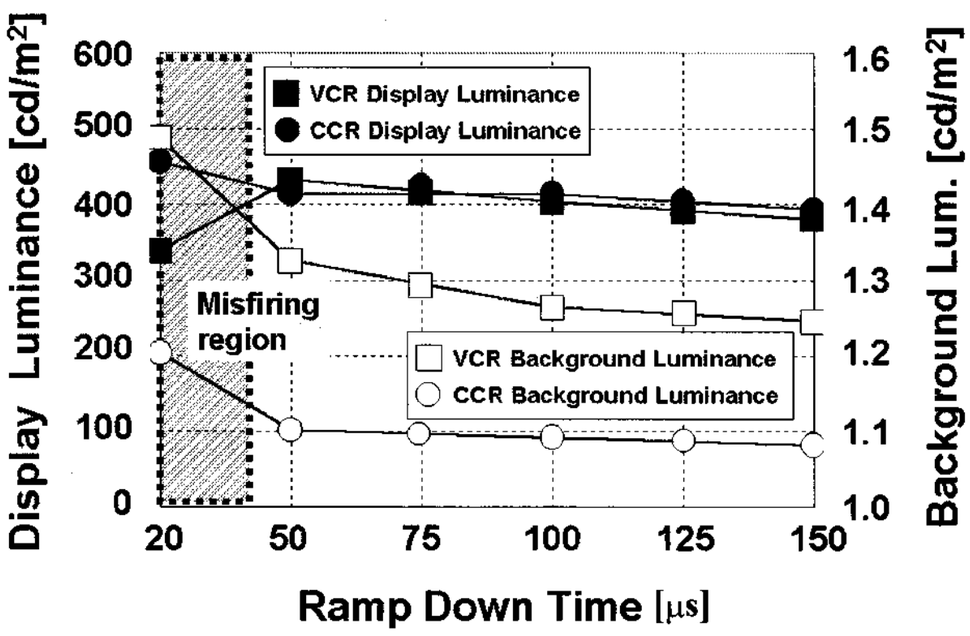
Fig. 4. Results of PSPICE simulation for the reset period of the AC PDP with VCR and CCR method.

Fig. 5 shows the typical experimental results for background and display luminance of both VCR and CCR method versus ramp down time under constant ramp up time of 20 μs and 150 μs with 7 inch model AC PDP.

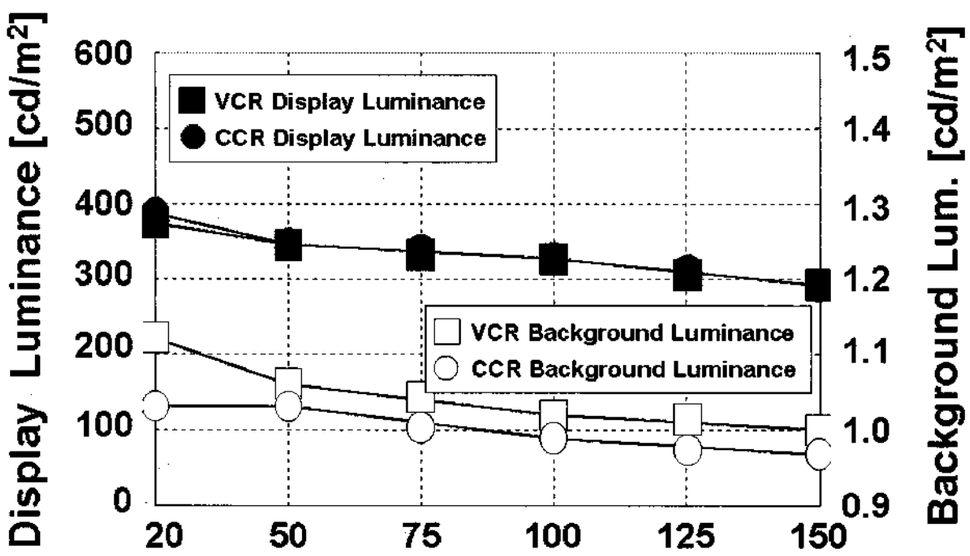
Under the constant ramp up time of 20 μs in Fig. 5(a), the misfiring occurrs in the ramp down time range of 20~40 μs. By increasing the ramp up and down time, the misfiring is no longer observed. According to our experimental results, the stable driving conditions are obtained in the range of 50~150 μs regardless of ramp up and down. These values correspond to ramp up rate of 1.5 V/μs ~5 V/μs and to ramp down rate of 1 V/μs ~4 V/μs. It has been reported that if the ramp rate is lower than 10 V/μm, the stable driving is possible[8].

As shown in Fig. 5, the background luminances

increase with decreasing ramp up and down time for both types. However, the background luminance of CCR method is lower than that of VCR within the experimental range. Especially, when the ramp up/down time is 20 μs /20 μs in VCR case, the oscillatory behavior of gap voltage generated by discharge current growth causes high background luminance, misfiring and low display luminance due to self-erasing discharge. However, in CCR case, the oscillatory behavior can be reduced by restricting the discharge current growth, so that the background luminance can be decreased compared to that of VCR method. As a result, when the ramp up/down time is 20 μs/20 μs in the case of CCR, there was no misfiring and self-erasing discharge.



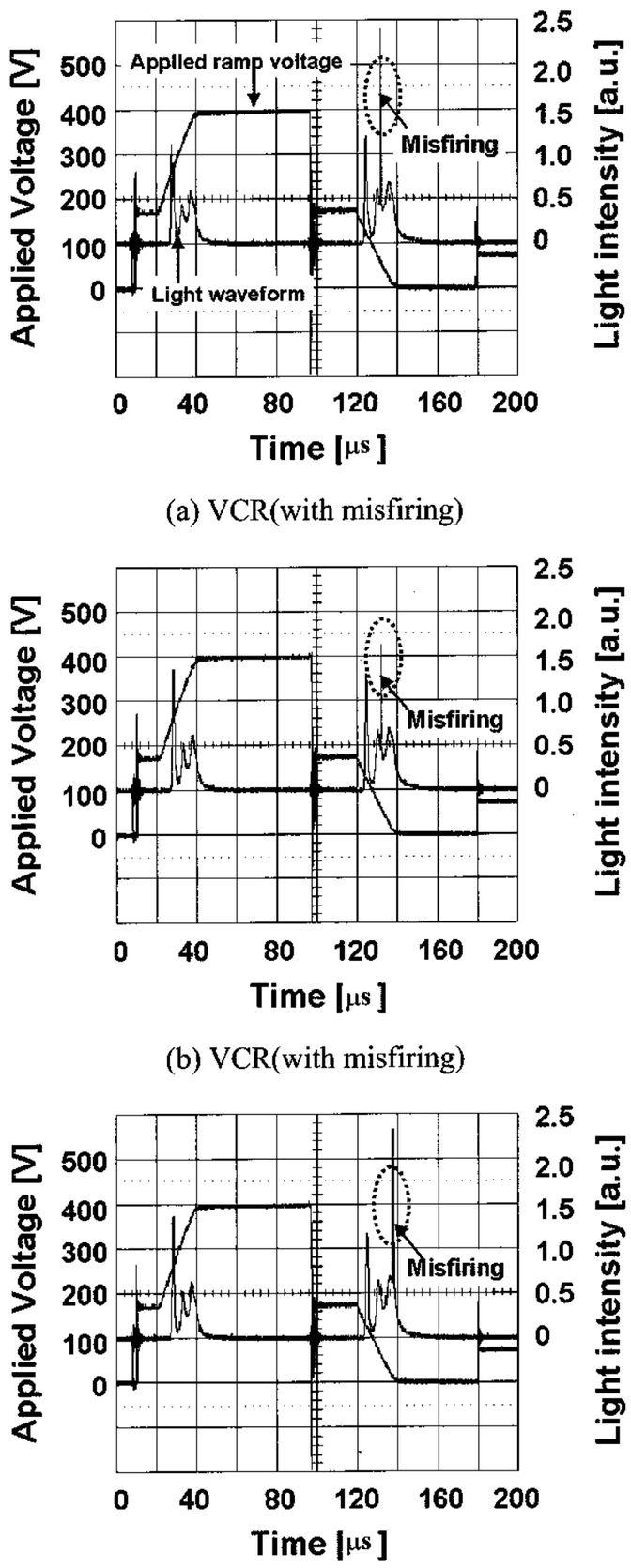
(a)



(b)

Fig. 5. Background and display luminance as parameters of ramp up and down time. (a) constant ramp up time : 20 μs (b) constant ramp up time : 150 μs

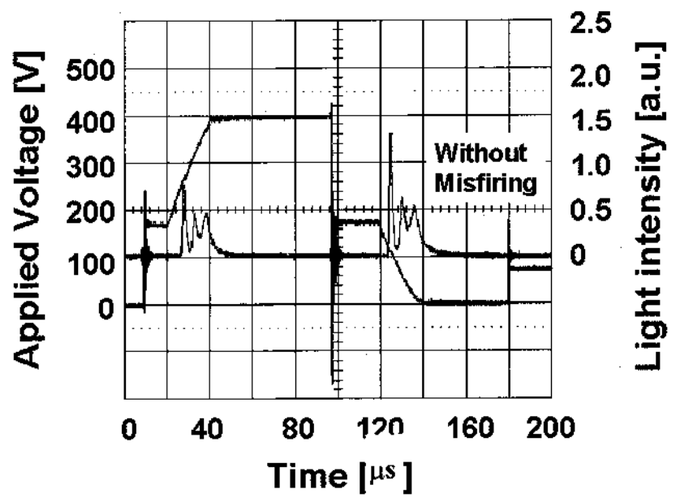
Fig. 6 shows the applied ramp voltage and emitted light waveforms of VCR and CCR during reset period when ramp up/down time is 20 μs/20 μs. In the case of VCR, the unstable light Emissions with the high peak



(a) VCR(with misfiring)

(b) VCR(with misfiring)

(c)VCR(with misfiring)



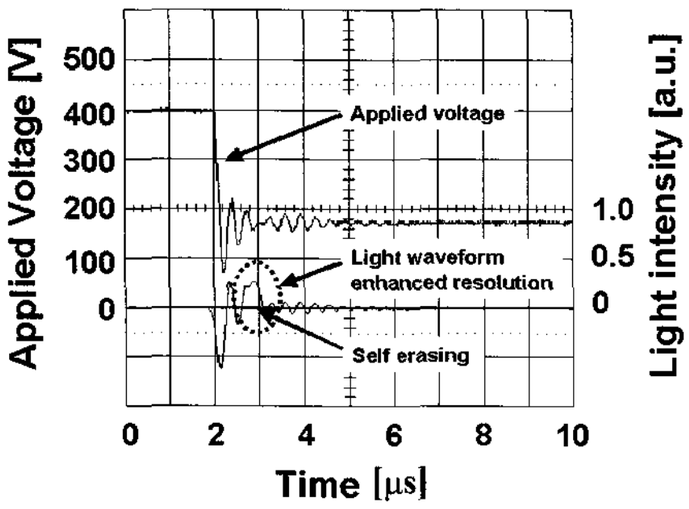
(d)CCR(without misfiring)

Fig. 6. Applied ramp voltage and emitted light waveforms during reset period for VCR and CCR method.

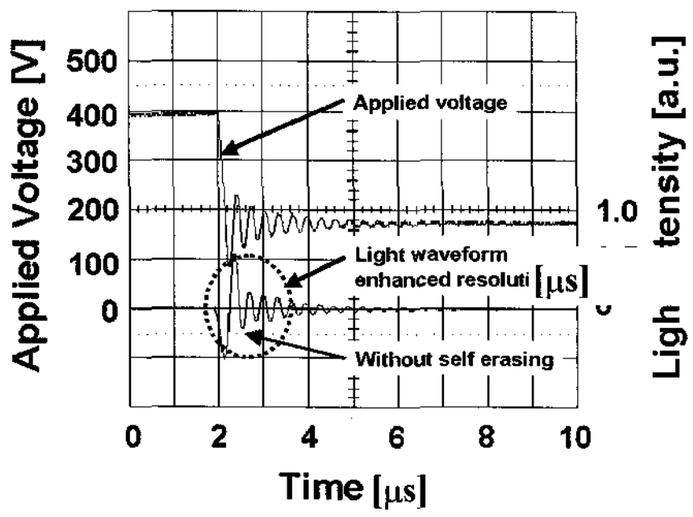
intensity caused by the misfiring are detected in background light waveforms as shown in Figs. 6(a)-(c). However, in the case of CCR the unstable light emission due to the misfiring is not detected as shown in Fig. 6(d).

As previously stated, the reason may be that the cell can not be modeled as a stable positive-resistance

discharge cell under the condition of ramp up/down time of 20 μs/20 μs in case of VCR. Because the shorter the ramp time, the stronger the discharge in the case of VCR. Moreover, since the wall charge increases with the strong discharge during ramp up period, a self-erasing discharge occurs at the beginning of ramp down, which leads to an undesirable addressing failure.



(a) VCR (with self-erasing after ramp up period)



(b) CCR (without self-erasing after ramp up period)

Fig. 7. The self-erasing discharge at the beginning of ramp down from light waveforms for both VCR and CCR cases.

Fig. 7 shows the applied ramp voltage and emitted light waveforms for both VCR and CCR cases at the beginning of ramp down under the condition of ramp up/down time of 20 μs/20 μs. In Fig. 7(b), there is a natural damping caused by switching noise at the beginning of ramp down in the case of CCR. However, in the case of VCR as shown in Fig. 7(a), the discharge current due to self-erasing is added to the natural damping waveform. Therefore, it can be said that the misfiring phenomena occur in the case of VCR, as shown in Figs. 6(a)-(c).

Fig. 8 shows the dynamic reset and sustain voltage margin of VCR and CCR method under the condition of ramp up/down time of 20 μs/20 μs of which the ramp up rate is 11.5 V/μs and ramp down rate is 8.5 V/μs. As shown in this figure, in case of VCR method, it can be noticed that the point of the 400 V reset voltage and 70 sustain voltage is out of stable driving region when the ramp up rate is 11.5 V/μs and ramp down rate is 8.5 V/μs as shown in Fig. 7(a). As a result, it can be said that the misfiring due to the self-erasing discharge occurs. From Fig. 8, it can be noticed that the driving margin of reset and sustain voltage of CCR is wider than the VCR method.

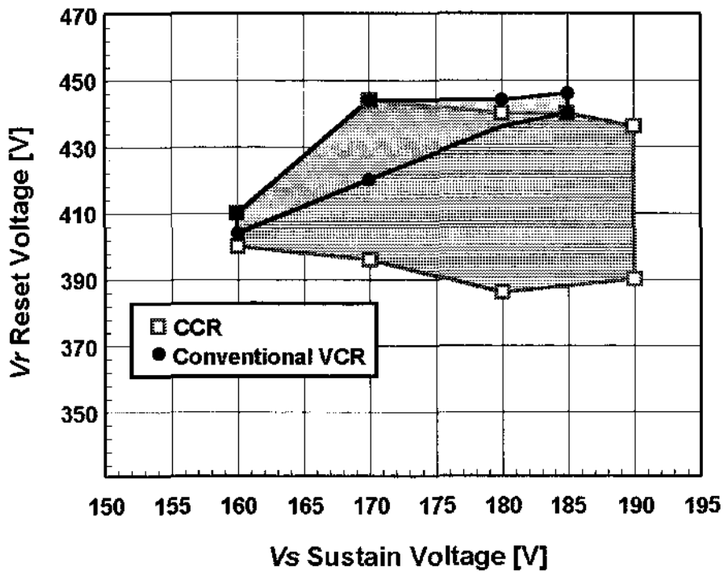


Fig. 8. Dynamic reset and sustain voltage margin (Ramp up rate=11.5 V/us, Ramp down rate=8.5 V/us)

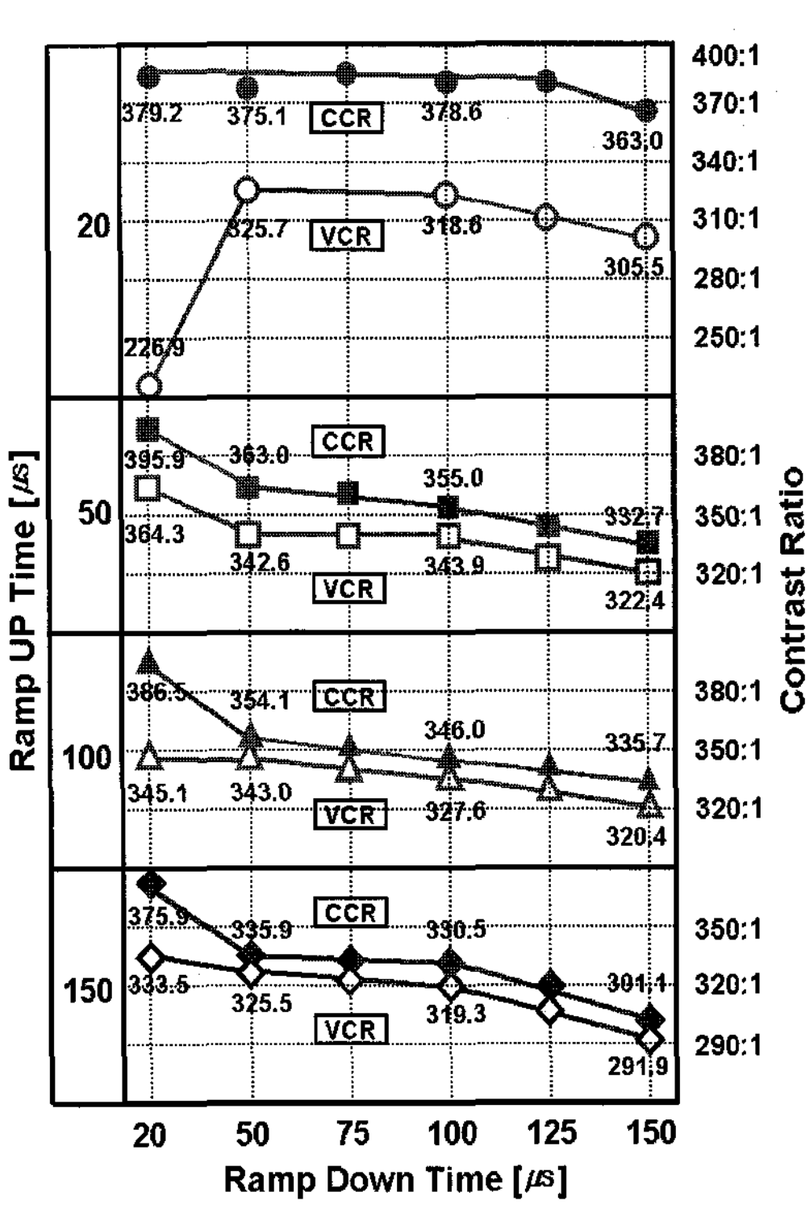
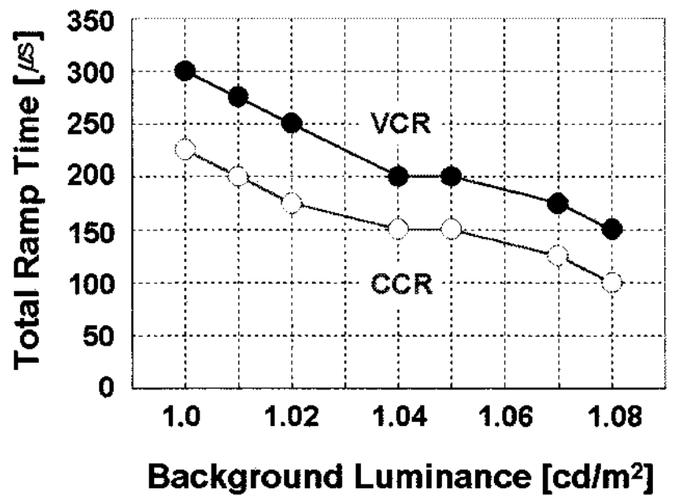


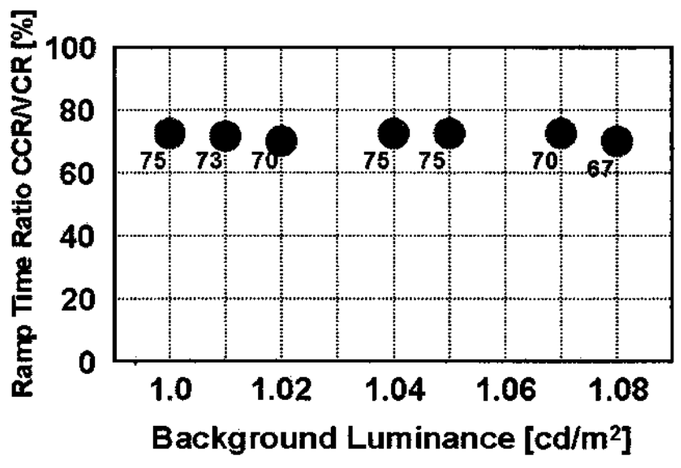
Fig. 9. Contrast ratio as parameters of ramp up and down time.

Fig. 9 shows the contrast ratio versus ramp up and down time plot. Since it is possible to reduce the

background luminance in the case of CCR, the contrast ratio of CCR method is higher than that of VCR method under the same driving condition. Especially, when the ramp up or down time is decreased to 20 μs, the contrast ratio of CCR method is increased by about 12 % relative to VCR without misfiring. When the misfiring was occur under the condition of the ramp up/down time of 20 μs /20 μs, the contrast ratio of CCR method was about 67 % higher than that of the VCR.



(a)



(b)

Fig. 10. Total ramp time (reset time) as parameters of background luminance.

Fig. 10(a) shows the total ramp time(reset time) in the case of CCR and VCR as parameters of background luminance. From this figure, the total ramp time of CCR method is seen to be reduced to about 50~75 μs compared with that of VCR under the same background luminance. That is, the reset period of CCR method is decreased to about 25~33 % compared with VCR method, as shown in Fig. 10(b).

Fig. 11 shows a characteristic of dynamic voltage margin of CCR and VCR. In this case, a reset and scan voltage remain constant as 400 V and 80 V, respectively. As shown in Fig. 11, the voltage margin of CCR is almost same with that of VCR. At the addressing discharge, the charge per single cell in the case of CCR is about 19 [pC], which is almost the the same with VCR regardless of the ramping up and down time. The addressing time[11-13] is also almost the same as about 1.0~1.1 μs for both types. As a result, it can be assumed that the characteristics of the addressing and sustain discharge are almost the same for both types.

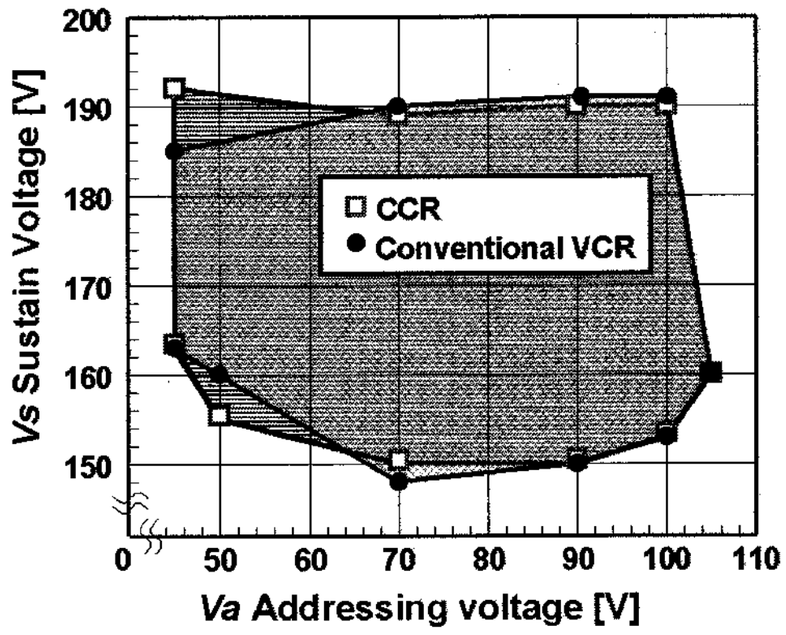


Fig. 11. Dynamic voltage margin.

4. Conclusion

In this paper, the current controlled ramp(CCR) waveform is suggested instead of the conventional voltage controlled ramp(VCR) waveform in reset period of ac PDP. Moreover, the contrast ratio and discharge characteristics for both methods are also investigated.

By the suggested CCR method, the oscillatory behavior of gap voltage which leads to misfiring can be reduced by restricting the discharge current growth in given cells in the case of shorter ramp time, and the contrast ratio characteristics is also improved.

The total ramp time of the suggested CCR method is reduced to about 50~75 μs compared with that of VCR under the condition of the same background luminance when the address period is about 1ms and total period is 2 ms. That is, the reset period of CCR method is reduced to about 25~33 % compared with VCR method under the same background luminance.

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