Adjustable-Performace, Single-Ended Input Double-Balanced Mixer

Jin-Yong Choi, Kyung-Ho Lee, and Sang-Gug Lee

Abstract – **A noble single-ended input, double-balanced mixer topology is proposed. The mixer incorporates the common-source amplifier input stage with inductive degeneration for impedance matching. The analysis based on simulations shows that the overall performance of the mixer is excellent and is adjustable by varying the input transistor size to give best characteristics for the given linearity specifications.**

Index Terms – **RF, Mixer, CMOS, Noise Figure**

I. INTRODUCTION

The superheterodyne receiver has been the most widely used architecture for modern radio communication receivers. A basic function block of the every superheterodyne receiver is the mixer, which converts the RF input signal to the IF. Among the various mixer topologies, the double-balanced mixer topology, which requires a double-ended input, is preferred since it can suppress LO signals at the output. To prevent noise or image signals from degrading the performance, an image-rejection filter is required prior to the mixer. Since such a filter usually requires a termination of single-ended 50 Ω at the input and output, a single-to-double-ended balun is required prior to the mixer. Apart from the extra hardware needed, the balun may degrade mixer performance. Therefore a mixer topology with a single-ended 50 Ω-input termination is very desirable.

A double-balanced mixer with a single-ended 50 Ω input was presented as the MICROMIXER [1], which has excellent linearity characteristics. However its conversion gain and noise characteristics are poor. To improve the noise characteristics of the MICROMIXER, a modified mixer topology was presented [2]. However its conversion gain is not large enough to suppress the noise contributions from the following stages.

In this paper, we propose a new mixer topology, which can optimize the gain and noise performances for the given linearity specification. In section II, we introduce the construction of the new topology following brief explanations about the operations of the previously reported mixers. In section III, we compare the performance of the proposed mixer to those of the previously reported mixers, and discuss about the advantages and disadvantages of the proposed mixer. In section IV, the results are summarized briefly.

II. MIXER TOPOLOGY

A double-balanced mixer with a single-ended 50 Ω input was presented as the MICROMIXER [1]. It is originally a bipolar double-balanced mixer in which the class-A differential pair is replaced by a class-AB buffer. Fig. 1 shows a CMOS-version example of the MICROMIXER. The input buffer is the combination of a common-gate amplifier (M_3) and a current mirror (M_1 and M_2). The M_4 forms a cascode amplifier, and helps to maintain the symmetry and hence to suppress the LO signals to appear at the mixer output. It also helps to suppress the second harmonic of the LO signals to appear at the output due to its inherent large output impedance. The resulting MICROMIXER can have a well-defined input impedance and essentially unlimited input capacity due to the gain expansion available in the

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class-AB operation [3]. The input impedance can be matched to 50 Ω by setting the values of the transconductance (g_m) of M_1 and M_3, and R_1 properly. However the MICROMIXER suffers from the low conversion gain and the resulting poor noise performance due to the required low g_m value of the input transistors (M_1 and M_3) for the impedance matching. The 50 Ω termination restricts the allowed maximum g_m value of M_1 and M_3 below 10 mS when R_1=0 Ω in Fig. 1.

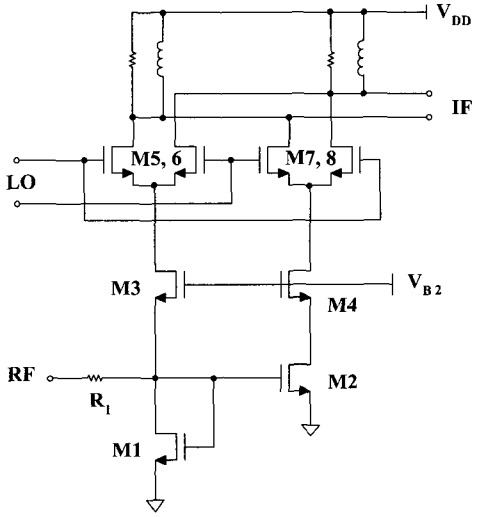

Fig. 1. CMOS-version example of the MICROMIXER.

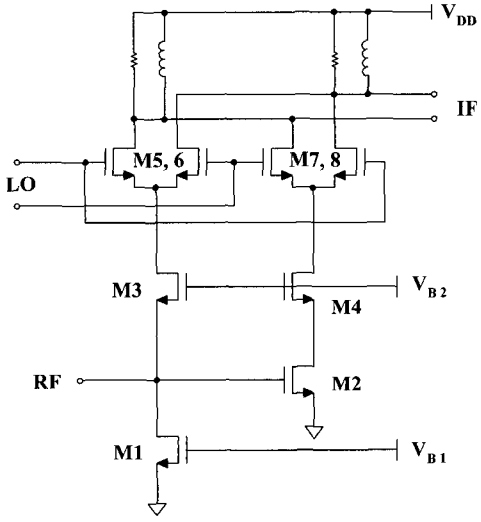

Fig. 2. Modified MICROMIXER [2].

A modified CMOS version of the MICROMIXER was presented to restore the noise performance while degrading the linearity in some extent, which is not problematic when adopting the CMOS technology due to the better linear characteristics of MOS transistors [2]. The proposed topology is shown in Fig. 2, which is modified in this work by adding the M_4 to improve the performance in terms of symmetry and 2LO suppression. The diode-connected M_1 in Fig. 1 is replaced by the current source M_1 in Fig. 2. In this topology the input signal is no longer shunted to ground by M_1 and only the g_m of the M_3 contributes to the input impedance. The resulting g_m can be doubled compared to that of the MICROMIXER with R_1=0 Ω in Fig. 1. The resulting conversion gain is improved due to the increased g_m, and the noise performance is improved because of the increased g_m and the reduced M_1 noise contribution.

The topology in Fig. 2. guarantees better performances in terms of the conversion gain and the noise compared to those of the MICROMIXER. However the g_m of M_3 is still restricted to have a value below 20 mS for 50 Ω impedance matching, and thereby limiting the conversion gain. The resulting system noise performance may not be good enough since the low-gain mixer cannot effectively suppress the noise at switching transistors and the noise generated in the following stages.

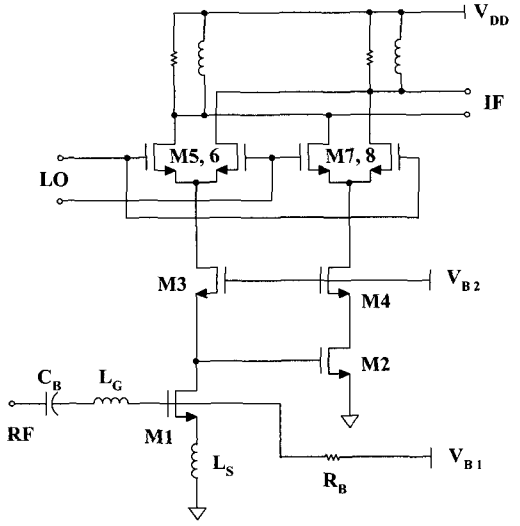

Fig. 3. Proposed mixer.

Fig. 3 shows the proposed mixer topology to improve the conversion gain and the noise performance. The input signal is fed to the common-source amplifier (M_1) with inductive source degeneration for impedance matching. The real part of the input impedance is

determined by L_S, and the combination of L_S and L_G cancels out the imaginary part [4]. C_B is simply a dc block capacitor. The output signal from the M_1 is fed to the common-gate amplifier (M_3) and the cascode amplifier formed by M_2 and M_4. The g_m value of the input transistors is essentially not limited by impedance matching, and hence larger conversion and better noise performance can be achieved.

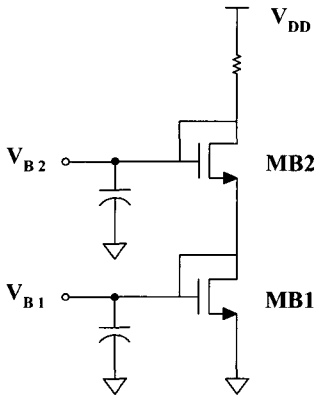

Fig. 4. Proposed bias circuit for the mixer.

Fig. 4 shows the proposed bias circuit for the proposed mixer. The diode-connected M_{B1} in Fig. 4 performs a current-mirror biasing for the input transistor M_1 in Fig. 3. The diode-connected M_{B2} in Fig. 4 guarantees the bias of the transistor M_2 being equal to that of M_1 if the drain and the gate voltages of M_3 in Fig. 3 are set equal. If the voltage headroom is not enough to make the drain and the gate voltage of M_3 being equal, it is suggested to make the dc current values through the transistor M_1 and M_2 as close as possible by choosing the LO dc bias level as its possible highest level to maintain the better symmetry. The bypass capacitors in Fig. 4 help to keep the noise generated in the bias circuit from penetrating into the mixer.

III. MPERFORMANCE EVALUATION

We compare the performances of three types of mixers in Fig. 1-3 with the help of circuit simulations. The previously calibrated bsim3v3 model set based on a standard 0.35 um CMOS technology is used for the transistors, capacitors, and the bond pads.

The assumed RF and IF frequencies are 2.4 GHz and 200 MHz, respectively. The supply voltage is assumed to be 3 V. The widths of transistors M_1-M_8 for all the mixers are chosen as 150 μm. The bias circuit of Fig. 4 is commonly applied for all the mixers, and the bias currents through M_1 and M_2 are set as 1.15 mA for 50 Ω input impedance matching of the mixer in Fig. 2. For the mixer in Fig. 1, the 15 Ω series resistor R_1 is added for the 50 Ω impedance matching. For the proposed mixer in Fig. 3, the source degeneration inductor L_S and the series inductor L_G are chosen as 1 nH and 13.3 nH, respectively for 50 Ω impedance matching. The mixer load is commonly composed of an ideal resistor and inductor combination, and is broadly matched to the differential resistive output port, just for comparison purpose.

In Fig. 1 and 2, the ground nodes are connected together to a ground pad, which is assumed to be connected to outside through a bond wire. In Fig. 3, the source node of M_2 is assumed to be connected to a separate ground pad.

Table 1. Performance comparison between the mixers.

Specifications	Micro-mixer	Modified Micromixer	Proposed Mixer (Version 1)
Conversion gain [dB]	-7.54	-3.07	5.18
Noise Figure [dB]	15.15	11.28	7.05
Input P_{1dB} [dBm]	8.55	0.74	-18.28
Output P_{1dB} [dBm]	-1.75	-3.34	-14.10
Input IP3 [dBm]	6.86	5.87	-10.29
Output IP3 [dBm]	-0.96	2.80	-5.12

Table 1 summarizes the simulated characteristics of the mixers. As shown in Table 1, compared to the MICRMIXER in Fig 1, the modified mixer in Fig. 2 shows improved performances in terms of conversion gain and noise, but somewhat worsened linearity performance as expected.

The proposed mixer (version 1) in Table 1 shows a lot improved performances in terms of conversion gain and noise. However the linearity degradation is very severe. It was confirmed that the severe linearity degradation is caused by the inherent voltage amplification between the input node and the gate node of the transistor M_1 at the matched condition. In Fig. 3, the amplification factor is

equal to the quality factor Q_{in}, which is expressed as

$$Q_{in} = \frac{1}{\omega_0 C_{gs}(R_S + \omega_T L_S)} \quad (1)$$

where R_S is the input source resistance, C_{gs} is the gate-to-source capacitance of the input transistor M_1, ω_0 and ω_T are the RF operating frequency and the transistor cutoff frequency, respectively [4].

From the equation (1), it is clear that Q_{in} can be quite large if the C_{gs} value is small. For the proposed mixer (version 1) in Table 1, we use only 150 um-wide transistors and hence the voltage amplification is large, resulting the poor linearity at the chosen RF frequency. From the equation (1), we can expect that Q_{in} can be reduced by choosing larger transistors to increase C_{gs}. With larger transistors, the voltage amplification at the input will be reduced to improve the linearity. The reduced voltage amplification will decrease the overall conversion gain, but the increased transistor g_m will compensate the gain decrease in some extent. With this conclusion, we performed more simulations on the proposed mixer with increased transistor width (version 2 and 3) without changing any other parameters. The bias currents of input transistors are also fixed at their previous values. The results are summarized in Table 2.

Table 2. Performance comparison of the proposed mixers with different transistor sizes.

Parameters \ Version no.	1	2	3
Transistor width [μm] (M_1-M_4)	150	300	400
Conversion gain [dB]	5.18	1.68	-0.67
Noise Figure [dB]	7.05	9.03	10.61
Input P_{1dB} [dBm]	-18.28	-3.83	3.60
Output P_{1dB} [dBm]	-14.10	-3.16	1.91
Input IP3 [dBm]	-10.29	-7.96	-6.96
Output IP3 [dBm]	-5.12	-6.30	-7.63

The results in Table 2 clearly show that the gain and noise performance degrades but the linearity improves as the width of the input transistors increases, as expected. There is a tradeoff among the conversion gain, noise, and linearity. The characteristics are adjustable by varying the input transistor size once the linearity specifications are given.

In the proposed mixer in Table 2, the P_{1dB} point can be improved as wanted by increasing the transistor width, but the third intercept point (IP3) value is somewhat limited. This can be improved by increasing the bias current of the input transistors [5]. We now present the simulation results of the proposed mixer with increased bias current. However, the expected improvement in performance can also appear in the other two mixers in Fig. 1 and 2 as well. Therefore we compare the performances of all the mixers at the same increased bias level. For all the mixers, the width of the input transistors M_1-M_4 is increased to 400 μm, and the width of the switching transistors M_5-M_8 is increased to 300 μm. The bias currents through M_1 and M_2 are doubled as 2.3 mA. For the MICROMIXER and the modified MICROMIXER, the resulting transistor g_m values are too large for 50 Ω impedance matching. For the MICROMIXER in Fig. 1, the 32 Ω series resistor R_1 is added for the 50 Ω impedance matching. For the modified MICROMIXER in Fig. 2, the 27 Ω series resistor is also added. For the proposed mixer in Fig. 3, the values of the source degeneration inductor L_S and the series inductor L_G are chosen as 1.4 nH and 6.1 nH, respectively, for 50 Ω impedance matching.

Table 3 summarizes the simulated characteristics of the mixers. The proposed mixer (version 4) in Table 3 shows a lot improved performance in terms of conversion gain, noise, and IP3 compared to those of the version 3 mixer in Table 2. Only the P_{1dB} characteristics are worse, but estimated to be quite acceptable for most of the applications.

As shown in Table 3, the conversion gain and the noise characteristics of the resistively matched (R-matched) MICROMIXER and the R-matched modified MICROMIXER are a lot worsened while the linearity is improved. With the series resistive matching in the mixers of Fig. 1 and 2, there exists a voltage attenuation at the input, which degrades the gain and noise characteristics while improving the linearity. Therefore it can be said that there is nothing to get other than unnecessarily high linearity when increasing the transistor g_m in the mixers with resistive matching in Fig. 1 and 2.

Table 3. Performance comparison between the mixers with increased bias current.

Specifications	Micro Mixer R matched	Micro Mixer LC matched	Modified Mixer R Matched	Modified Mixer LC matched	Proposed Mixer (Version 4)
Conversion gain [dB]	-8.61	-4.03	-4.61	-1.13	5.36
Noise Figure [dB]	18.87	14.29	15.89	12.03	8.07
Input P_{1dB} [dBm]	13.98	9.18	7.07	3.60	-7.47
Output P_{1dB} [dBm]	4.36	4.16	1.46	1.46	-3.12
Input IP3 [dBm]	7.79	6.64	9.46	7.62	-2.25
Output IP3 [dBm]	-0.82	2.61	4.85	6.28	3.11

In Table 3, we also include the simulated characteristics of the mixers in Fig. 1 and 2 with reactive (LC) matching for fair comparison. The results show that the gain and noise characteristics improve with reactive matching, but the linearity degrades compared to those of the R-matched mixers. This is caused by the elimination of the voltage attenuation at the mixer internal input nodes. However the gain and noise characteristics are still far worse than those of the proposed mixer (version 4).

From the equation (1), we can expect that the voltage amplification at the input can be quite large at lower RF frequencies, which indicates that the proposed mixer topology is required to use very large-size input transistors in this case. Possible disadvantage with the large-size transistors resides in the sensitivity of the mixer to the variation of the transistor threshold voltage. Therefore the proposed mixer can be said more suitable for high frequency applications.

IV. Conclusions

We proposed a noble single-ended input, double-balanced mixer topology, and compared its performance to those of the two previously presented mixers. The analysis based on simulations showed that the overall performance of the proposed mixer is excellent and the performance can be adjustable by varying the input transistor size to give best characteristics in terms of conversion gain and noise for the given linearity specification.

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