Antifuse Circuits and Their Applicatoins to Post-Package of DRAMs

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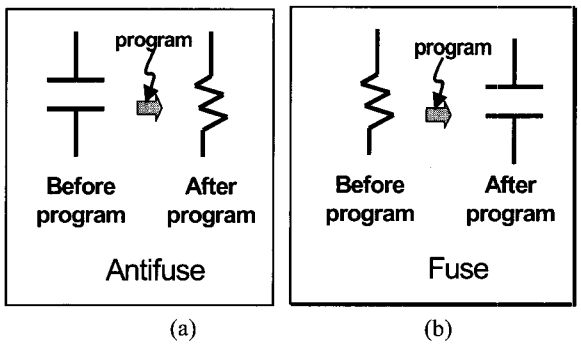
Abstract − **Several methods for improving device yields and characteristics have been studied by IC manufacturers, as the options for programming components become diversified through the introduction of novel processes. Especially, the sequential repair steps on wafer level and package level are essentially required in DRAMs to improve the yield. Several repair methods for DRAMs are reviewed in this paper. They include the optical methods (laser-fuse, laser-antifuse) and the electrical methods (electrical-fuse, ONO-antifuse). Theses methods can also be categorized into the wafer-level(on wafer) and the package-level(post-package) repair methods. Although the wafer-level laser-fuse repair method is the most widely used up to now, the package-level antifuse repair method is becoming an essential auxiliary technique for its advantage in terms of cost and design efficiency. The advantages of the package-level antifuse method are discussed in this paper with the measured data of manufactured devices. With devices based on several processes, it was verified that the antifuse repair method can improve the net yield by more than 2%~3%. Finally, as an illustration of the usefulness of the package-level antifuse repair method, the repair method was applied to the replica delay circuit of DLL to get the decrease of clock skew from 55ps to 9ps.**

Index Terms − **High K gate dielectric, Metal gate, CMOS Fabrication process.**

I. INTRODUCTION

As the DRAM technology is scaled down, DRAM cells become electrically susceptible to electrical, thermal, and mechanical stresses. Compared to typical CMOS digital systems, operations of DRAM are more complicated requiring several trimming and repair techniques. As a result, these techniques are becoming more of an issue for bringing the yield-up in DRAM technologies. The most common DRAM programming (repair) techniques can be categorized into the optical programming method using laser fuse or laser antifuse[1-3] and the electrical programming method using electrical fuse or ONO antifuse[4-7]. Tuning and option techniques for complex operations and functional convergences for various systems' needs have also been developed [8-9]. Fig. 1 shows a simplified view of the electrical state changes of fuse and antifuse programming. In case of fuse, the state changes from resistor to capacitor by programming. The inverse means the programmed state for the antifuse.



(a) (b)

Fig. 1. Concepts of electrical state changes by programming on antifuse and fuse.

Several types of fuse and antifuse components are

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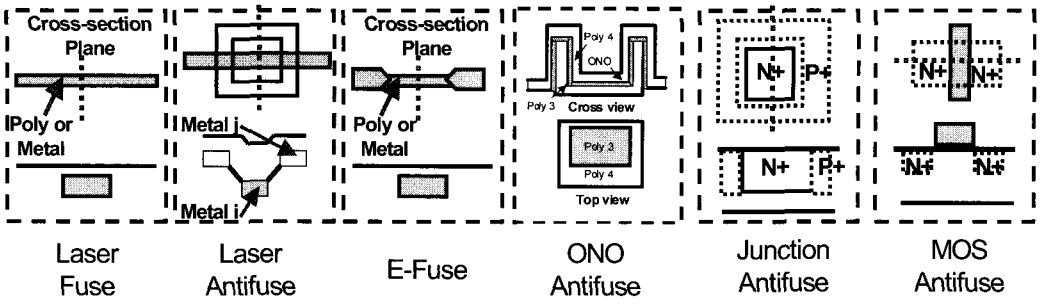


Fig. 2. Several types of antifuse and fuse components.

commercially used as shown in Fig. 2. The selection of using fuse or antifuse depends on the design needs, the process compatibility, and the production cost. One of the simplest methods for nonvolatile programming as shown in Fig. 2.(a) is to optically cut polysilicon (or metal) fuse links by using a high-energy laser [1,2]. Another method by using a laser is to form a vertical metallic link of two interlayer metals [3]. The first method(laser fuse method) has been the most widely used nowadays for nonvolatile programming of DRAM repair circuitry. The second method(laser-formed antifuse method) was developed to replace the bonding options by vertically connecting two horizontally crossing metals in the VLSI circuits. These optical methods are relatively simple, although they are limited to programming only on wafer level, before packaging.

Direct electrical programming of antifuse and E(electrical)-fuse structures with high external voltages have also been utilized, but is conventionally limited to wafer level repair due to the incompatibility of high voltage I/O pins with the standard DRAM package configurations [5-6,20]. Recently, the package-level programming techniques were proposed with E-fuse and antifuse [7,11-15]. The post-package antifuse EPROM repair methods were reported to improve yield significantly [11-13]. For this, an internal high voltage charge pump or negative voltage charge pump and a programming circuitry was integrated inside a DRAM chip to repair defective DRAM cells after burn-in test of the packaged DRAM chips. The antifuse component can be devised using different structures depending on process as shown in Fig. 2 (d) to (f). In most cases the ONO antifuse was typically used in DRAM process however, the MOS antifuse or the junction antifuse is expected to be used in the next generation without an ONO (Oxide-Nitride-Oxide) capacitor.

Another method using the stacked-flash transistor fuses was proposed as a multi-programming scheme for post-package, which had good programming characteristics such as the relative lower programming voltage and the program repeatability. However, it requires more complicated process that is less cost efficient than the conventional repair methods [7].

In this paper the discussion is going to be focused on the antifuse programming techniques and their applications for the post-package repair. This capability is expected to become more cost efficient with increasing memory density and especially for advanced chip scale packaging technologies, which typically involve the failure-prone module assembly and the pre-burn-in DRAM chips. Several repair methods will be compared in terms of (1) the process and pin compatibility with existing DRAM products and (2) the applicability to the post-package repair scheme which was achieved by integrating the antifuse EPROM into the design of existing DRAM products. These post-package repair schemes using the antifuse are very favorable in achieving a high-yield and high-throughput mass production because the yield loss as much as 2-3 % occurring after the burn-in test with packaged chips can be fixed without any additional process penalty.

In contrast to wafer-level repair schemes, the standard SDRAM protocol and the antifuse EPROM circuit implementations also enable a large variety of field programmable(post-package repair) functions in DRAM by using special test modes available. In particular, they are useful for the in-field repair of failed memory locations, the output impedance matching and calibration

of system memory modules, the programmable analog bias generation to compensate for process variations, the nonvolatile programming of encryption keys and serial numbers as well as the programmable interface protocols and memory bank architectures. As an example, the antifuse calibration technique on DLL delay trimming will be illustrated in comparison with the previous methods [8-9].

II. General Description of Programmable Components

While the integration of typical floating gate EPROM and EEPROM structures requires significant modifications to the existing DRAM processes [7], a simple antifuse EPROM structure can be implemented without any process modifications to the DRAM process by using the thin and highly reliable ONO storage capacitor dielectric available in DRAM technology [11-13]. In particular, the basic antifuse structure was implemented as a 5μm x 5μm crown cell capacitor formed between poly3 and poly4 that required no process modifications or special structures in contrast to the floating gate EPROM structures. Fig. 2(d) shows the cross section and the top view of the widely used ONO crown capacitor. Before programming, the ONO dielectric is essentially an open circuit (see Fig. 1(a)) and has a very high resistance (>100 MΩ). As shown in Fig. 3(a), the ONO dielectric will be broken destructively under high voltage stress between two electrodes (i.e. ~8V and ~10uA/5 x 5 μm^2 antifuse). The resulting short circuit has a significantly lower resistance of <1KΩ. The post-program antifuse resistance over multiple samples was reported to be 125-498Ω as shown in Fig. 3(b). The measured results can guarantee the operation of a programmed state (<40KΩ) in the reported circuitries. The temperature-dependant characteristic exhibited less than 10% variation over the 25-95°C temperature range as shown in Fig. 3(c). In addition, the continuous stress testing with pulse peaks of 3.3V for 6 hours at 10MHz resulted in the change in post-program antifuse resistance less than 10% and the pre-program antifuse resistance larger than 100MΩ. In most cases the pattern area dependence of programmed properties were not found for the antifuse area between 1μm x 1μm ~ 10μm x 10μm.

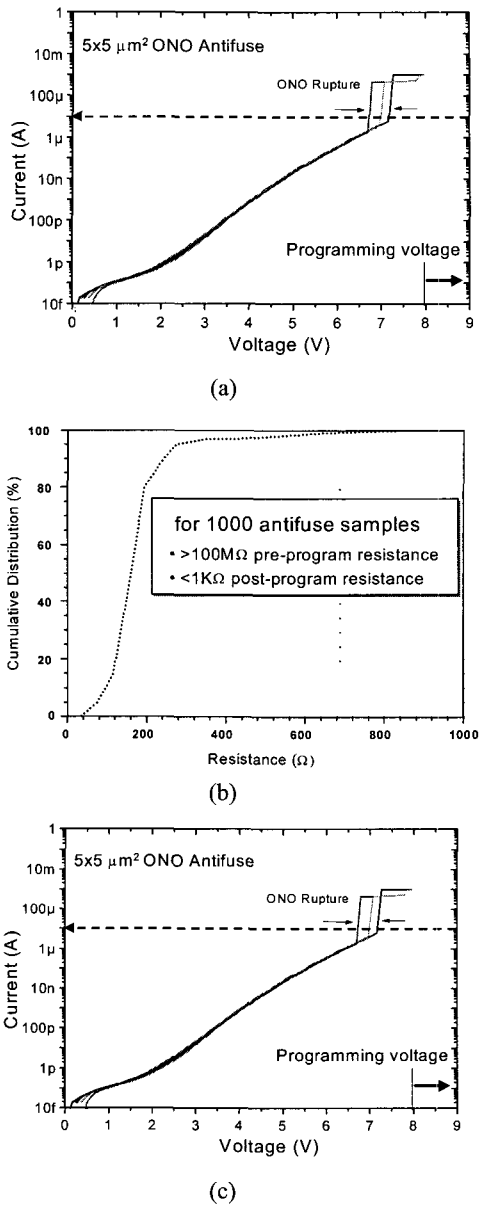


Fig. 3. (a) Measured ONO breakdown characteristics (b) Cumulative distribution of programmed resistance of antifuses, (c) Temperature-dependant characteristics of programmed resistance of antifuse

In other implementations for post-package repair, the poly E-fuse method shown in Fig. 2(c) is reported to have the fusing time 100msec and the fuse fail rate less than 10^{-12} at the ambient temperature of 25°C and the power supply voltage of 3.3V. Although the E-fuse using polysilicon has a good programming characteristic, this method needs to be aided by a pattern opening through

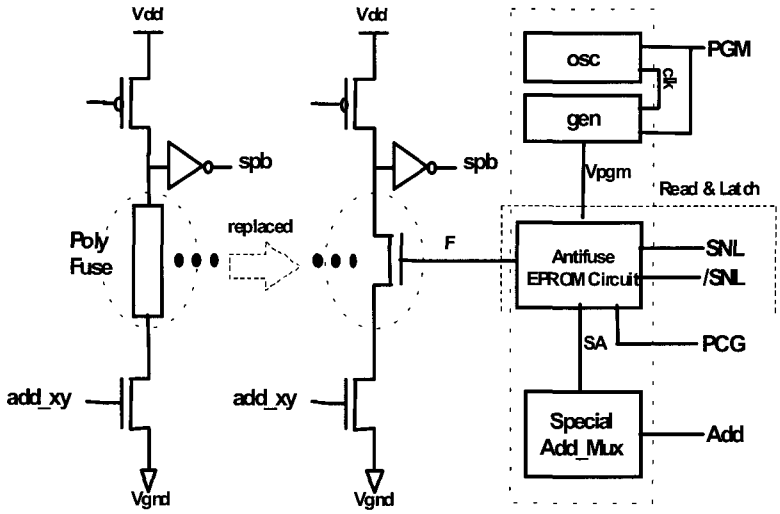


Fig. 4. Wholepost-package memory-repair scheme using the antifuse EPROM

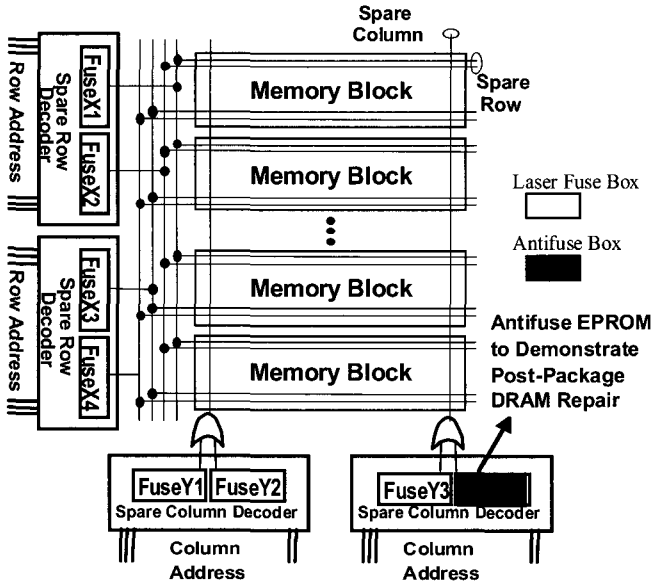


Fig. 5. Column redundancy scheme having antifuse circuitry.

laser illumination to improve the programming efficiency and as a result, the package reliability can become an issue [15]. In case of the flash-fuse, it is reported that the flash-fuse failure rate depends on the number of flash fuses used, i.e. the 3-stacked flash fuse has improved the failure rate by an order of 10^{10} compared to the single flash fuse. The selection of the number of flash fuses can become an issue because of the die penalty [7].

III. Antifuse Programming Circuitry

Fig. 4 shows one of the reported post-package repair schemes using the antifuse EPROM components. The reported post-package repair schemes are composed of three functional parts, which are the voltage generator, the antifuse block, and the address block. The operations involving the antifuse can be simply distinguished into two modes, which are the programming mode and the

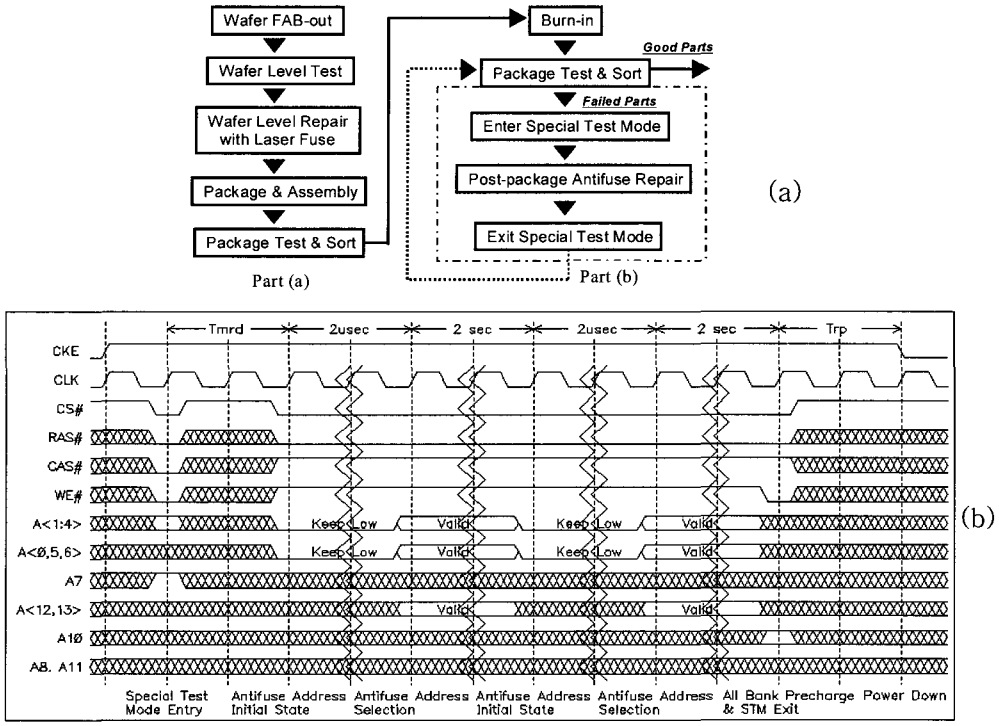


Fig. 6. (a) Generic flow sequence for the DRAM repair algorithm using the post packag repair scheme, (b) brief time diagram of antifuse programming sequence

reading (normal) mode. In the programming mode, the PGM signal activates a pump generator and an oscillator in the voltage generator, which generates the program voltage, Vpgm. Special Add_Mux selects the antifuse using the special address, "Add", for programming fuse address. The Add's are only used for antifuse program and return to low for normal operations. In the reading-and-latching mode during the power-up period, the input memory address (add_xy) can be compared to known defect locations by using a dynamic NMOS logic. When matched, the spb signal activates a redundant memory location to replace the defective memory cell. For reliable operation, the electrically programmable antifuse may not be used directly in the address comparator. Instead the ONO antifuse, resistance is sensed at power-up time and is used to control another transistor that acts as a polysilicon fuse [12].

For an example of the above antifuse circuitry, we proposed a simple repair scheme based on the conventional laser fuse repair scheme for the first time. Fig. 5 shows the proposed antifuse EPROM repair scheme in a simplified 2-Mb memory cell array. In the figure, four fuse boxes and two redundant column decoders are placed in a 2-Mb memory cell array, and the redundant column decoder is controlled by an output from one of the two fuse boxes.

To sustain the pin compatibility with commodity SDRAM chips, an internal voltage generator was used for the programming operation without additional pins. To provide the in-field programmability, an antifuse EPROM circuitry and an NMOS transistor were used as shown in Fig. 4. Antifuse EPROMs are used to program the gate voltage of NMOS transistors into "high" or "low", and the NMOS transistors ("F" in Fig. 4) with low gate voltage correspond to the laser-blown poly fuse.

A. *Antifuse Programming Sequence*

Previous wafer-level antifuse repair schemes of antifuse EPROM in commercial DRAM chips required external high-voltage power supplies for programming [20]. Since the wafer-level repair scheme cannot fix the problems which occurred during the burn-in test of the packaged chip, the post-package repair scheme is widely being adopted. The conventional post-package repair

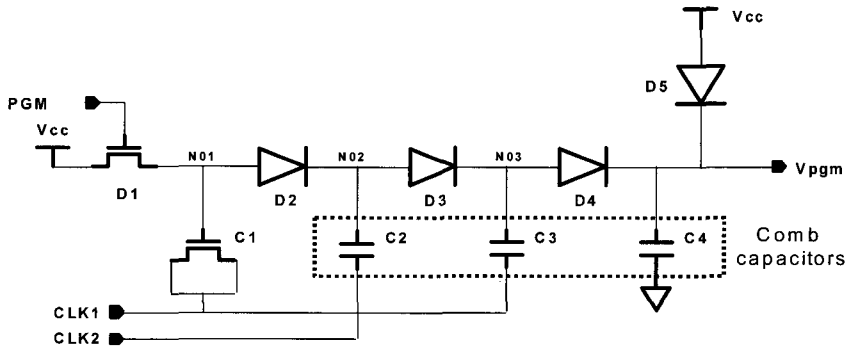


Fig. 7. Schematic of a high voltage charge pump.

scheme applies the off-chip generated high voltage to the chip through the pins. These schemes are not compatible with conventional SDRAM chips in the pin-compatibility specifications since the operation with the standard 2V~3V power supply is essential for maintaining the pin compatibility. To solve the pin compatibility issue an internal voltage generator [10] and a special test mode of the SDRAM protocol were used to antifuse elements.

Fig. 6(a) shows a post package DRAM repair algorithm using the proposed repair scheme, and fig. 6(b) shows the timing sequences for antifuse programming using the special test mode. Part (a) in Fig. 6(a) is the same as the conventional repair algorithm, and the antifuse program mode in part (b) is additionally added for the failed parts of DRAM products after the burn-in test mode. The first step of the antifuse programming mode is the execution of a special test mode (STM). The STM used for the antifuse program is entered when the A7 pin goes up into a high state when all of the RAS#, CAS#, WE#, and CS# pins remain in the low state. The voltage generator is operated and stabilized during the initialization time of antifuse circuitry, forcing the initial state of antifuse address to "low" during in this period. Next, the selected antifuse is programmed during the antifuse address selection time. In summary, the programming sequence is composed of five steps, such as, (1) special test mode entry, (2) antifuse address initialization, (3) antifuse address selection, (4) repetition from (2) to (3), (5) all bank precharge and STM exit. The STM is exited when the RAS# and WE# pins are low and the CAS# and A10 pins are high. This finishes a special antifuse programming test mode. These loops are performed on all repairable packages to attain the maximum yield.

B. *Programming by Internal Voltages*

These antifuse schemes for post-package can be further categorized into the unipolar scheme and the bipolar scheme[12,13]. In the unipolar scheme, an internally generated positive high voltage V_{CC} is used to program the antifuse elements. In the bipolar scheme, one positive voltage V_{CC} and one negative voltage $-V_{CC}$ are generated internally and the $V_{CC} - (-V_{CC})$ voltage is used to program the antifuse elements. Each scheme has advantages and disadvantages depending on chip architecture, operation voltage, in-field operation, and process, as explained in the following two sub-sections.

(1) Unipolar Voltage Scheme for Programming

The internal voltage generator in the reported unipolar voltage scheme includes two parts: an oscillator and a high voltage charge pump. The oscillator is designed to generate two output clocks of CLK1 and CLK2 with complementary phase and the frequency of 10MHz. Non-standard components were utilized in the high voltage charge pump (see Fig. 7). Specifically, a high voltage coupling capacitor was realized by using a comb structure based on fringing capacitances [16,17] that exploits the high interlayer fringing capacitance as well as the interlayer capacitance available with poly1, poly2, metal1 and metal2 in a deep submicron process as shown in Fig. 8. The pitches of poly lines and metal lines for the proposed comb capacitor are fixed at the minimum design rule of metal 2 line, i.e., widths of 0.5 μm and spaces of 0.5 μm. In the 0.22 μm CMOS technology, the

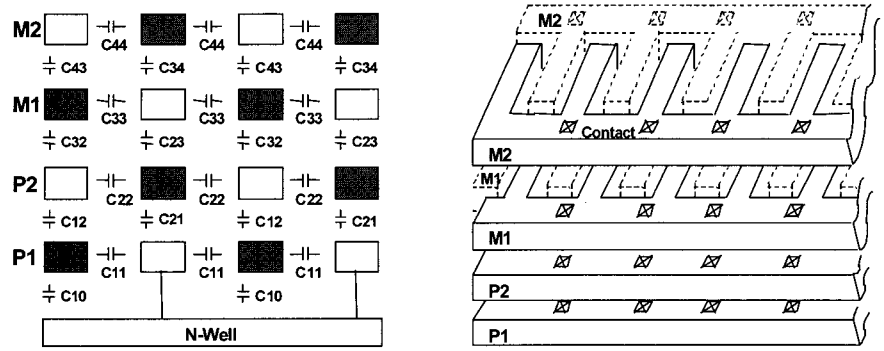


Fig. 8. High voltage capacitor (a) cross-sctional view (b) 3-D perspective view.

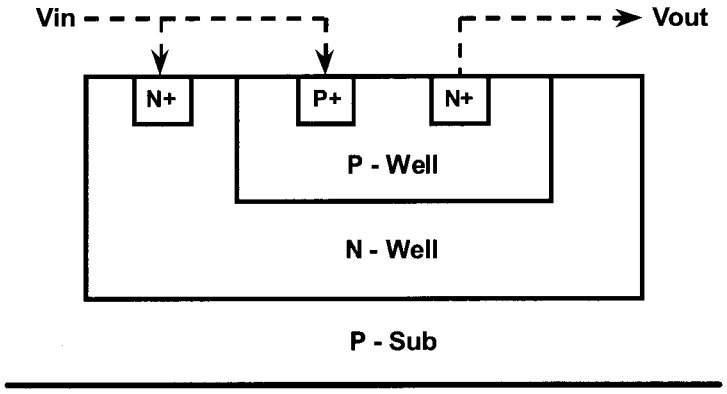


Fig. 9. Triple-well structure of D2-D4 in Fig.7.

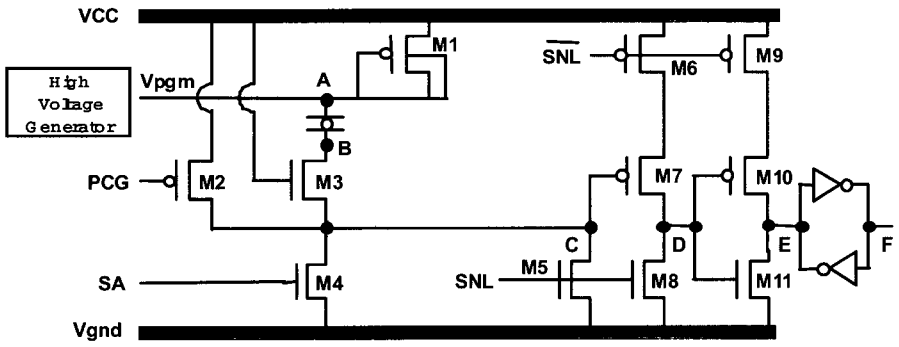


Fig. 10. Unipolar anfifuse circuit for programming and sensing.

comb structure yielded approximately 1pF/1600 μm^2 with a correspondingly very high dielectric breakdown voltage. The capacitance of the comb capacitors was measured by HP 4284 LCR meter with the uniformity variations less than 10%. The proposed comb capacitor becomes more efficient as the minimum line feature becomes more scaled down. To improve the pump efficiency and the long-term reliability, the MOS diode in the standard charge pump(D2~D4 of Fig.7) was also replaced by an isolated pn junction with utilization of the

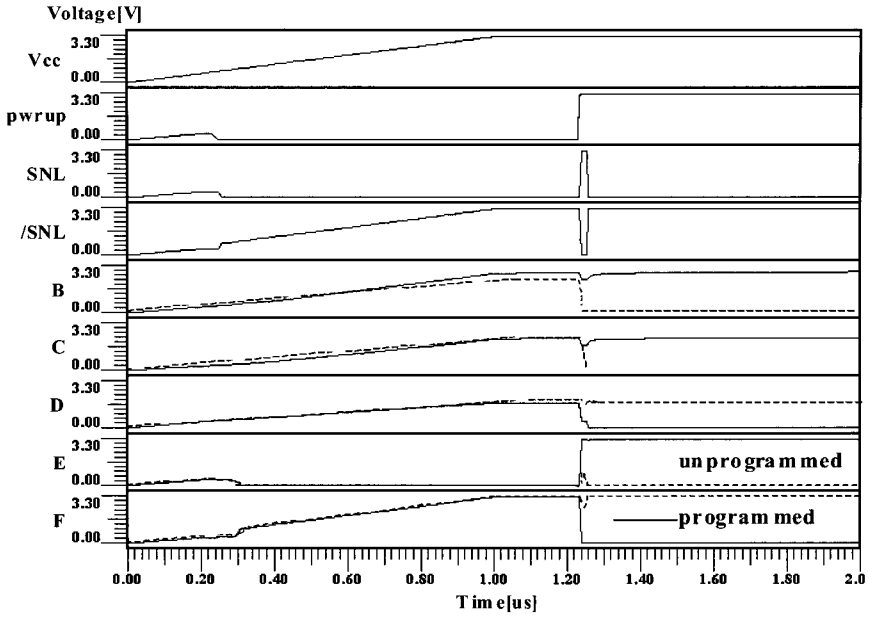


Fig. 11. Operation diagram for programming and sensing.

triple well structure used in advanced DRAM processes as shown in Fig. 9. The high voltage charge pump was designed to provide a minimum of 8V output (Vpgm) with the current capacity of 300 μA and with the chip area of 30,000 μm^2. Due to the relatively large area associated with the high voltage charge pump, only one high voltage generator was used and its output voltage was multiplexed to all antifuse EPROM structures. Although the breakdown voltages of the n+/p-well and p+/n-well junctions were all higher than 8V, and typical MOS gate oxide breakdown voltage was above 11V, special care was taken to limit the exposure of any MOS transistors to voltages larger than 5V during programming for reliability.

Using the circuitry shown in Fig. 10, each antifuse EPROM element can be individually addressed for programming. The antifuse programming cycle is initiated by pulsing PCG "low" to precharge node B to V_{CC} -Vtn through M2 and to protect antifuse EPROM elements that will not be selected for programming. Concurrently, the oscillator for the high voltage charge pump is activated with PGM as shown in Fig. 7, and Vpgm is applied to all antifuse elements in parallel. Subsequently, for selected antifuse elements, SA is set "high" which discharges node B through M3 and M4 and applies the full Vpgm across the antifuse for destructive programming to a low resistance state. If SA is "low," the applied voltage across the antifuse will be limited by the precharged floating node B, and M3 will protect node C and the associated peripheral circuitry from the high programming voltage. After programming, the oscillator for the high voltage charge pump is shut down using PGM, and the external power supply V_{CC} is cycled to activate the circuitry for reading and latching the antifuse EPROM state.

At the power-up time, the state of an antifuse is always sensed and statically latched by the circuit shown in Fig. 10 to improve the antifuse reliability [6] and to enable the high-speed evaluation of the nonvolatile antifuse data. During the power-up time period, since the programming circuit is not enabled, M2 and M4 are both off, and the high voltage charge pump is at "Hi-Z." When external power, Vcc, is sufficiently high and stable, M5, M6, M8 and M9 are pulsed on with clocking signals, SNL and /SNL, for approximately 100ns. By appropriately sizing M5 < M1, the voltage on node C will be approximately V_{CC} -Vtn if the antifuse has been successfully programmed to a low resistance (<40KOhms) and will be pulled to ground if the antifuse is still in the high resistance state. This analog voltage is buffered and further amplified by an inverter formed by M6, M7, and M8. The output voltage on node D is used

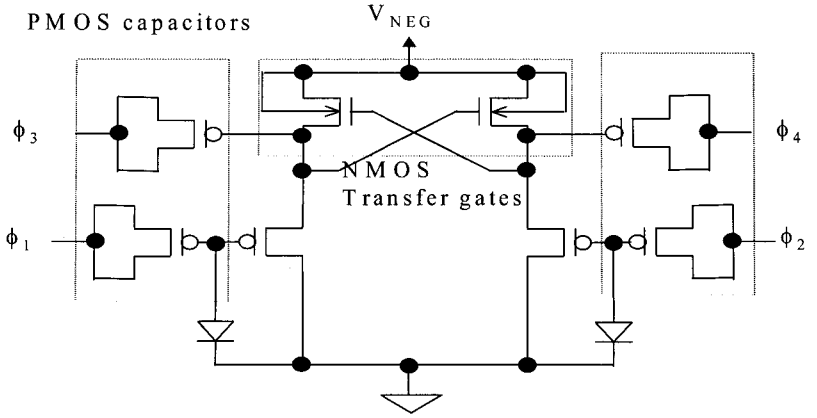


Fig. 12. 1-stage hybrid charge-pump circuit for generating-Vcc.

to drive another inverter formed by M9, M10, and M11 which overdrives and sets the static latch formed by two inverters. The entire sensing and latching operation typically takes less than 20ns and has been demonstrated to be fully operational over the full range of operating temperatures and voltages. After the 100ns clock cycle, the sensing circuitry is shut down by turning off M5, M6, M8 and M9 and also by insuring that the node D is discharged to ground. Thus, if the antifuse is programmed to a low resistance, the output of the static latch, node F, will be "low" and vice versa. These simulated results of typical power up sequence are shown in Fig. 11, which illustrates the operation of sensing and latching the antifuse state.

(2) Bipolar Voltage Scheme for Programming

In the previous unipolar scheme, the programming voltages of V_{PGM} and V_{SS} were applied to the terminals of the ONO insulator where V_{PGM} means a high-positive programming voltage as high as 8 V and V_{SS} is the ground potential. The high voltage requirement of V_{PGM} involved a three-stage Dickson charge-pump circuit with high-voltage tolerable devices. A voltage as high as 8 V generated by the Dickson pump [18] in Fig. 7 can give rise to some reliability problems such as permanent device breakdown and aging, because the nominal DRAM processes are usually intolerant to high-voltage stresses. To solve these shortcomings of the unipolar high voltage charge pump scheme, a bipolar scheme was proposed where antifuses are programmed using bipolar voltages of V_{CC} and $-V_{CC}$. Here, V_{CC} is the supply voltage with a range of 2.9 V~ 4.2 V including both the normal and burn-in conditions. Unlike generating V_{PGM} as high as 8 V, voltage of $-V_{CC}$ can be generated using a simple one-stage hybrid charge-pump circuit [19] with MOS capacitors as shown in Fig. 12. Using the MOS capacitors instead of the comb capacitors makes the layout area of the programming voltage generation circuit much smaller. In addition, the absolute value of $-V_{CC}$ is much smaller than value of V_{PGM} of the unipolar scheme, which alleviates the high-voltage problems such as device breakdown and aging.

Two major functional improvements were made in the bipolar scheme compared to the unipolar scheme. First, the programming voltages for rupturing the antifuse changed to bipolar voltages of V_{CC} – ($-V_{CC}$)[13]. This was done to replace a high-voltage generator by two relative low-voltage generators (V_{CC}, - V_{CC}), alleviating the high-voltage related problems such as device breakdown and aging, and achieving a smaller layout area for the antifuse circuit than the previous high voltage scheme [12]. Second, an efficient bit-repair scheme was proposed instead of the conventional line-repair scheme after the post-package burn-in, which reduces the layout area for the redundancy bits [13,14]. Also, using the static latches as the redundancy bits eliminates possible defects in the redundancy area, making this scheme robust.

Fig. 13 shows the antifuse programming circuit for the bipolar scheme. When both signals of 'add<i>' and 'anti_cut' go high, the node 'A' also goes high with voltage of V_{INT}. As a result, two ports of antifuse cell are ruptured with V_{INT} and the negative-generated voltage of

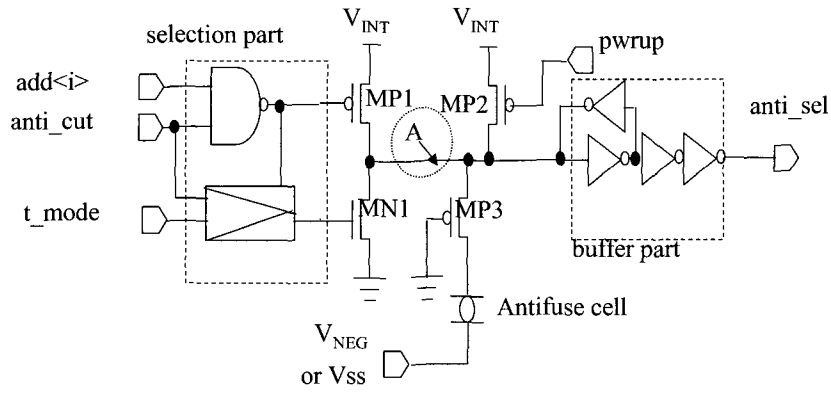


Fig. 13. Antifuse programming circuit.

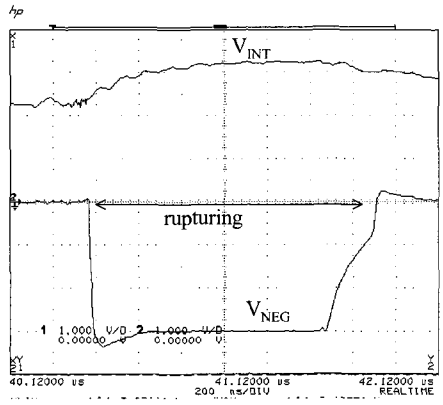


Fig. 14. Measured waveforms of V_{INT} and V_{NEC}.

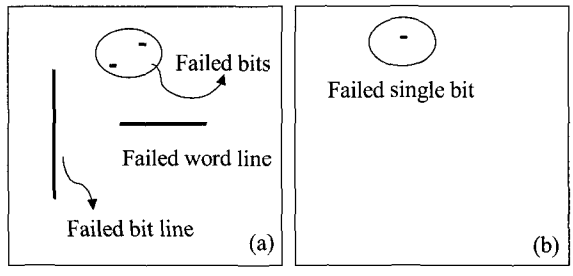


Fig. 15. Comparison of the bit maps between (a) the wafer probe test and (b) the post-package burn-in test.

V_{NEG}. One should note here is that V_{INT} is connected to the internal regulated voltage that has lower value than the external supply voltage in normal operations, but is directly connected to the external supply voltage in rupturing the antifuses. Required rupturing time for the antifuses has strong dependence on the voltage across the antifuse cell(V_{INT}-V_{NEG}) and the thickness the ONO insulator which forms the antifuse cell. The measured waveforms of V_{INT} and V_{NEG} during programming are shown in Fig. 14. During the normal modes, the negative charge pump is shut down and the sink nodes of the antifuses are switched from V_{NEG} to Vss(0V). During this mode, the output voltage of the selection part (NAND gate) of Fig. 13 is set to high to shut off MP1 by setting the 'anti_cut' signal to low. Also the gate level of weak NMOS MN1 is switched off by the low level of signal 't_mode'. The level of node 'A' is determined from whether the antifuse cell is programmed or not. When the antifuse cell is programmed, the signal, 'anti_sel' is at high state. During the normal mode, the voltage difference between the node A and Vss of non-programmed antifuse cells is precharged to a voltage slightly less than V_{INT} during the power-up time and maintained to that value by the buffer part. Thus, unwanted programming of the antifuse cells during normal operations is avoided.

Fig. 15 shows typical bitmaps of (a) the wafer probe test and (b) the post-package test after the burn-in stress. In most cases of wafer-probe test and post-package test, the wafer probe test shows appearances of both the failed lines and failed bits as shown in Fig. 15 (a), however the post-package test shows only the failed bits as shown in Fig. 15 (b). This is due to the fact that the failed bits after the burn-in test mainly come from the poor refresh characteristics and the insufficient AC timing margins. Unlike Fig. 15 (b), the defects shown in Fig. 15 (a) are mainly due to solid defects occurring at word lines, bit lines, and memory cells, the poor refresh characteristics, the insufficient timing margins, and so on, exhibiting

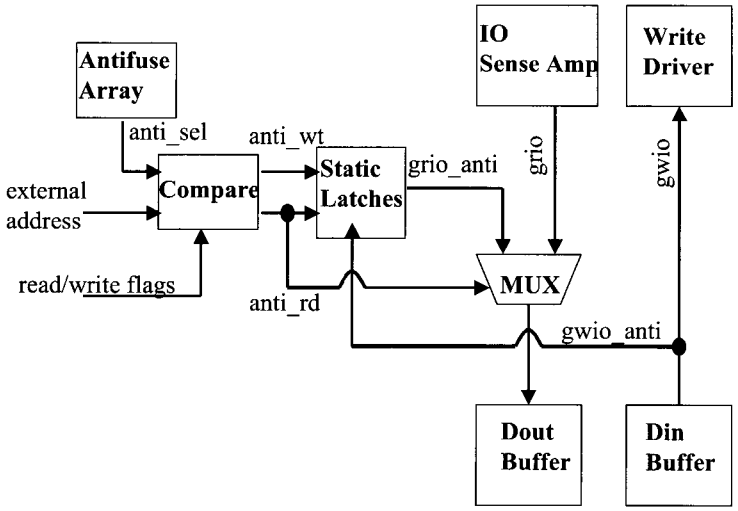


Fig. 16. Block diagram of the post-package antifuse repairable column path using the static latches.

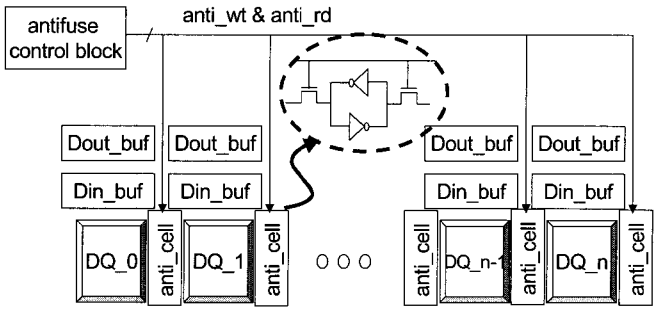


Fig. 17. Placement of the static latchesnear to the DQ pads.

both failed lines and bits. Note that the number of failed bits after the burn-in test is very small. The statistical results of the burn-in test for 0.16μm 256M SDRAM chips indicate that 80% of the total failed chips has only single failed bit among the total 256 M bits in a chip[13]. Hence the conventional word-line or bit-line repair scheme can be considered to be redundant and inefficient for the post-package repair scheme. According to statistical results, the line-repair scheme of the high voltage program scheme in a vast majority of cases, replaces good bits of very large numbers for repairing only one defect bit. To overcome this inefficiency of the previous line repair, a bit-repair scheme using static latches can be used [13,14]. Because the static latches are formed by two cross-coupled inverters located in the peripheral area, they cannot be destroyed during the burn-in stress, which eliminates possible defects in the redundancy area. Moreover, this new scheme requires only 16 latches for the SDRAM operation with 16 I/O channels, reducing the layout area for the redundancy bits to be much smaller than the line-repair scheme.

Fig. 16 shows a simple block diagram of the modified column path including the proposed post-package antifuse repair scheme. At first, the input column addresses(external address) are compared with the programmed addresses ('anti_sel' in Fig. 16) in the antifuse array block. In case when the input column address matches, either 'anti-rd' or 'anti-wt' signal is asserted depending on the external READ or WRITE command (read/write flag). When the 'anti-rd' signal is set, the MUX activates the read-data path from the static latches and simultaneously deactivates the data path from the I/O sense amplifiers. Here the read-data path from the static latches is represented by 'grio-anti' and the path from the I/O sense amplifiers is represented by 'grio', respectively. Similarly, the write-data path to the

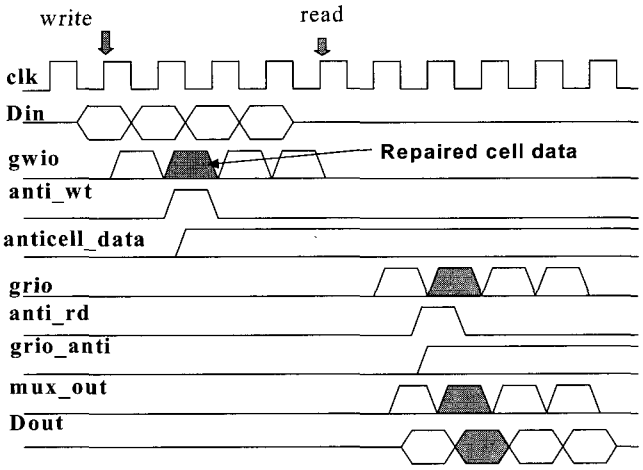


Fig. 18. Timing diagram of the repaired cell.

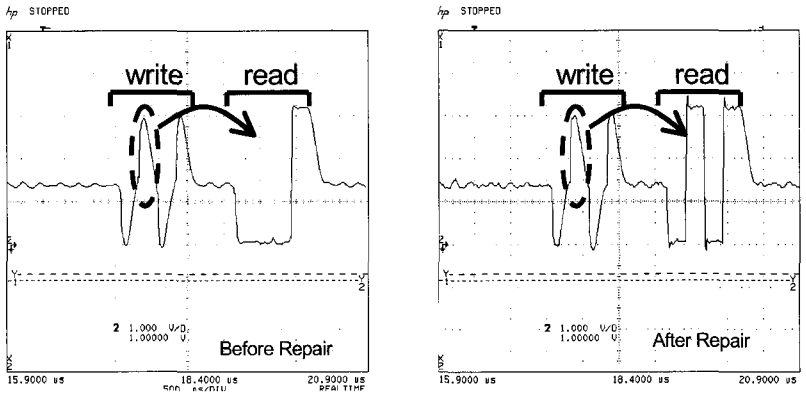


Fig. 19. Measured results before and after repair.

write driver is represented by 'gwio' and the write-data path to the static latch is represented by 'gwio_anti', respectively. When the 'anti-wt' signal is asserted, the write-data path of 'gwio_anti' is latched, storing the data from the data-input(Din) buffers in the static latches. Fig. 17 indicates that the static latches are located in close proximity to the data input and output buffers(Din-buf, Dout-buf) of the DRAM chip. It ensures that the data accesses to the latches are not slower than the accesses to the I/O sense amplifiers and the write drivers which are placed near the DRAM cell array. Moreover, inserting the static latches in a chip does not increase the total layout area for the DRAM peripheral. This is due to the fact that the layout area of the modern DRAM peripheral is determined not by the number of transistors but by the number of routing signals. The only global signals that are added for the antifuse circuit are 'anti_rd' and 'anti_wt', which occupies very little portion of the total global signals.

C. *Experimental Results*

Fig. 18 shows the timing diagram of a 4-bursting write-read operation including the access to the repaired bit that is shown to be the second bit among of the four data bits. The second data during the 4-bursting write operation is written to a static latch and the second output data is read from the same latch. The corrected data are represented by the "mux-out" results of normal DRAM cells and repair cells. Fig. 19 shows a scope trace of the measured results before and after the repair. The actual area penalty of reported antifuse repair schemes is strongly dependent on the specific application, the amount of integrated antifuse EPROMs, the power and signal routing requirement and so on. As an example, the

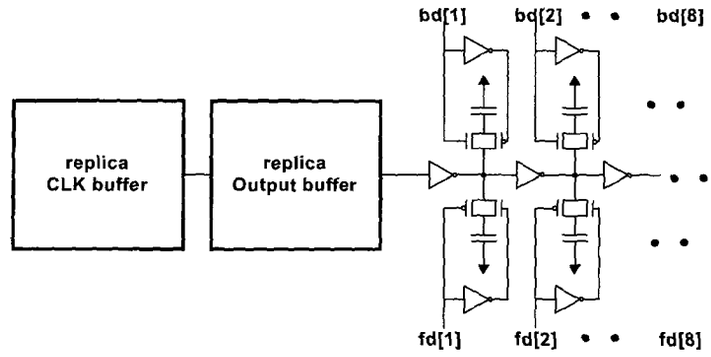
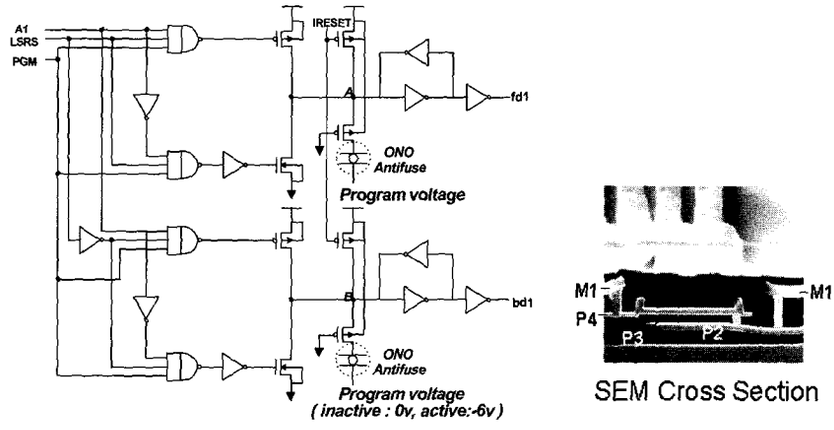


Fig. 20. Replica delay including the programmable delay.



(a) (b)

Fig. 21. (a) Antifuse circuit for skew calibration (b) SEM photograph of OnO antifuse.

area penalty of the antifuse circuit to the total chip area was reported to be as small as 0.16 % in the bipolar scheme [13]. It is also reported that the yield improvement by the post-package repair scheme reaches as much as 2.4 % for a 0.16 μm 256M SDRAM.

IV. Applications

These antifuse schemes can be implemented in variety of applications in addition to the post package bit repair. This section discusses the use of the antifuse to improve the performance of the highly sensitive DLL circuits for high speed DRAM such as DDR SDRAM.

Although the replica delay circuit, which is a vital component of DLL, can be well matched with the sum of the on-chip and off-chip delays at design time, the on chip process variations and the unexpected changes in the off chip circumstance such as output load, clock slew-rate and so on, result in the unavoidable skew. There are two methods for the skew elimination: the wafer-level tuning by laser or electric stress [8] and the post-package tuning by antifuse or fuse [9]. The wafer-level tuning is not effective since the wafer-tester is not precise and also the off-chip condition cannot be considered. Although the post-package tuning by antifuse is more practical, the conventional post-package method has some problems [9], such as the requirement for the application of the external high voltage through pins to rupture the antifuse.

Fig. 20 shows the programmable replica delay circuit based on the antifuse circuitry. The entire circuitry is divided into three functional units, the replica clock buffer, the replica output buffer, and the tunable delay circuit. The tunable delay circuit is connected to the antifuse circuitry and the antifuse is made of ONO dielectrics as shown in Fig. 21.

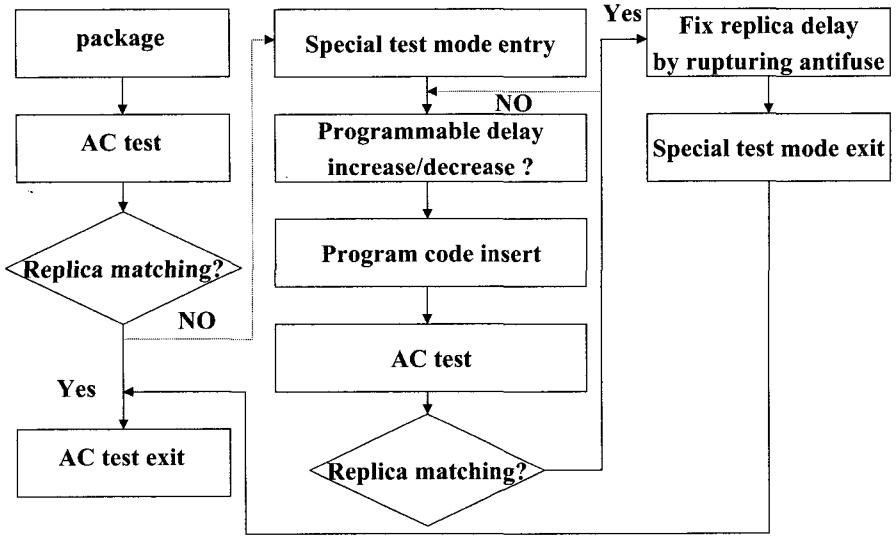


Fig. 22. Flow of skew calibration after package process..

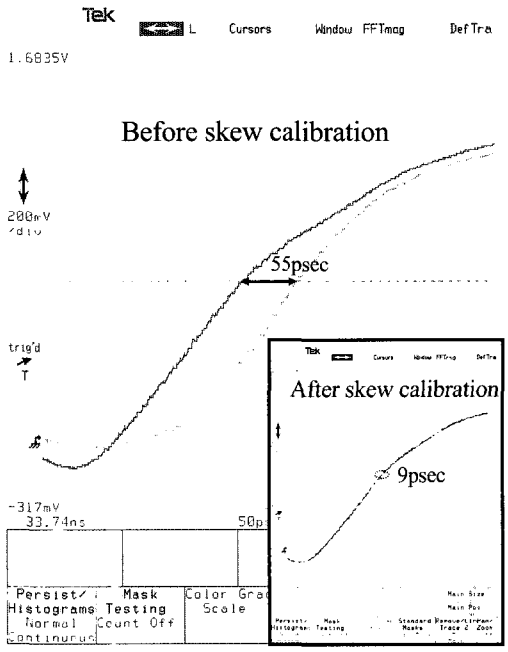


Fig. 23. Flow of skew calibration after package process..

The sequence of skew calibration is explained as follows. When the DLL circuit is enabled for test, the nodes fd[1-8] and bd[1-8] in Fig. 20 are all fixed at the high state because the initial program voltage is at the ground level and the RESET signal initializes the node A and B of Fig. 21 at the Vdd level. In this state, no address code can have an effect on the fixed levels of fd[1-8] and bd[1-8]. Firstly, the skew between the external clock and the data strobe signal is measured. The measured skew is estimated by the selection of optimal number of delay loads. After the PGM signal is activated, the program code corresponding to the estimated number of delay loads is applied to the address pins and the skew is re-measured. This process is iterated

to increase or decrease the replica delay times for minimizing the skew. When the skew is almost eliminated, the inserted program address code is fixed and the on-chip negative voltage generator is enabled to produce a program voltage (-3.5~-4.5V) for rupturing antifuses. The replica delay is tuned through the flow shown in Fig. 22. According to the simulation results, the programmable tuning range using eight antifuses is from −350psec to +350psec and the minimum tuning resolution is approximately 10psec. Fig. 23 shows skews before and after a skew calibration. The skew before the calibration is measured to be 55psec, which consists of the phase detector offset and the replica mismatch offset due to process variations. After the calibration, the measured skew is reduced to 9psec with the measured peak-to-peak jitter of 46ps.

V. SUMMARY

In this paper, we briefly reviewed the fuse and antifuse repair methods on the wafer-level and also on the package-level (post-package). As the technology is scaled down, these repair methods become more important. Although the wafer-level repair method is mainly used nowadays, the post-package repair method is becoming an essential auxiliary technique for the cost and the design efficiency. Although several options for programming components have been studied, the ONO antifuse post-package repair scheme turns out to be the most cost-efficient and is expected to be widely used in the future. In most cases, the selection of fuse or antifuse repair methods on the package-level strongly depends on the process and should be chosen by comparing both the reliability of programmed components and the fabrication cost. The fabrication cost can be estimated by the chip area and the requirements for particularly added processes.

As shown in the reports [11-13], the post-package repair methods using antifuse EPROM components can be categorized into unipolar and bipolar voltage schemes. The bipolar voltage scheme is more efficient for manufacturing than the unipolar voltage scheme, because of the relative small chip area and the better device reliability due to the use of two lower voltage supplies instead of a single high voltage supply as in the unipolar voltage scheme. The manufactured results showed the improvement of the whole yield by 2~3% through replacing the failed cells with redundant cells after the burn-in stress.

As a demonstration of the antifuse repair scheme on the package-level (post-package), it was applied to the tunable delay cells in a replica delay circuit of DLL and the improvement of the clock skew from 55ps to 9ps was measured on the fabricated chip.

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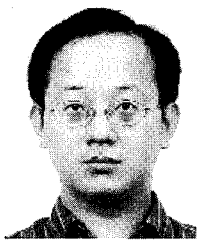

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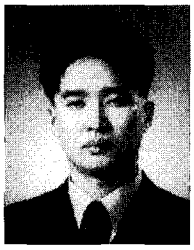

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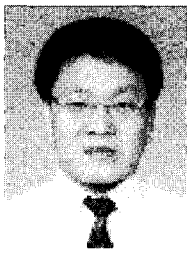

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