Electrical and Chemical Properties of ultra thin RT-MOCVD Deposited Ti-doped Ta_2O_5

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Abstract— **In Recent results suggested that doping Ta_2O_5 with a small amount of TiO_2 using standard ceramic processing techniques can increase the dielectric constant of Ta_2O_5 significantly. In this paper, this concept is studied using RTCVD (Rapid Thermal Chemical Vapor Deposition). Ti-doped Ta_2O_5 films are deposited using $TaC_{12}H_{30}O_5N$, $C_8H_{24}N_4Ti$, and O_2 on both Si and NH_3-nitrided Si substrates. An NH_3-based interface layer at the Si surface is used to prevent interfacial oxidation during the CVD process and post deposition annealing is performed in H_2/O_2 ambient to improve film quality and reduce leakage current. A sputtered TiN layer is used as a diffusion barrier between the Al gate electrode and the $TaTi_xO_y$ dielectric. XPS analyses confirm the formation of a $(Ta_2O_5)_{1-x}(TiO_2)_x$ composite oxide. A high quality $TaTi_xO_y$ gate stack with EOT (Equivalent Oxide Thickness) of 7Å and leakage current Jg=0.5A/cm^2 @ Vg=-1.0V has been achieved. We have also succeeded in forming a $TaTi_xO_y$ composite oxide by rapid thermal oxidation of the as-deposited CVD TaTi films. The electrical properties and Jg-EOT characteristics of these composite oxides are remarkably similar to that of RTCVD Ta_2O_5, suggesting that the dielectric constant of Ta_2O_5 is not affected by the addition of TiO_2.**

Index Terms — **High K gate dielectric, Metal gate, CMOS Fabrication process.**

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I. INTRODUCTION

High dielectric constant materials such as Ta_2O_5, TiO_2, $SrTiO_3$, $(Ba,Sr)TiO_3$ have been considered as a replacement for SiO_2 and SiN in future DRAM capacitors and MOSFET gate oxide applications [1-3]. Among them CVD Ta_2O_5 and TiO_2 have received significant interests as a potential gate dielectric material for sub-100nm CMOS technology because of their high dielectric constant and excellent step coverage [4-5].

Recent results from Cava et al. [6] showed that the dielectric constant of Ta_2O_5 can be enhanced significantly (by a factor of 4) by the addition of ~8% TiO_2. This would have considerable impact on future high-K gate dielectric technology. In their study, ceramic samples in the Ta_2O_5-TiO_2 system were made by standard ceramic processing technologies. In our study, attempts are made to apply this concept in a more manufacturable RTCVD process for the fabrication of a Ta_2O_5 gate stack with the addition of controllable amount of TiO_2.

II. EXPERIMENTS

In our experiments, MOS capacitors with $TaTi_xO_y$ dielectric were fabricated on p-type silicon wafer by *in-situ* rapid-thermal multiprocessing whose temperature-time profile is shown in Fig 1. The bottom passivation layers were grown in NH_3 at 700°C for 10 s or in NO at 800°C for 20 s. An HF dip was applied after NO passivation processing to reduce the interface layer thickness. $TaTi_xO_y$ films were deposited at 450°C for

120sec by reacting $TaC_{12}H_{30}O_5N$ and $C_8H_{24}N_4Ti$ with O_2 simultaneously using N_2 as the carrier gas. Post deposition annealing was performed in H_2/O_2 (50:50) at 600~800°C for 30 s to improve film quality and reduce leakage current. An alternative approach was also used by depositing the Ta and Ti without O_2 present, followed by RTP O_2 oxidation. A TiN diffusion barrier was deposited on the $TaTi_xO_y$ films by reactive sputtering and Al was used as a gate electrode.

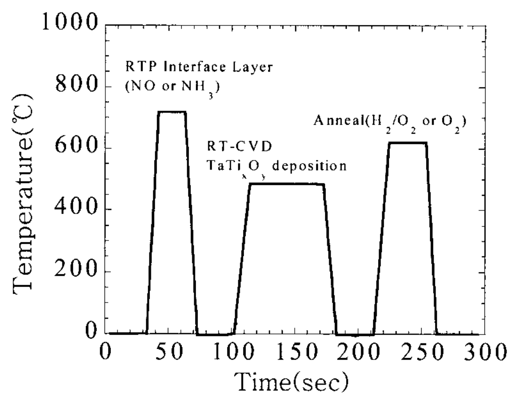

Fig. 1. *In-Situ* RTP fabrication process for $TaTi_xO_y$ gate stack dielectics.

The EOT is extracted from a simulation program considering quantum mechanical (QM) effects (7). The chemical properties of ultra-thin $TaTi_xO_y$ films were investigated by *in-situ* XPS (X-ray Photoelectron Spectroscopy) in a separate CVD-UHV system. Deposition and annealing for XPS were carried out in a bench scale CVD reaction chamber (base pressure ~ $1x10^{-8}$ Torr) connected by a gate valve and sample transfer mechanism to a UHV (Ultra High Vacuum) XPS chamber (base pressure ~ $8x10^{-10}$ Torr). XPS data were taken with a cylindrical mirror analyzer at 25eV pass energy and analyzed for peak positions and peak areas.

III. Results and Discussion

The interfacial layer between the high-K layer and Si is one of the key issues related to the development of high K dielectric stack. It was reported that ultra thin CVD Ta_2O_5 (4) with an NO-grown oxynitride interface layer showed 3 orders of magnitude lower leakage current compared to the thermal oxide with same Tox,eq and superior interface quality. In this work, $TaTi_xO_y$ devices with an NO interface layer show a similar trend to Ta_2O_5 devices as shown in ref [4]. In order to reduce EOT, an NH_3-based interface layer is used instead of an NO interface layer. The NH_3-based interface layer shows stronger resistance to oxygen diffusion during $TaTi_xO_y$ deposition and post-deposition annealing and by using an NH_3 interface layer, we obtained thinner films with EOT=7Å, Jg=0.5A/cm^2 @ Vg=-1V. Fig. 2 and Fig. 3 show the C-V (sweep rate: 500mV/sec) and I-V of this film. The Jg-EOT characteristics are quite similar to that of CVD Ta_2O_5 films, suggesting that the addition of TiO_2 in our case may not have a major impact on the dielectric constant of Ta_2O_5, as reported in [6]. The high frequency C-V characteristics of $TaTi_xO_y$ devices (EOT = 11.5Å) show that the NH_3-based interface layer has similar good interface quality as an NO interface layer (Fig. 4). For the same EOT, the leakage current of the NH_3 interface devices is about one order of magnitude lower than that of devices with an NO interface layer (Fig. 5).

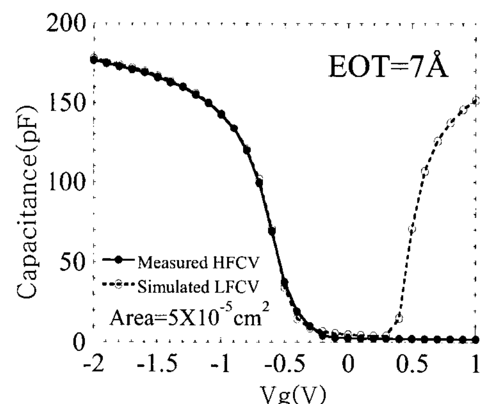

Fig. 2. HFCV of $TaTi_xO_y$ film with NH_3 interface layer (EOT=7Å).

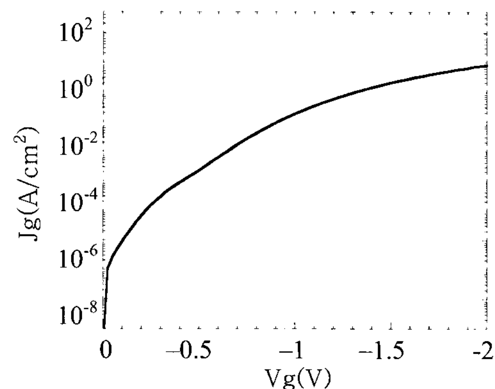

Fig. 3. I-V of $TaTi_xO_y$ film with NH_3 nterface layer (EOT=7Å).

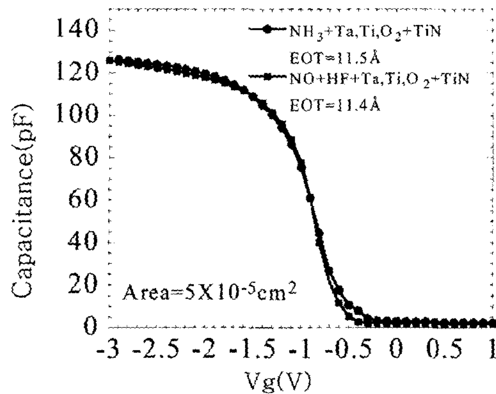

Fig. 4. HFCV of $TaTi_xO_y$ film with NO and NH_3 interface layer.

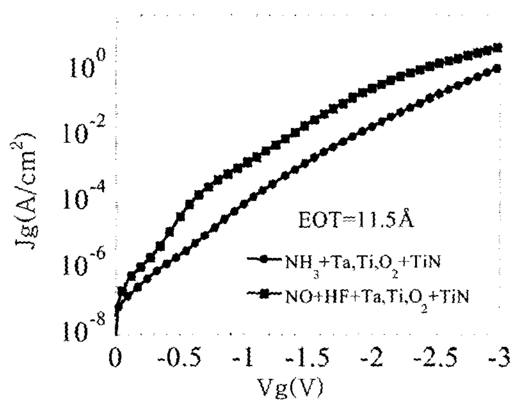

Fig. 5. I-V of $TaTi_xO_y$ film with NO and NH_3 interface layer.

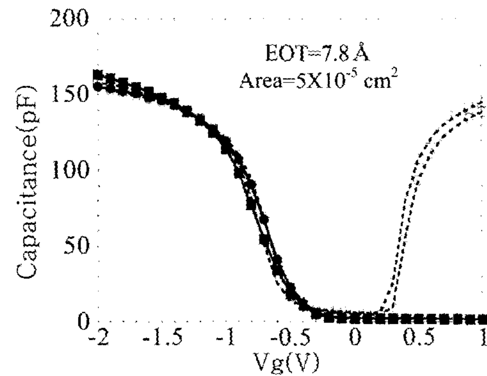

Fig. 6. Measured HFCV and simulated LFCV of $TaTi_xO_y$ gate stack.
(solid circle : HFCV of co-deposition film, open circle : LFCV of co-deposition film.
solid square : HFCV of oxidation of TaTi film,
open square : LFCV of oxidation of TaTi film)

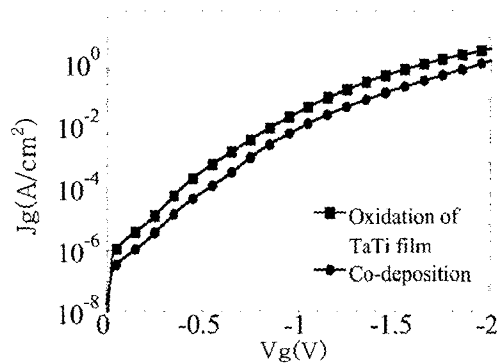

Fig. 7. I-V of $TaTi_xO_y$ devices fabricated by co-deposition and post- deposition oxidation of TaTi films.

We have also studied the formation of $TaTi_xO_y$ by introducing Ta, Ti precursors into the CVD chamber without O_2 present, followed by an RTP oxidation O_2 at 450~550°C. In Fig. 6 and Fig. 7, devices with post deposition oxidation are compared with co-deposition devices in terms of C-V and I-V characteristics. As shown in Fig. 5, for the same EOT, oxidation of TaTi devices show a little higher leakage current than co-deposition devices. The resulting $TaTi_xO_y$ film after oxidation has similar stoichiometry to the co-deposited films with O_2 present during deposition, the stoichiometry of the films was obtained from peak areas of XPS spectra of Ta 4f, Ti 2p, and O 1s with consideration of atomic sensitivity factors, O 1s peak was deconvoluted to exclude oxygen signal from interfacial Si-oxide. However, N was detected in the as-deposited $TaTi_x$ film, which was not completely removed even after 45s oxidation. The increase of leakage current in these films may be due to this residual N which was not found in conventional Ta,Ti,O_2 co-deposition.

XPS analysis was performed on an as-deposited $TaTi_xO_y$ film (Fig. 8), $TaTi_xO_y$ deposited on NH_3-passivated film (Fig. 9) and Ta/Ti deposited film followed by oxidation (Fig. 10). From literature, Ta 4f (7/2) from Ta_2O_5 peaks at 26.8eV and Ti 2p (3/2) from TiO_2 peaks at 458.8eV [8]. In Fig. 8, Ta 4f (7/2) and Ti 2p (3/2) peaked at 26.71 and 458.25 eV, respectively, suggesting that both Ta and Ti were not fully oxidized which could be attributed to the Ta-Ti bond. This observation indicates the CVD $TaTi_xO_y$ (x~0.17, y~2.56) film is a composite oxide. The Si 2p peaks at 99.1eV represent the Si substrate and the second peak at 102.48eV represented non-stoichiometric Si oxide (SiO_x, x<2), compared with 103.3eV from fully oxidized Si (SiO_2) [8]. The O 1s peak could be decomposed into two peaks – one from $TaTi_xO_y$ and the other from SiO_x. N 1s spectrum (not shown) showed the as-deposited film

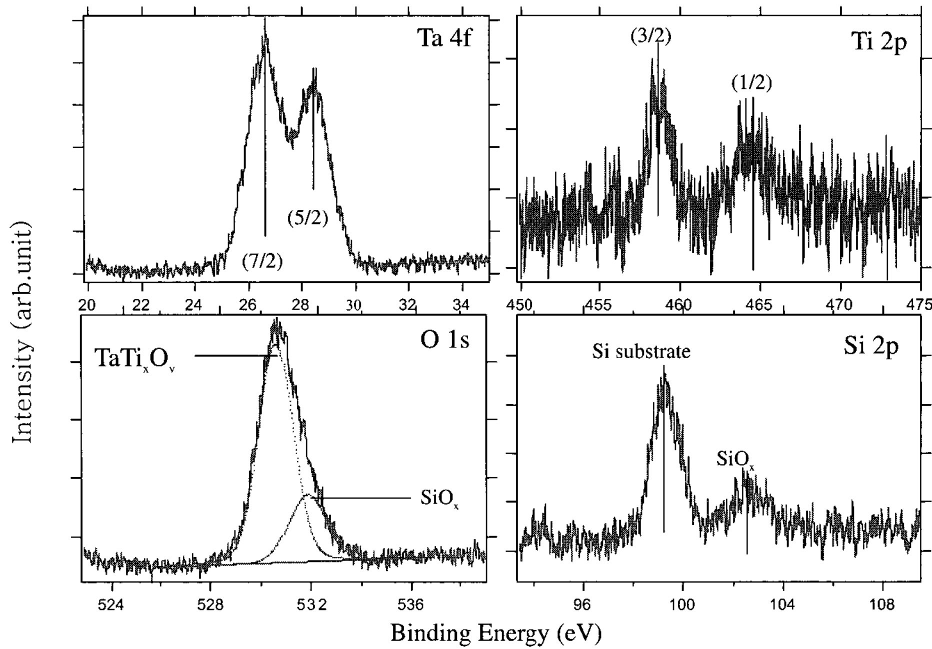

Fig. 8. XPS of Ta 4f, Ti 2p, O 1s, and Si 2p of $TaTi_xO_y$ film deposition on clean Si(100) at 500 °C for 10 s.

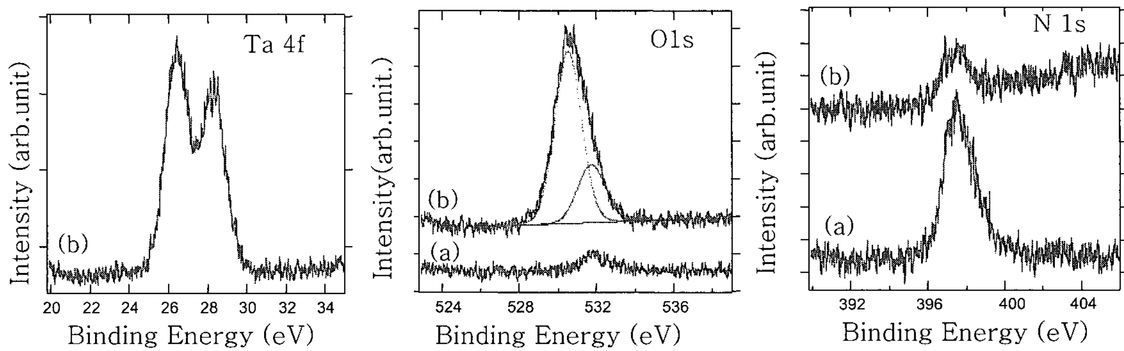

Fig. 9. XPS of Ta 4f, O 1s and N 1s of $TaTi_xO_y$ deposited on nitrided Si with NH_3 at 500 °C for 10 s(b); curves (a) are the XPS taken before Ta_2O_5 deposition.

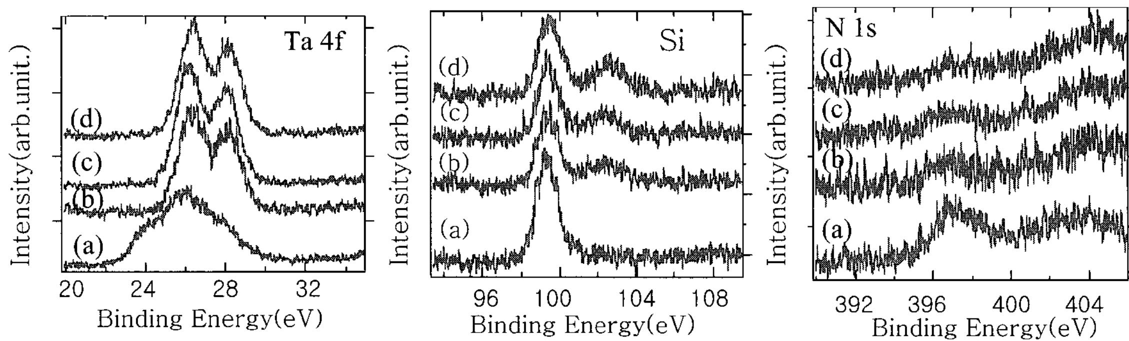

Fig. 10. XPS of Ta 4f, Si 2p, N 1s, and of (a) as-deposited $TaTi_x$ film, followed by oxidation in O_2 at (b) 450 °C for 30 s, (c) 45 s and (d) 75 s.

contained no N within the XPS detection limit. Fig. 9 shows the XPS of $TaTi_xO_y$ deposited on NH_3-passivated Si at 500 °C for 10 s. A small O 1s peak, indicating some O incorporation in the nitride film, was from the

background during the nitridation. The N 1s peak position (397.5eV) was 0.1eV higher than that from Si_3N_4 (397.4eV) (8), also indicating slight O incorporation. After film deposition, the nitrided Si was oxidized, resulting in the 8Å thicker SiO_xN_y(x~0.15, y~1.12). An alternative approach was implemented by depositing the film without co-dosing O_2 and followed by O_2 oxidation at relatively low temperature (< 500°C). As shown in Fig. 10, there was no evidence of SiO_x formation from Si 2p spectrum after the deposition of $TaTi_x$. SiO_x was formed, due to the diffusion of O_2, during oxidation (Fig. 8 (b), (c), and (d)). There were at least two oxidation states in both Ta and Ti spectra for as-deposited $TaTi_x$. The Ta and Ti peaks at lower binding energies could result from the bonds with the precursor ligands. Nevertheless, those Ta and Ti components at lower binding energies were eliminated after oxidation in O_2 at 450°C for 30 s (Fig. 10 (b)). The resulting $TaTi_xO_y$ after oxidation had similar stoichiometry as if the film were deposited directly with O_2. However, N in the as-deposited $TaTi_x$ film still could not be completely removed, although reduced, even after additional 45 s of oxidation (Fig. 10 (d)), and finally removed by oxidation at 500°C for 30 s.

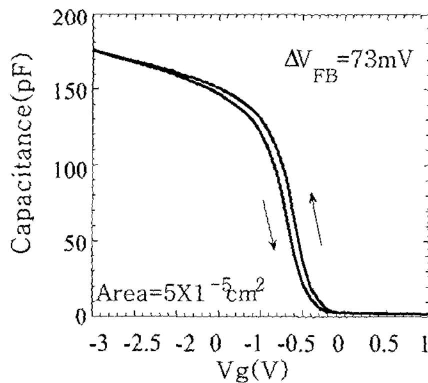

Fig. 11. Hysteresis characteristic of a $TaTi_xO_y$ film with NH_3 interface layer.

The hysteresis of the high frequency C-V of the $TaTi_xO_y$ film was evaluated (Fig. 11). For the $TaTi_xO_y$ film (EOT~7Å) with NH_3 interface layer and H_2/O_2 annealing at 600°C for 60 s, the amount of V_{FB} shift was 73mV. The SILC (Stress Induced Leakage Current) was measured under constant negative voltage stress with E=14MV/cm for 1000 s. For $TaTi_xO_y$ with NH_3 interface layer, the increase of leakage current due to stress was 11% (Fig. 12) and V_{FB} shifted 72mV (Fig. 12). In comparison, for $TaTi_xO_y$ without interface layer, the increase of leakage current was 62% (Fig. 12) and V_{FB} shifted as much as 208mV (Fig. 14). This means that the $TaTi_xO_y$ film without interface layer has more traps, which is believed to be due to sub-oxide grown at the interface (Fig. 8).

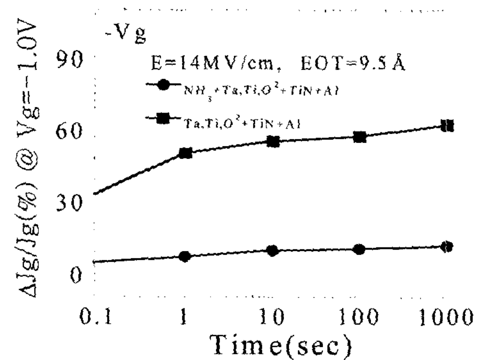

Fig. 12. Stress induced leakage current as a function of stress time for $TaTi_xO_y$ with NH_3 interface layer and without interface layer.

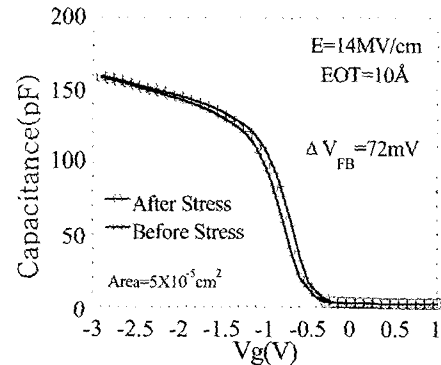

Fig. 13. C-V curves of before and after constant voltage stress (E=14MV/cm)for $TaTi_xO_y$ with NH_3 interface layer.

The conduction mechanism of $TaTi_xO_y$ was studied by investigating the temperature dependence of the leakage current. The Schottky plot in Fig. 15 (a) and the Poole-Frenkel plot in Fig. 15 (b) show a linear relationship between Jg vs. $E_{eff}^{1/2}$ (E_{eff}=Vg/Teq) at low electric field (E<2MV/cm), and a linear relationship between Jg/E_{eff} vs. $E_{eff}^{1/2}$ at high electric field (E>2MV/cm). This indicates that the Schottky mechanism is dominant at low electric field and the Poole-Frenkel mechanism becomes dominant at high electric field [9]. Fig. 16 shows the temperature dependency of the leakage

current. At low electric field, leakage current shows more dependence on temperature, which supports the Schottky-type conduction mechanism in this region

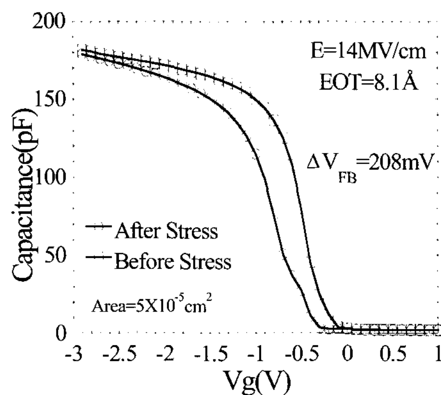

Fig. 14. C-V curves of before and after constant voltage stress (E=14MV/cm) for $TaTi_xO_y$ without interface layer.

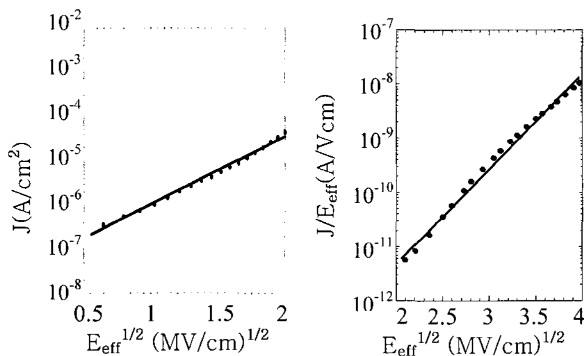

Fig. 15. (a) Schottky plot of $TaTi_xO_y$ with NH_3 interface layer (b) Poole-Frenkel plot of $TaTi_xO_y$ with NH_3 interface layer.

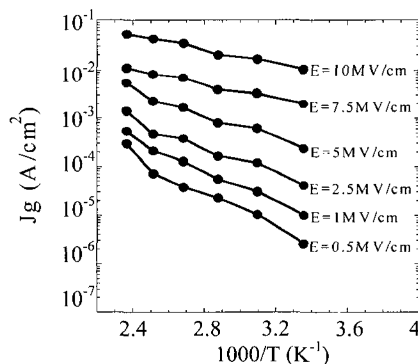

Fig. 16. Temperature dependence of leakage current of $TaTi_xO_y$ with NH_3 interface layer.

IV. CONCLUSIOIN

Recent results suggested that doping Ta_2O_5 with a small amount of TiO_2 using standard ceramic processing techniques can increase the dielectric constant of Ta_2O_5 significantly. In this paper, this concept is studied using RTCVD. Ti-doped Ta_2O_5 films are deposited using $TaC_{12}H_{30}O_5N$, $C_8H_{24}N_4Ti$, and O_2 on both Si and NH_3-nitrided Si substrates. An NH_3-based interface layer at the Si surface is used to prevent the interfacial oxidation during the CVD process and post deposition annealing is performed in H_2/O_2 ambient to improve film quality and reduce leakage current. A sputtered TiN layer is used as a diffusion barrier between the Al gate electrode and the $TaTi_xO_y$ dielectric. XPS analyses confirm the formation of $(Ta_2O_5)_{1-x}(TiO_2)_x$ composite oxide. High quality $TaTi_xO_y$ gate stack with EOT=7Å and the leakage current Jg=0.5A/cm^2 @ Vg=-1.0V has been achieved. We have also succeeded in forming $TaTi_xO_y$ composite oxide by RTP oxidizing as-deposited TaTi films. The electrical properties and Jg-EOT characteristics of these composite oxides are remarkably similar to that of RTCVD Ta_2O_5 suggesting that dielectric constant of Ta_2O_5 is not affected by the addition of TiO_2.

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The biography and photograph of Mr. Senzaki is not available.

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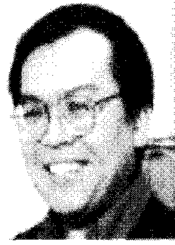

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