A High Density MIM Capacitor in a Standard CMOS Process

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Abstract— **A simple metal-insulator-metal (MIM) capacitor in a standard 0.25 μm digital CMOS process is described. Using all six interconnect layers, this capacitor exploits both the lateral and vertical electrical fields to increase the capacitance density (capacitance per unit area). Compared to a conventional parallel plate capacitor in the four upper metal layers, this capacitor achieves lower parasitic substrate capacitance, and improves the capacitance density by a factor of 4. Measurements and an extracted model for the capacitor are also presented. Calculations, model and measurements agree very well.**

Index Terms – **Capacitors, MIM devices, Device modeling, Integrated circuit modeling, CMOS integrated circuits.**

I. INTRODUCTION

The capacitor is one of the fundamental circuit elements for integrated circuits. Capacitors are used extensively in many applications such as analogue filters, switched capacitor circuits, data-converters, sample and hold circuits, and radio frequency (RF) circuits. The metal-insulator-metal (MIM) capacitor offers high linearity, high Q, and low temperature dependency [1][2][3]. These are all highly desirable features in many applications. The main problem with the MIM capacitor is that it occupies a considerable area. To alleviate this problem, some process technologies offer the option of thin insulator capacitors to achieve high-density MIM capacitors [1][4]. Such extra process steps are, however, associated with higher cost, and are not generally available. Modern digital CMOS processes offer more and more interconnect layers to fully exploit the potential for high gate density. This opens the possibility of more dense MIM capacitors using standard interconnect layers. Another important observation to make is that the minimum lateral spacing of metal layers reduces with scaling, whereas the vertical spacing stays relatively constant [2]. In future technologies, capacitors exploiting lateral fields may thus gain increased density both by reduced lateral metal spacing and increased number of metal layers. Traditional parallel plate capacitors gain only from increased number of metal layers.

This letter introduces a high-density MIM capacitor using a simple structure, that can be built in a standard CMOS process using interconnect layers. The capacitor exploits both lateral and vertical electrical fields, to achieve high density, and has electrical characteristics similar to those of conventional parallel plate capacitors. Section II describes the capacitor structure and a simple approximation to estimate the capacitance is presented. Section III presents on-wafer measurement results and an extracted model.

II. THE MIM CAPACITOR STRUCTURE

A prototype MIM capacitor has been implemented in a 0.25 μm digital CMOS process with six interconnect layers denoted M1 to M6. M1 and vias are tungsten, whereas M2 to M6 is aluminum material. The lower four metal layers, M1 to M4, have a thickness of 0.6 μm, and the upper two metal layers, M5 and M6, have a thickness of 1.0 μm. The minimum lateral metal spacing, d_f, is 0.4

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μm for M1 to M4, whereas it is 1.0 μm and 1.8 μm for M5 and M6 respectively. The vertical metal layer spacing, d_l, is 0.9 μm between all layers, and the distance from M1 to the substrate, d_{ox}, is 1.35 μm. The principle of the MIM capacitor structure is illustrated in Fig. 1 and Fig. 2.

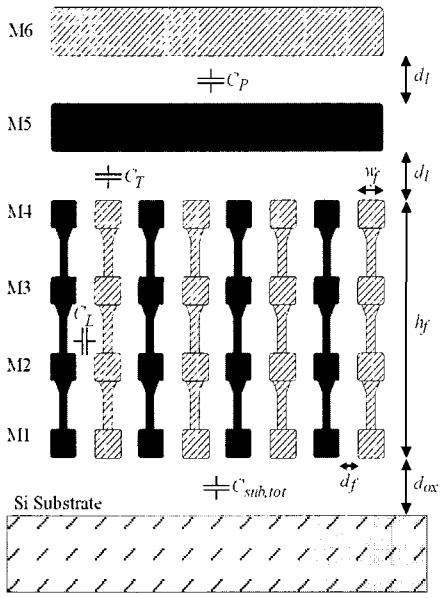

Fig.1. Cross section of the proposed MIM capacitor structure.

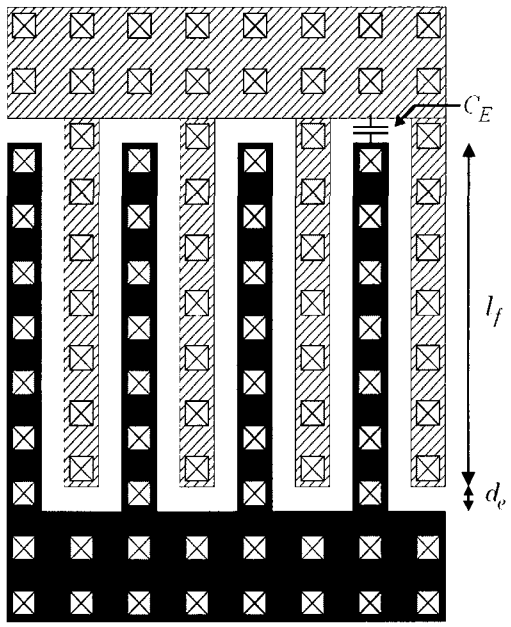

Fig. 2. Top view of the MIM capacitor structure, showing the interdigitated structure. Metal layers 5 and 6 are not shown.

In the lower four metal layers, the low lateral spacing is exploited. The metal strips and interconnecting vias forms perforated vertical plates, which are used as fingers in an interdigitated structure as shown in Fig. 2. The perforated plates do not give as high capacitance as solid plates, but due to fringing fields around the holes, it is expected that the capacitance is only slightly less. The thicker metal layers M5 and M6, have too wide minimum lateral spacing to be efficient in such a structure. M5 and M6 are thus used to form a conventional parallel plate capacitor. For a simple approximation of the capacitance, four contributions are recognized, as indicated in Fig. 1 and Fig. 2. These are: (i) C_L is the capacitance between two adjacent fingers in the vertical plate structure; (ii) C_E is the end capacitance of each of the fingers; (iii) C_P is the total parallel plate capacitance of the capacitor in M5 and M6; and (iv) C_T is the top capacitance for each finger of opposite polarity to M5. Assuming the vertical plates to be solid and neglecting fringing and corner fields, the four capacitance contributions may be approximated as:

$$C_L \approx \frac{h_f \cdot l_f}{d_f} \cdot \varepsilon_{ox}; \qquad C_E \approx \frac{h_f \cdot w_f}{d_e} \cdot \varepsilon_{ox}$$
$$C_T \approx \frac{l_f \cdot w_f}{d_l} \cdot \varepsilon_{ox}; \qquad C_P \approx \frac{A_P}{d_l} \cdot \varepsilon_{ox} \tag{1}$$

where ε_{ox} is the inter-metal oxide permittivity. The total capacitance of the MIM capacitor is given by:

$$C \approx (N_f - 1) \cdot C_L + N_f \cdot C_E + \frac{N_f}{2} \cdot C_T + C_P \tag{2}$$

which assumes an even number of fingers N_f. Similarly, a simple estimate of the total parasitic capacitance to the substrate can be found as:

$$C_{sub,tot} \approx \frac{A_C}{d_{ox}} \cdot \varepsilon_{ox} \tag{3}$$

where A_C is the total area occupied by the capacitor and d_{ox} is the distance from M1 to the substrate.

III. Results And Discussion

A prototype capacitor having N_f = 30 fingers, a finger width of w_f = 0.6 μm, a finger length of l_f = 30.8 μm, a finger height h_f=5.1 μm, and a parallel plate area of

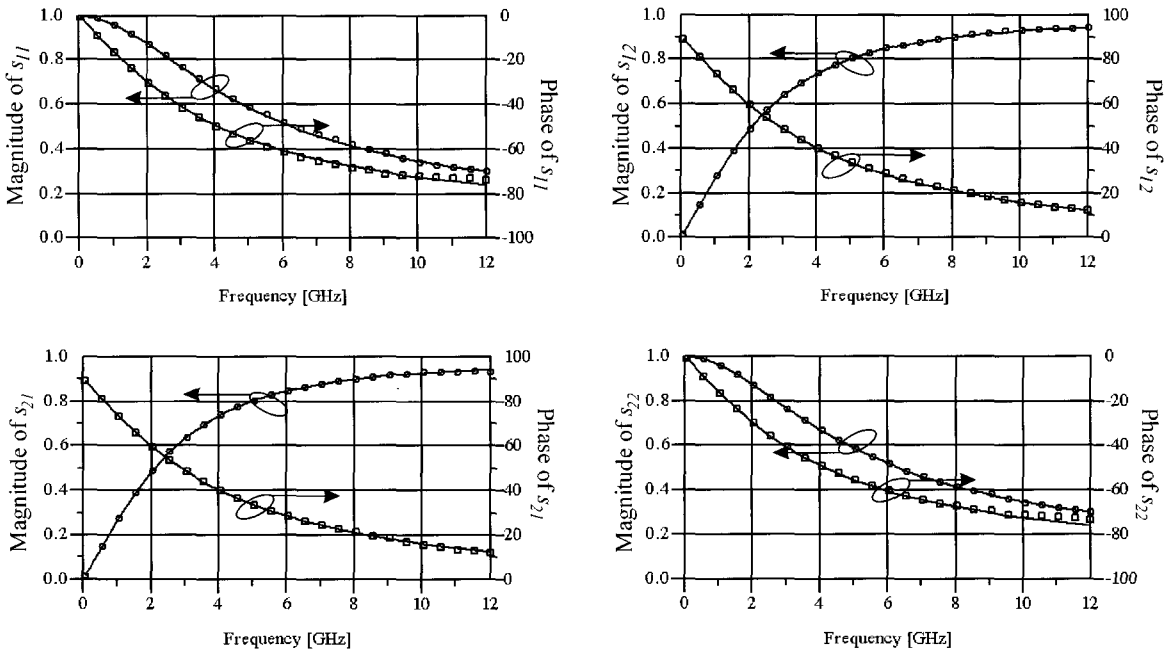

Fig. 3. Measured and modeled s-parameters. Solid line is modeled data.

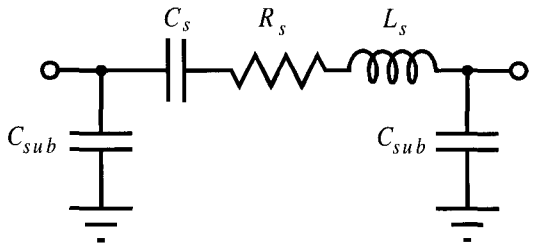

Fig. 4. Equivalent circuit model of the capacitor. The extracted model parameters are: C_s = 0.44 pF, R_s = 1 Ω, L_s = 40 pH, and C_{sub} = 12 fF.

A_P=841 μm^2 has been designed in the aforementioned process. Lateral metal spacing is d_f= d_e = 0.4 μm, and the relative permittivity of the inter metal oxide is 4 and therefore ε_{ox} = $4\varepsilon_0$ = 3.54X10^{-11} F/m. The capacitor occupies a total area of A_C = 1035 μm^2. Using (1), (2) and the mentioned process data the approximated capacitance of the capacitor is 0.46 pF, giving a density of 0.44 fF/μm^2. Only 9.6 % of this capacitance is contributed by the M5 and M6 layers, i.e. by C_P and C_T. If for some reason it is found advantageous not to use M5 and M6, these can be omitted, leading only to a slight reduction of density to 0.4 fF/μm^2. Using (3), the total parasitic capacitance to the substrate is estimated to be 27 fF. For characterization, the prototype has been placed in a series configuration in a shielded test fixture for high frequency on-wafer measurements [5]. Measurements are performed using an HP8510 network vector analyzer and Cascade ACP40 probes. De-embedding is performed using the four-step method described in [6]. The de-embedded *s*-parameters are shown in Fig. 3, and used for extraction of the equivalent circuit model in Fig. 4. The model is valid up to 12 GHz, and the calculated response is shown with solid lines in Fig. 3. The extracted capacitance is 0.44 pF, compared to the approximated value using (1) and (2) of 0.46 pF. Using the extracted capacitance the density is 0.43 fF/μm^2. The series resistance is 1 Ω, resulting in a Q of about 180 at 2 GHz which is in the range typically achieved for MIM and thin insulator capacitors. The series inductance is 40 pH, and yields a series resonance

frequency well above the range of the measurements. The total parasitic capacitance to the substrate is 24 fF compared to the estimated 27 fF, and giving a ratio of parasitic to fundamental capacitance of only 5.5 %. For comparison, a conventional parallel plate capacitor has been implemented in the same process. To achieve low parasitic capacitance to the substrate only metal layers M3-M6 have been used. This capacitor achieves a density of 0.10 fF/μm^2, a ratio of parasitic to fundamental capacitance of approximately 9 %, and otherwise comparable electrical characteristics. Using all six metal layers it is estimated that a density of 0.17 fF/μm^2 is achievable. The ratio of parasitic to fundamental capacitance would however be around 15%. Special thin insulator capacitors, requiring additional process steps, achieve capacitance density values around 0.7 to 1 fF/μm^2 [1][4]. The fractal capacitor described in [2] achieves a density of 0.23 fF/μm^2, this however, in a process with a minimum lateral spacing of 0.6 μm. With 0.6 μm lateral spacing the capacitor structure described in this letter is estimated to achieve a similar 0.25 fF/μm^2.

IV. Conclusion

In this letter a simple high density MIM capacitor structure for a standard CMOS process is proposed and evaluated. Due to the smaller area a further advantage of this capacitor is reduced parasitic capacitance to the substrate. A prototype capacitor is implemented in a 0.25 μm CMOS process with six metal layers and minimum lateral metal spacing of 0.4 μm. This capacitor achieves a density of 0.43 fF/μm^2 and a low total parasitic capacitance to the substrate of only 5.5 % of the main capacitance. A simple 5 component model shows excellent agreement with measurements in the frequency range up to 12 GHz.

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