Integration Process and Reliability for $SrBi_2Ta_2O_9$-based Ferroelectric Memories

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Abstract— **Highly reliable packaged 64kbit ferroelectric memories with 0.8 μm CMOS ensuring ten-year retention and imprint at 125 °C have been successfully developed. These superior reliabilities have resulted from steady integration schemes free from the degradation, due to layer stress and attacks of process impurities. The resent results of research and development for ferroelectric memories at Hynix Semiconductor Inc. are summarized in this invited paper.**

Index Terms — **thermal stress, moisture, hydrogen, reliability, FeRAM, imprint, retention, ferroelectric, 1T/1C, 2T/2C**

I. Introduction

Ferroelectric random access memories (FeRAM) have attracted attention due to their superior low-voltage and high-endurance operations to non-volatile flash memories, and also their fast operation matched for static random access memories. However, one of crucial issues for realization of the commercial FeRAM has been the reliability (especially, retention and imprint) at high temperatures that should be upgraded. For the reliability on the level of FeRAM commercialization, integration processes causing electrical degradation such as RIE, interlayer dielectrics, passivation, and packaging should be optimized. In conjunction with the degradation, the control of layer stress and process impurities such as moisture and hydrogen is most critical. However, there have not been proposed yet the methodology to protect completely ferroelectric capacitors from the degradation during full integration up to packaging. The resent results addressing the critical issues of research and development for ferroelectric memories at Hynix Semiconductor Inc. are summarized in this invited paper. In view of process integration, the important issues, the thermal stress and impurity effects of the inter-level dielectric layer on the ferroelectric performance of integrated Pt/SBT/Pt capacitors, are addressed. The hydrogen barrier technologies, imperative during especially passivation and packaging processes, are also discussed. In regard with the reliability of the ferroelectric memories, the retention characteristic of FeRAM related with imprint degradation of ferroelectric capacitors at high temperature is evaluated on the level of 8" wafer. Both cell configurations of 2T/2C and 1T/1C are discussed in terms of imprint reliability. General reliability items of the FeRAM after TSOP-I type package, such as fatigue endurance, early failure rate (EFR), humidity acceleration stress test (HAST), and temperature cycle (TC), are also evaluated.

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II. Device Fabrication And Key Issues For Commercial Memories

There have been considerable efforts for comercialization of ferroelectric random access memories using two types of ferroelectric materials. For the reliability on the level of FeRAM commercialization, the selection of ferroelectric films is most essential. The lead zirconate titanate perovskite system (PZT family) has an advantage of low temperature during process integration.

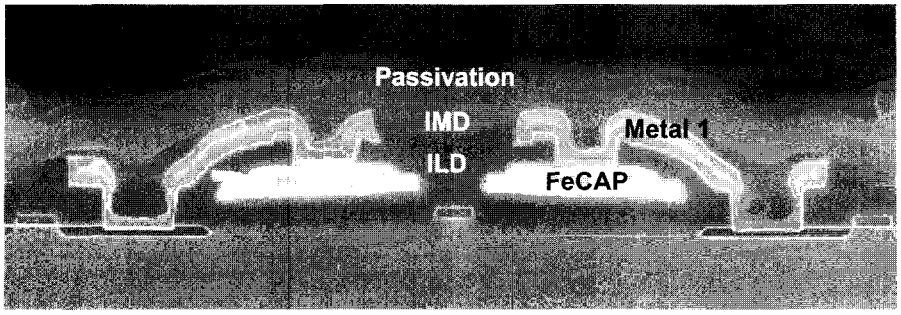

Figure 1. SEM photograph of cross-sectional structure of a fully integrated 64kbit cell with 1 poly, 2 metal, and CUB structure.

Table I Main Features of Integration Processes

0.8 μm CMOS Front-end	1. Isolation/Well 2. Vth implantation 3. Gate formation: Wsix + poly-Si electrode 4. Interlayer dielectric deposition
FeRAM Back-end	1. Capacitor formation; - Stack: Ti/Pt/SBT/Pt - SBT: 200nm by spin-coating using MOD Crystallization annealing @ 800 °C 2. Patterning: RIE using Cl_2 + CF_4 + Ar gases 3. Capacitor level dielectric layers: TEOS/BPSG by APCVD 4. Metallization: Ti/TiN/Al by sputtering 5. Hydrogen Barrier: Alumina film by ALD 6. Inter-metallic dielectric layers: SOG base 7. Passivation: USG/SiN by PECVD
Packaging	1. PIX 2. Back Grinding & Inking 3. Assembly; - Molding using plastic compound - Post molding curing @ 175 °C / 6 hr.

In case of layered perovskite based on strontium bismuth tantalate (SBT), simple Pt electrodes could be applied without the polarization loss due to fatigue. However, it was recently reported that BLT thin films using Pt electrodes were free from fatigue [1]. The electrical properties of the reported BLT films by a pulse laser deposition should be further optimized for the level of commercialization. The device performance and features using the BLT-based capacitors, which were recently optimized on the level of commercialization by our research team, were reported at the IEDM, which will be opened in this year [2]. The key process is on the randomly oriented crystallization by noble bake treatments to obtain high polarization and excellent reliabilities at low crystallization temperatures less than 650 °C, compared to $SrBi_2Ta_2O_9$ (SBT) films [3,4] with 800 °C. The remnant polarization of the BLT capacitors is about 60 % larger than that of SBT, and furthermore the BLT films have the coercive voltages less than the SBT films. One of advantages for the BLT over PZT films is the simplicity of cell schemes. For examples, BLT capacitors do not require such the complicate barriers in capacitor level dielectrics (CLD) as preventing PZT films from chemical interactions with dielectrics. Additionally, the BLT capacitors are not fatigued with Pt electrodes, while PZT films require the complicate metal-oxide electrodes to overcome the endurance. In this paper, the recent results for the SBT-

based ferroelectric memories are summarized. In view of process integration, the device fabrication is not basically different from others, regardless of the capacitor materials.

The 64K bit FeRAMs with 2T/2C and 1T/1C configurations have been successively fabricated with standard 0.8μm CMOS process, capacitor process of Pt/SBT/Pt, double level metalization, and Si_3N_4 passivation process. The SEM photograph showing the cross-sectional view of a fully integrated FeRAM cell is presented in Fig. 1. The fabrication sequences for the SBT-based ferroelectric memories are summarized in Table I. The cell area and ferroelectric capacitor area are about 50μm^2 and 9μm^2, respectively. For reliability tests, the FeRAM chips were packaged in TSOP-I type package. The ferroelectric SBT layers were formed on $Pt/TiO_2/SiO_2/Si$ substrates by a sol-gel spin coating technique.

The bottom and top Pt electrodes were deposited using a dc magnetron sputtering. After the formation of capacitors, an ILD layer was covered over capacitors. First metal layers, used for connecting the top electrodes to active areas of transistors, consist of TiN/Al/TiN/Ti stacks. After the fabrication of first metal lines, IMD layers were deposited with SiON and spin-on-glass (SOG) SiO layers. The IMD layers were used for flattening. After the deposition of IMD layers, the second metal lines, followed by passivation and packaging processes, were formed.

Compared to other devices in view of an integration process, one of the advantages of ferroelectric memories is the similarity of integration schemes with the well-developed DRAM. Except for the capacitor formation, other processes may be done in the almost same fashion as the conventional DRAM process.

Thus, the conventional and well-developed processes provide cost effective schemes for ferroelectric memories. However, the electrical properties of the ferroelectric capacitors, compared to the usual capacitors in DRAM, are significantly degraded depending on the integration processes. The integration processes causing electrical degradation such as RIE, interlayer dielectrics, passivation, and packaging should be optimized for the commercialization of ferroelectric memories. In conjunction with the degradation, the control of thermal stress in each layers near ferroelectric capacitors with different thermal properties under the dramatic thermal budget is important for the retardation of electrical degradation of ferroelectric capacitors during the integration processes. Furthermore, optimal control of process impurities such as moisture and hydrogen during the ILD, IMD, passivation as well as packaging processes is most critical. However, there have not been proposed yet the methodology to protect completely ferroelectric capacitors from the attack of the thermal stress and impurities during full integration up to packaging. In next section, integration schemes for the solution are proposed.

III. Optimization Of Thermal Stress

In relation to the capacitor formation, the top Pt electrodes were patterned to a square shape to define the capacitor area, whereas the bottom Pt and SBT layers were patterned to the strip shape. Therefore, the ILD layer laterally intervenes the bottom Pt and SBT layers as well as the top Pt electrodes. As described in Table I, there are four annealing steps; the first at 800 °C is for the crystallization of the SBT layer, the second at 700 °C is to recover the etching damage generated by capacitor patterning, and the third at 800 °C is to make the ILD layer dense and for better recovery of the etching damage. During the third annealing step, the capacitor stack, especially the Pt layers, suffers a serious thermal stress due to thermal expansion mismatch between the Pt layer, Si substrate, and ILD SiO_2 layer. To test the effect of the ILD layer on the ferroelectric performances of the capacitor, two different ILD materials were tested: un-doped SiO_2 glass (USG) using TEOS, grown at 650 °C by low-pressure CVD, and BPSG using trimethylboron, trim-ethylphophorus, TEOS, and ozone, grown at 400 °C by atmospheric-pressure CVD. Some of the ILD samples have a combination of the two layers. The fourth annealing step at 700 °C is for curing the damage imposed by contact hole etching. The top electrode sizes were varied from 2x2 μm^2 to 20x20 μm^2 while maintaining the total top electrode area as 20,000 μm^2 to test the size effect on the ferroelectric performances. The bottom strip width was accordingly varied with variations in top electrode size.

Figures 2 (a) and 2 (b) show the *P-V* hysteresis loops and *J -V* curves of array capacitors having two different

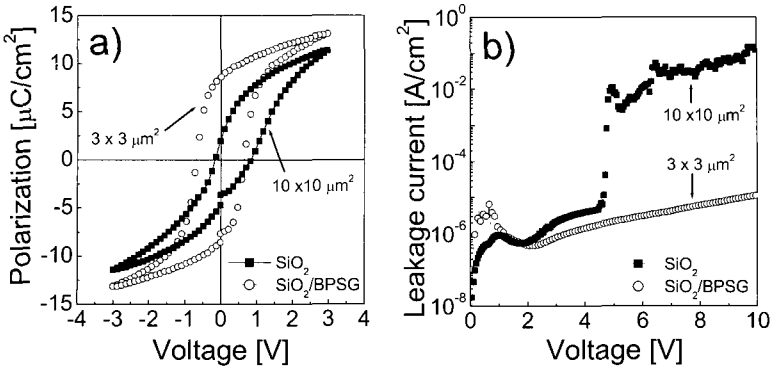

Fig. 2. (a) P-V hysteresis loops and (b) J-V curves of the array capacitor that has 500-nm-thick USG and 50-nm-thick USG/500-nm-thick BPSG layers, respectively, as the ILD.

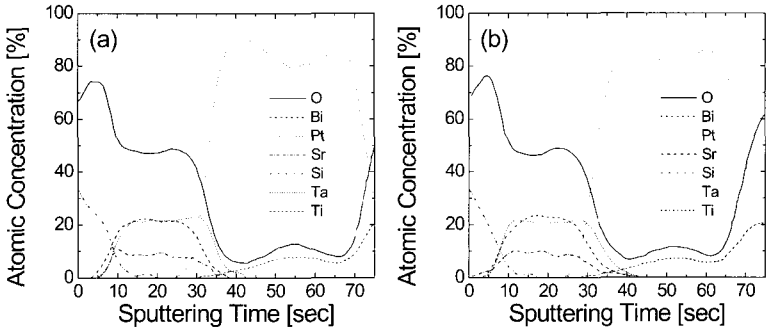

Fig. 3. AES depth profiles of the USG/SBT/Pt/Ti/SiO2/Si stacked layers (a) before and (b) after the ILD annealing at 800 ℃.

ILDs. There are two hysteresis loops from the two different ILDs in Fig. 2 (a). A good hysteresis loop was obtained from the 3x3 μm^2 capacitor array having a composite ILD layer composed of 50-nm-thick USG and 500-nm-thick BPSG. Al-though it is not included in this figure, all the hysteresis loops obtained from other sized capacitor arrays, from 2 x2 μm^2 to 20x20 μm^2, with the same ILD layer had al-most the same shapes. However, the capacitor arrays having a 500-nm-thick USG ILD showed distorted hysteresis loops with a severe imprinting behavior. The distorted loop shown in Fig. 2 (a) was obtained from the 10x10 μm^2 capacitor array. When the capacitor size was smaller than this, almost all of the capacitors short circuited. It can be clearly understood that the ILD composed of only USG greatly increases the short-fail probability. The failure rate also increases with de-creasing capacitor size. The BPSG ILD produces a very reliable ferroelectric behavior of the capacitor array irrespective of size. For the case of USG/BPSG double layer, the failure probability increased with increasing USG thickness. However, up to 50-nm-thick USG, all the capacitors are good enough. The reason for using a thin USG layer between the thick BPSG ILD and capacitor is to alleviate the possibility of B or P diffusion from the BPSG layer to the capacitors.

The direct reason for the cases of USG ILD for the failure is the increased leakage current, as shown in Fig. 2 (b). To determine whether an interfacial reaction or interdiffusion between the USG and SBT layers during annealing at 800 °C causes the large leakage, Auger electron spectroscopy analysis was performed. Figures 3 (a) and 3 (b) show that there is little difference in the AES depth profiles of the USG/SBT/Pt/Ti/SiO_2/Si stacked layers before and after annealing. Therefore, it is not plausible to assume that the in-creased leakage current is due to a chemical reaction between the USG and SBT films.

Figures 4 (a) and 4 (b) show bright field cross-section TEM micrographs of an integrated SBT capacitor having a dimension of 3x3 μm^2 with a USG ILD after the third an-nealing at 800 °C. The figures were obtained from two different areas of the capacitor. It can be clearly seen

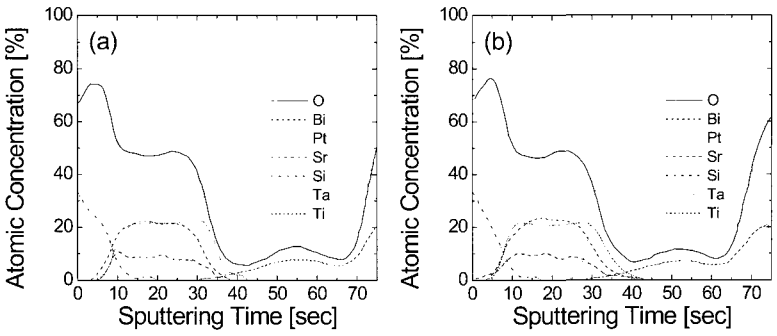

Fig. 3. (a) AES depth profiles of the USG/SBT/Pt/Ti/SiO2/Si stacked layers (a) before and (b) after the ILD annealing at 800 ℃.

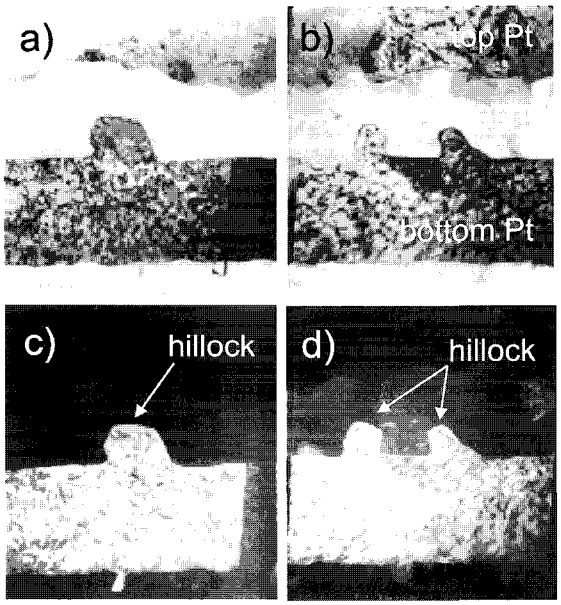

Fig. 4. (a), (b) Bright field cross-sectional TEM micrograph of the integrated SBT capacitor having a dimension of 3 x 3 ㎛2 with USG ILD after the annealing at 800℃, and (c), (d) corresponding dark field images obtained from the 111 diffraction spot.

that the bottom Pt generates hillocks into the SBT layer. Figures 4 (c) and 4 (d) are the corresponding dark field images obtained with a Pt111 diffraction spot clearly revealing that the protruded region is Pt hillock. Before the ILD annealing process, these types of hillocks were not observed by extensive scanning electron microscopy as well as TEM analyses. Therefore, it is quite certain that these hillocks are formed during the ILD annealing step.

It can be assumed that the reason for the increased leakage and short-failure probability of the capacitor arrays having USG ILD is hillock formation on the bottom Pt electrode during the ILD annealing step at 800 °C. From the array structure of the capacitors, it might be expected that the Pt layer could be subjected to serious

compressive stress by the large thermal expansion of the Pt layer when the laterally intervening ILD does not con-tract at all during the high temperature annealing step. Therefore, an investigation into the contraction behavior of the USG, BPSG and USG/BPSG combination layers was necessary. Figure 5 shows the variations of the stresses in the USG, BPSG, and combined layers with increasing temperature up to 800 °C. For the tests, the different layers were deposited on bare Si wafers with the same thickness ~500 nm.

The USG layer shows very little stress over the entire

temperature range with negligible hysteresis behavior. Because the stress was measured by the wafer curvature method, it implies that the film shows very little expansion or contraction during the heating and cooling stages, respectively. However, the BPSG and BPSG containing films show a large tensile stress during heating but a negligible stress during cooling. The tensile stress increases with the increasing portion of the BPSG layer thickness. It should be noted that the tensile stress increases with temperature up to about 450 °C, then decreases. At 800 °C all the films show almost the same small stress.

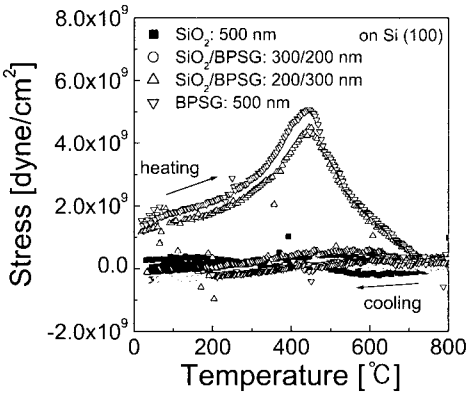

Fig. 5. Variations of stresses of the USG, BPSG and combined layers with temperature up to 800℃.

Considering the stress behavior shown in Fig. 5, it can be understood why the BPSG ILD suppresses hillock formation in the Pt electrodes. During the ILD annealing at 800 °C, the intervening BPSG layer between the Pt electrodes con-tracts by removing impurities, allowing easier thermal expansion of the Pt layer. The easier expansion results in the smaller compressive stress in the Pt layer and thereby less hillock formation.

Therefore, the smaller electrode is under a much larger hydrostatic stress compared to the larger electrode, which results in a larger probability for hillock formation. These results correspond very well to increased failure rate with decreasing electrode size. From the considerations on stress distribution, the optimum ILD was determined to be a composite layer comprised of a 50-nm-thick USG and a 500-nm-thick BPSG. Even though the single layer BPSG also does not impose a serious stress to the SBT capacitor, the leakage current characteristics of the array capacitor having a single layer BPSG ILD was inferior to that of the array capacitor having the optimum ILD.

Figures 6 (a) and 6 (b) show the *P-V* and *J -V* curves of the array capacitors having different unit capacitor sizes with the optimum ILD layer. The *P-V* curves are almost the same, whereas the *J-V* curve of 2x2 μm^2 capacitor array shows slightly greater leakage characteristics compared to those of the larger capacitor arrays. However, the current density level at the operation voltage (~3V) is low enough for the stable operation of the FeRAM devices.

In summary, an optimization study of the ILD process for the integrated ferroelectric SBT capacitor array was performed. It was found that the compressive stress imposed on the Pt electrode by thermal expansion during the ILD annealing at 800 °C was the crucial factor determining the capacitor yield. When the compressive stress is excessive, the Pt electrodes form hillocks into the SBT layer resulting in a large leakage current, which eventually short circuits. This behavior becomes more serious when the pattern size decreases due to the increase in stress level. The major cause of the

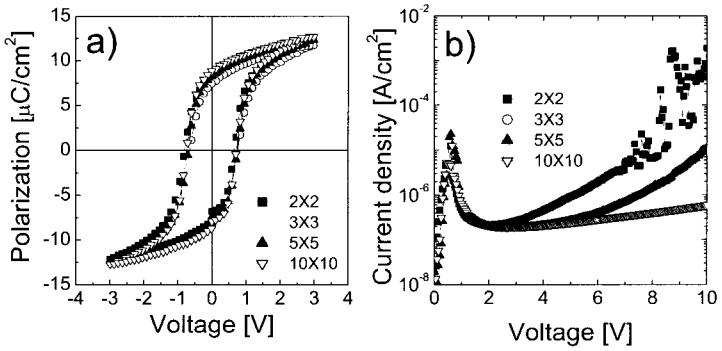

Fig. 6. (a) P - V and (b) J - V curves of the array capacitors having different unit capacitor sizes with the optimum ILD layer.

compressive stress evolution during heat treatment is the rigidity of the ILD material that laterally intervenes between the capacitors. Therefore, the adoption of BPSG as the ILD, which contracts during the ILD annealing by removing impurities, greatly reduces the thermal stress level and suppresses hillock formation [5]. With the optimum combination of a 50-nm-thick USG and a 500-nm-thick BPSG, the integrated capacitors showed excellent *P-V* and *J-V* characteristics down to a unit capacitor size of 2x2 μm^2.

IV. Optimal Control Of Process Impurities

The electrical degradation of ferroelectric capacitors, which is induced by the damage, is caused by integration processes such as reactive ion etching (RIE), interlayer dielectrics, passivation, and packaging. Among the processes discussed above, hydrogen barrier is one of most important issues to be addressed for realization of commercial ferroelectric memories [6-8]. Metallic (Ti films) [9] and ceramic (Al_2O_3) [10] hydrogen barriers have been recently reported. The metallic interconnection including Ti layers can be used as a hydrogen barrier without additional dielectric layers. However, specific conformal coatings of the capacitor by the barrier layer and intermediate insulation layer are required for the metallic hydrogen barriers to prevent hydrogen attack of the ferroelectric layer. Thus, metallic hydrogen barriers may be restrictively used for low-density memories. On the other hand, ceramic hydrogen barriers do not require the additional dielectrics for electrical isolation and can be optionally located in any sites such as capacitor level dielectrics, metal lines, or inter-metallic dielectrics. This flexible integration-scheme makes ceramic barriers more useful for high-density memories. Regarding the electrical degradation of ferroelectric capacitors on integration process, there have been several reports on effects of H_2 mixtures for forming gas treatment [11] and ionized hydrogen during passivation [9]. However, effects of hydrogen and moisture on the properties of dielectric layers of capacitors need further studies. In this letter, we report on results of a systematic investigation of the effect of impurities on the properties of the dielectric layer of ferroelectric capacitors and how hydrogen barriers (Ti and Al_2O_3 films) can help overcome these problems during integration process.

Results of electrical measurements for these memories before and after the passivation processes are represented in Fig. 7. The RIE processes for the capacitor and the contact formation were followed by annealing at 700 °C and O_2 ambient for 30 minutes. This treatment was sufficient to recover the RIE-damaged electrical properties. However, the dielectric deposition degraded little the electrical properties of capacitors. The thermal reaction during the dielectric deposition produces nearly molecular hydrogen or hydrogen compounds such as H_2O, C_2H_5OH, and $(C_2H_5)_2O$ [12]. Thus, it is believed that the electrical degradation was not significant due to difficult penetration of molecular hydrogens with thermal energy. On the other hand, the passivation processes significantly degraded the electrical properties. Switching polarization is significantly reduced (Fig. 7(b)). The leakage current measurements (Fig. 7(a)) also indicate leaky properties of the capacitors. It is expected that the passivation

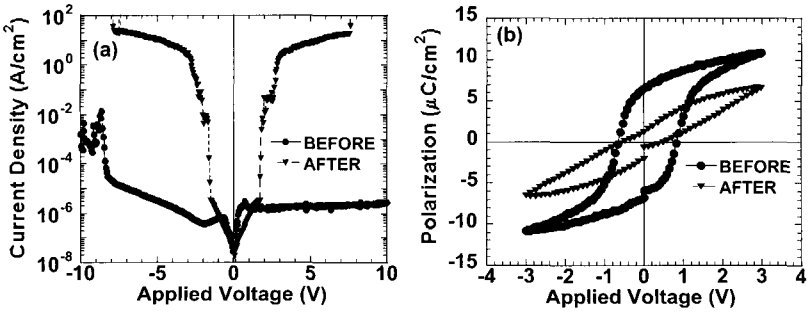

Fig. 7. Leakage current density (a) as a function of applied voltage and hysteresis loops (b) measured at 3V for integrated memories without hydrogen barriers before and after the passivation process.

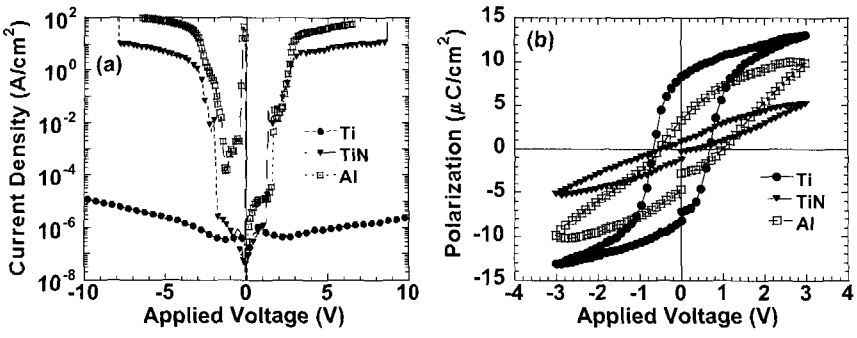

Fig. 8. Leakage current density (a) as a function of applied voltage and (b) hysteresis loops measured at 3V for passivation-processed memories, using candidate hydrogen barriers (Ti, TiN, and Al films).

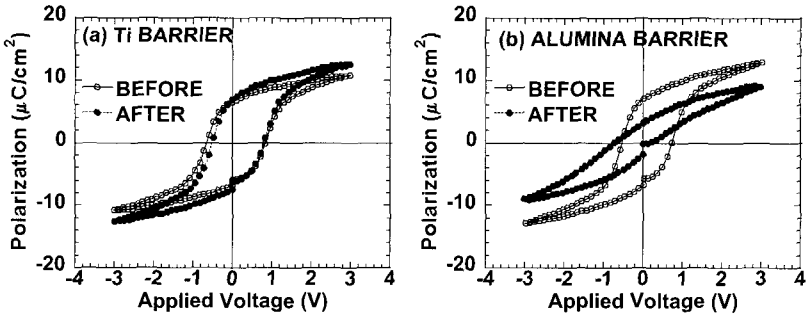

Fig. 9. Hysteresis loops for 2K-array capacitors integrated with the hydrogen barriers, (a) Ti and (b) Al_2O_3, on non-annealed dielectrics (SiO) before and after passivation.

deposition enhanced by the plasma produces significant amount of atomic hydrogen with high energy [13], resulting in easy penetration and the serious damage to capacitors [14]. Consequently, the TEOS rather than the silane-based CVD sources and the APCVD without plasma is more desirable in terms of preventing the degradation.

Therefore passivation processes for the protection of capacitors from the atomic hydrogen damage were investigated using hydrogen barriers (Ti, TiN, and Al). Results of electrical measurements for capacitors integrated with these passivation processes are shown in Fig. 8. Ti films over 500Å were effective enough to protect the capacitors from the hydrogen damage. There is little difference in both hysteresis loop and leakage current measurements between before and after the passivation processes using the Ti film as shown in Fig. 7 and Fig. 8, respectively. On the other hand, TiN (1000Å) and Al (4000Å) layers were not effective to barrier the penetration of hydrogen. The significant decrease of 2Pr and the increase of leakage current are observed in the ferroelectric memories using these films (Fig. 8). These measurements are similar to the results (Fig. 7) for the memories processed the passivation without a hydrogen barrier. It was reported, however, that the TiN films effectively functioned as a hydrogen barrier for SBT capacitors [15]. We believe that this is mainly due to the different ambient of forming gas (mixture of H_2 and N_2) annealing from the passivation process (including the atomic hydrogen with high energy).

The motivation for this study originated from the observation of the electrical properties (Fig. 9) of the capacitors using the hydrogen barriers over the non-annealed dielectrics. In Fig. 9 (a), the tests on capacitors covered with a Ti hydrogen barrier show that the electrical properties were not degraded after passivation, regardless of the annealing process of the sub-dielectrics. However, the electrical properties of the capacitors with Al_2O_3 barriers were significantly degraded after passivation [Fig. 9 (b)]. The degradation of the capacitors after passivation depends on the annealing of

the dielectrics followed by the deposition of Al_2O_3 films as shown in Fig. 10. In Fig. 10, the polarization values of the capacitors after the deposition of Al_2O_3 barriers followed by passivation are normalized by the values before the deposition of Al_2O_3 films. The higher the annealing temperature, the less the degradation of the capacitors. Furthermore, the composition analysis by x-ray photoemission spectroscopy (XPS, Q2000) show negligible differences in the depth profiles of the dielectrics covered with Al_2O_3 (Fig. 11) as well as Ti barrier films, regardless of the annealing temperatures of the dielectrics. In view of these results, it was not clear at that time the reason for the different behaviors of the capacitors with Ti or Al_2O_3 barriers.

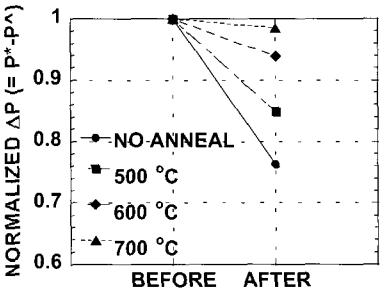

Fig. 10. Normalized polarization changes ($\Delta P = P^*$, switched - P^, nonswitched) for the capacitors fabricated using Al_2O_3 hydrogen barriers as a function of annealing temperature of the sub-dielectrics (SiO) up to 700 °C. The polarization values measured after passivation are normalized with those before the deposition of the hydrogen barriers on the sub-dielectrics.

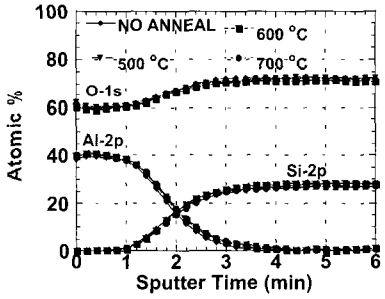

Fig. 11. XPS depth profiles for the stacks of Al_2O_3 barriers on sub-dielectrics (SiO) annealed up to 700 °C.

In view of the results shown above, systematic experiments were done using TDS and FTIR analyses to understand the underlying mechanisms responsible for the different behaviors. The desorption intensities of several gases such as CO_2, CO, CH_3, C, and O_2 in TDS analyses were negligible for all samples as the TDS temperature increased up to 600 °C. Thus, the desorption curves presented in Fig. 12 are only for H_2O (mass number, m/e = 18) and H_2 (m/e = 2) gases. The substrates under the dielectrics (SiO) were annealed at 800 °C for 1hr. before the deposition of the dielectrics. Thus, the desorbed impurities from the substrates could be negligible in TDS measurements. The results of the TDS analyses for the samples with only dielectrics (SiO) annealed at different temperatures are presented in Fig. 12 (a). As the annealing temperature of the dielectric (SiO) increases up to 700 °C, the amount of the desorbed H_2O from the SiO layer decreases as a function of the TDS heat-temperature. In the case of the samples with the stacks of Al_2O_3/SiO on the substrate, the curve similar to that of the sample with only SiO layer is shown as a function of increasing annealing temperature [Fig. 12(b)]. The H_2O peak intensities are observed at the TDS heat-temperature of around 410 °C, which is higher than the peak temperature of around 230 °C for the samples with only SiO layers. Passivation process followed from the deposition of hydrogen barriers was done at 350 °C. Thus, it is expected that most of the moisture and hydrogen in the SiO layers can not diffuse out through the Al_2O_3 films and remains in the state of high thermal energy during the passivation process. These impurities could easily arrive at the capacitors through weak paths such as contact via between the capacitors and metal lines or through the dielectrics covering the capacitors. The interaction of forming gas (mixture of H_2 and N_2) with the capacitors results in the formation of non-perovskite phases in the capacitors, consequently the electrical degradation of the capacitors [16-18]. Therefore, it is expected that the degree of the degradation in Fig. 10 is closely related to amounts of both H_2O and hydrogen in the dielectrics depending on the annealing temperature. For the samples of Fig. 12 (a), the quantified amounts of H_2O for the non-annealed and 700 °C-annealed samples are approximately 2.7×10^{18} and 3.7×10^{17} molecules/cm^2, respectively, which were measured using a quadruple mass spectrometer (QMS) attached in the TDS [see the label denoted by H_2O-SiO in Fig. 12 (d)]. The calibration of the QMS for the quantified measurements was done using standard samples with the known implantation dose of impurities on Si substrates. The method details on the quantitative calibration were reported elsewhere [19]. The amounts

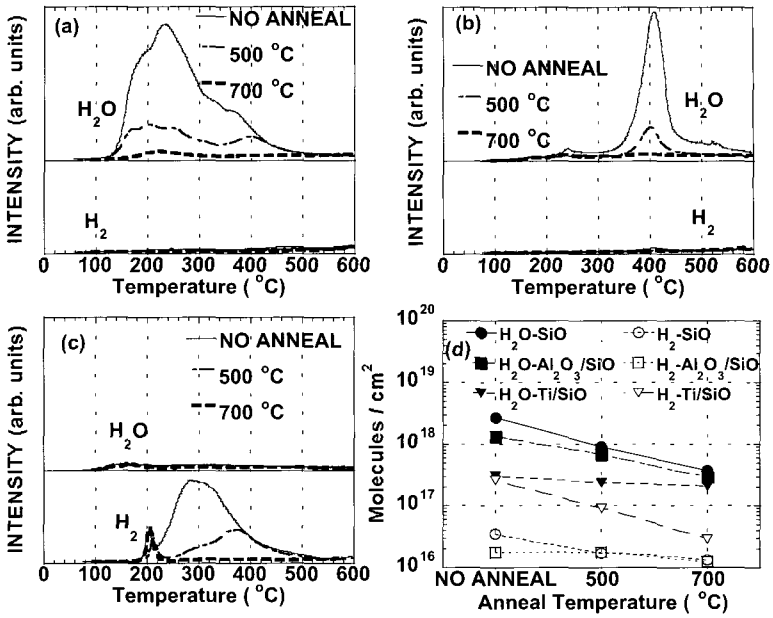

Fig. 12. TDS analysis as a function of temperature up to 600 °C for three samples, that is, (a) only dielectrics (SiO), (b) Al_2O_3 barriers on the dielectrics, and (c) Ti barriers on the dielectrics using the thermally oxidized Si wafers. The annealing treatments for the sub-dielectrics were done right before the deposition of the hydrogen barriers. (d) Quadruple mass spectrometer (QMS) measurement of H_2O and H_2 evolving from the three samples for TDS heating up to 600 °C.

of the H_2 for the non-annealed and 700 °C-annealed samples are approximately $3.5x10^{16}$ and $1.4x10^{16}$ molecules/cm^2, respectively [see the label denoted by H_2-SiO in Fig. 12 (d)]. These seven and two times larger amounts of H_2O and hydrogen, respectively, for the non-annealed sample compared to the 700 °C annealing are practically blocked by the Al_2O_3 barriers, resulting in around 22 % more degradation in electrical properties (Fig. 10).

The samples with Ti hydrogen barriers on dielectrics, on the other hands, showed different behaviors during the TDS measurements. Desorption intensities of H_2O are very low regardless of the conditions of annealing treatments [Fig. 12 (c)], compared to the Al_2O_3 samples. The differences in the quantified amounts of H_2O between the annealing conditions are negligible [see the label denoted by H_2O -Ti/SiO in Fig. 12 (d)]. However, desorption behaviors of H_2 are significantly depending on the annealing conditions [Fig. 12 (c)]. The intensities of the first H_2 peaks at the TDS heat-temperature of around 210 °C are almost the same, regardless of the annealing conditions, while the intensities of the second and third peaks at the TDS heat-temperatures of 280 °C and 380 °C, respectively, decrease as a function of increasing the annealing temperature. At this point, there are several mysteries, that is, why the amount of the H_2O is so small, near the temperature for which the highest intensity of the H_2 peak is observed and why the intensities of the second and third H_2 peaks depend on the annealing temperatures.

Therefore, in order to understand the abnormal behaviors of desorption gases, the bonding states of the H_2O and H_2 in the dielectrics immediately after the deposition of the hydrogen barriers or the dielectrics were investigated by FTIR analysis. The analysis results for the samples with only dielectrics are presented in Fig. 13 (a). As the annealing temperature increases, the intensities of the very broad peaks related to H_2O with the wave numbers ranging from 3200 to 3700 cm^{-1} decrease. The differences in the FTIR analyses between the samples with only dielectrics and with the Al_2O_3 barriers on dielectrics [Fig. 13 (b)] are small. These results correspond to the TDS analyses. However, the intensity of the broad H_2O peaks for the samples with Ti barriers on the dielectrics are negligibly regardless of the annealing conditions [Fig. 13 (c)]. The Ti films were deposited using DC magnetron sputtering. There were some reports regarding the effects of plasma treatments

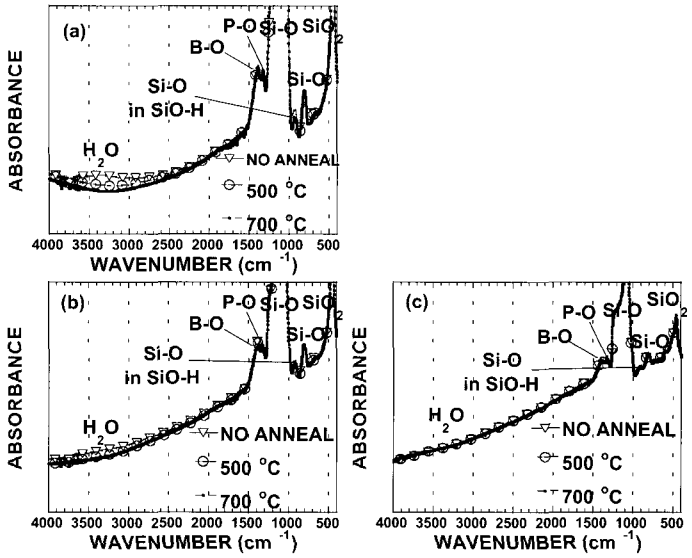

Fig. 13. FTIR analysis for three samples, that is, (a) only dielectrics (SiO), (b) Al_2O_3 barriers on the dielectrics, and (c) Ti barriers on the dielectrics using the thermally oxidized Si wafers.

on the elimination of the moisture in dielectrics [20-22]. Thus, it is expected that moisture in the dielectrics were removed during the deposition of the Ti films on the dielectrics, due to the interaction of the plasma with the moisture in the dielectrics. Furthermore, the Ti films with the strong tendency of absorbing hydrogen [9,23] also absorbed the hydrogen from the fragmented H_2O during the plasma interaction with the moisture in the dielectrics. The amount of hydrogen absorbed in the Ti layer for the non-annealed sample is approximately $2.2x10^{17}$ molecules/cm^2, which is obtained by subtracting the hydrogen content of SiO from that of the Ti/SiO stack [see the labels denoted by H_2-SiO and H_2-Ti/SiO in Fig. 12 (d), respectively]. The amount of the fragmented H_2O during the Ti deposition on non-annealed SiO layer is approximately $2.5x10^{18}$ molecules/cm^2, which is the difference of H_2O content between H_2O-SiO and H_2O-Ti/SiO in Fig. 12 (d). Thus, it is expected that approximately only 10 percent of the fragmented H_2O were contributed to the absorption of hydrogen in Ti layer, and the remainder was exhausted from the Ti deposition chamber. The possibility that the dielectrics absorb the hydrogen is small because the intensities of the peaks related to the SiO-H bonding in the FTIR curves are practically the same for the three samples (Fig. 13). Consequently the not-degraded electrical properties of the capacitors with Ti hydrogen barriers [Fig. 9 (a)], regardless of the annealing temperature of dielectrics, are due to the removed moisture in the sub-dielectrics and the absorbed hydrogen in the Ti barriers during the barrier deposition.

In summary, it is demonstrated that one of the most important factors on the process integration of the ferroelectric memories is the control of the impurities inside the dielectrics. The differences in the degradation behaviors of the memories using Ti from Al_2O_3 barriers originate from the interaction of the impurities in the dielectrics with the DC plasma and the blocking effects of the barriers, respectively.

V. Reliability Evaluation

In order to commercialize FeRAM, it is required to evaluate the reliability or lifetime of FeRAM exactly. One of the most fatal degradation mechanisms in FeRAM has been imprint of ferroelectric capacitors [24, 25]. Imprint is a voltage shift of the ferroelectric hysteresis curve, which occurs during high temperature storage (HTS) of ferroelectric capacitors with a specific polarization state. Imprint also results in a reduction of remnant polarization as a function of HTS time and temperature. Sensing signal margin in FeRAM for distinguishing DATA stored in cells is determined by the magnitudes of switching charge (Q_S), non-switching

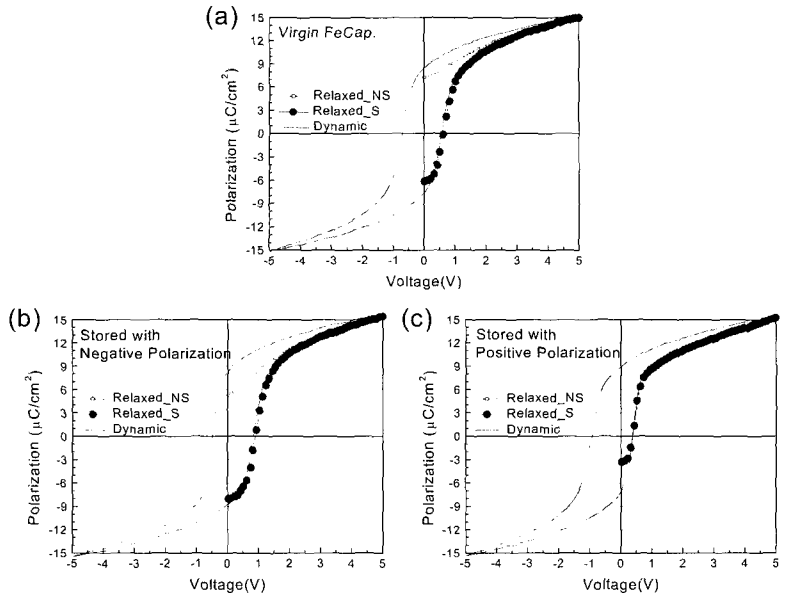

Fig. 14. Typical hysteresis curves of ferroelectric capacitors (a) before HTS, (b) after HTS with negative polarization state, and (c) after HTS with positive polarization state.

charge (Q_{NS}), and bit line capacitance (C_{BL}) [25]. Hence the reduction of remnant polarization leads to the reduction of the sensing signal margin. Consequently, the lifetime of FeRAM could be calculated from the imprint degradation of ferroelectric capacitors.

In this section, we report on imprint degradation rates of ferroelectric capacitors and FeRAM cells fabricated using 0.8μm CMOS technology with Pt/$SrBi_2Ta_2O_9$ (SBT)/Pt ferroelectric capacitors. By correlating those imprint degradation rates the lifetime of FeRAMs with 2-transistor and 2-capacitor (2T/2C) and 1-transistor and 1-capacitor (1T/1C) is estimated.

64K bit FeRAMs with 2T/2C and 1T/1C configurations have been fabricated with standard 0.8 μm CMOS process, capacitor process of Pt/SBT/Pt, double level metalization, and Si_3N_4 passivation process. Figure 1 shows a cross section view of the memory cell. The cell area and ferroelectric capacitor area are about 50μm^2 and 9μm^2, respectively. For general reliability test, the FeRAM chips were packaged in TSOP-I type package.

Measurements of ferroelectric properties were conducted with parallel 2048-array capacitors at 90 °C. Cell signals or bit line voltages (V_{BL}) during DATA READ [26] were measured by comparing cell DATA with externally supplied variable reference voltage from memory tester at 90 °C.

In order to induce the imprint to ferroelectric capacitors, some capacitors were polarized prior to HTS with positive polarization state (+P_R), and the other capacitors were polarized with negative polarization state (-P_R) at room temperature. In order to induce the imprint to FeRAM memory cells, some cells were written with DATA "1" and the other cells were written with DATA "0". Then the capacitors and devices were stored at 125°C and 175°C for cumulative time of 3, 6, 12, ..., 504, and 1008 hours, respectively. After each HTS step, ferroelectric properties of capacitors and V_{BL} distributions of memory cells were measured.

Figure 14 shows typical ferroelectric hysteresis curves of ferroelectric capacitors before (a) and after (b), (c) HTS. The capacitors before HTS show symmetric hysteresis. However, the capacitors after HTS show asymmetric hysteresis curves. The capacitor polarized with -P_R before HTS shows a negative voltage shift with a decrease in switching polarization (P_S), while the capacitor polarized with +P_R before HTS shows a positive voltage shift with an increase in non-switching polarization (P_{NS}). The variations in P_S of positively polarized capacitors (P_{S+}), and P_{NS} of negatively polarized capacitors (P_{NS-}) are linear in logarithm of HTS time and a function of HTS temperature, as shown in Figure 15. From the extrapolation of the change in P_{S-}

and P_{NS-}, the lifetime of a ferroelectric capacitor, which is defined by the time when the difference between P_{S+} and P_{NS-} is zero, could be extracted. It is about 2000 years for 125°C of the HTS temperature. If the HTS temperature is 175°C, it is reduced to about 1.1 year.

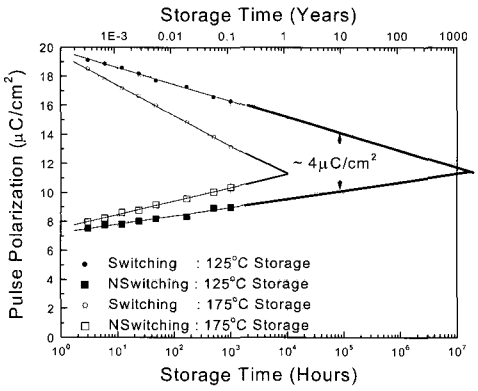

Fig. 15. Variations in switching polarization (P_S) of positively polarized capacitor (P_{S+}), and non-switching polarization (P_{NS}) of negatively polarized capacitor (P_{NS-}) as a function of time at 125°C and 175°C HTS.

Even though we can recognize the significant reduction in the difference between P_{S+} and P_{NS-}, it is difficult to pre-estimate when the FeRAM shows function failure due to the lack of sensing signal margin. From the above results, we can just say that the lifetime of the FeRAM is shorter than 2000 years if the HTS temperature is 125°C, and shorter than 1.1 year if that is 175°C The difference between the lifetimes of ferroelectric capacitor and FeRAM can be caused by the fact that an FeRAM needs a minimum sensing signal margin, larger than sense amplifier sensitivity, typically about 100mV, for reliable DATA READ operation. Moreover the ferroelectric properties usually obtained from ferroelectric tester are average properties of the array of the test structure, for example, 2048-array capacitors in this experiment. Therefore, the distribution of the properties in FeRAM cell capacitors is overlooked. In actual memory devices, there is also a distribution of cell properties because the circumstances of cells are different from each other. In order to overcome these problems, distribution of cell signal or V_{BL} measurements have to be included [26]. Figure 16. (a) and (b) show the distribution of V_{BL} of FeRAM cells after HTS at 175°C, for 3 hours and 48 hours, respectively. Both distributions of V_{BL} of DATA"0" READ ($V_{BL"0"}$) and of DATA"1" READ ($V_{BL"1"}$) show bimodal distribution. It results from the fact that half of the memory cells were written with DATA"0" and the other half of those were written with DATA"1" before HTS. The memory cells written with DATA"0" show a reduction of DATA"1" signal, while those written with DATA"1" show an increase of DATA"0" signal. Because during the measurements of V_{BL}, the sense amplifier operation is executed, the measured V_{BL} is different from real V_{BL} by the magnitude of sense amplifier sensitivity, about 100mV. Therefore real $V_{BL"1"}$ distribution must be shifted to right-hand side by 100mV, and real $V_{BL"0"}$ distribution left-hand side by 100mV in Figure 16. With this calibration of the effect of sense amplifier sensitivity during the measurements of V_{BL} distribution, we can consider that the minimum sensing signal margin of an FeRAM with 2T/2C configuration is equivalent to the difference between minimum of $V_{BL"1"}$ and maximum of $V_{BL"0"}$.

The variation in the minimum sensing margin as a function of HTS time at 175°C is shown in Figure 17.

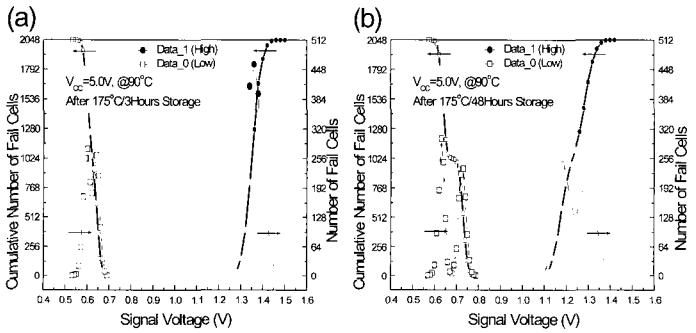

Fig. 16. Distributions of V_{BL} during DATA READ from FeRAM cells after HTS for (a) 3 hours and (b) 48 hours at 175°C.

It also shows a linear relationship with logarithm of HTS time as the variations in P_{S+} and P_{NS-} of ferroelectric capacitor do. We can estimate the lifetime of FeRAM with 2T/2C cell configuration, which is defined by the time when the minimum sensing margin becomes smaller than the sense amplifier sensitivity of 100mV. The lifetime of the FeRAM estimated from Figure 17 is about 800 hours 175°C HTS.

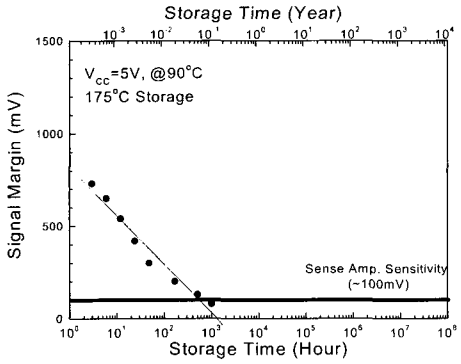

Fig. 17. Variation in minimum sensing margin of 2T/2C FeRAM as a function of time at 175°C HTS.

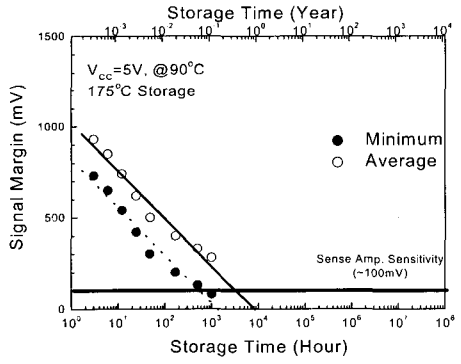

Fig. 18. Variation in average (open) and minimum (solid) sensing margin of a 2T/2C FeRAM as a function of time at 175°C HTS.

There is a significant difference between the lifetimes of a ferroelectric capacitor and of an FeRAM. Because the lifetime of a ferroelectric capacitor is obtained from the average properties of the capacitor array, it is possible to consider that the average sensing margin, which is defined by the difference between average $V_{BL"1"}$ and average $V_{BL"0"}$, would be zero at the lifetime of ferroelectric capacitor. The difference between the average and minimum sensing margin in Figure 16 (a) is about 200mV. Hence, if we add the difference of 200mV to the minimum sensing margin as shown in Figure 18, the average sensing margin becomes zero after ~10^4 hours at 175°C, which is equivalent to the lifetime of ferroelectric capacitor as shown Figure 15.

Now it is possible to calculate the lifetime of an FeRAM at any HTS temperature if we know the lifetime of a ferroelectric capacitor at the HTS temperature. Figure 8 shows the lifetime estimation of the FeRAM at 125°C HTS, where the minimum lifetime of ferroelectric capacitor is about $2x10^7$ hours as shown in Figure 15. The minimum lifetime at 125°C HTS is about $1x10^5$ hours, which is corresponding to more than 10 years.

Table II shows a reliability test result of 64K bit FeRAM with 2T/2C configuration at TSOP-I type package level. It has not reached a commercialization level yet, even though the reliability test results are excellent. The reliability of the FeRAM with a modified ferroelectric capacitor process is under evaluation.

TABLE II. 64K 2T/2C FeRAM Reliability Test Results.

Test Item	Test Condition	Fail/ Sample
EFR	125°C/Dynamic/5.5V : 80Hrs.	1/50
Fatigue-1	0°C/5.5V : $9x10^{11}$ Cycles	0/50
Fatigue-2	75°C/5.5V : $9x10^{11}$ Cycles	0/50
Temp./Humidity	85°C/85%RH/5.5V : 96Hrs.	0/50
Temp. Cycle	-65°C/150°C : 200Cycles	0/50
HAST	130°C/85%RH/5.5V: 96Hrs.	0/50
ESD_HBM	2000V	0/5
EST_MM	250V	0/5
Latch Up	EIA JEDEC JC-40.2	0/5

The lifetime of an FeRAM with 1T/1C cell configuration is defined by the time when the minimum sensing margin becomes less than twice the sense amplifier sensitivity, 200mV. It could be estimated from Figure 19, to be about $3x10^4$ hours, which is less than 10 years yet. However, because FeRAM with 1T/1C cell configuration needs reference voltage, which also has some distribution, the actual lifetime is shorter than the above result.

In case of an FeRAM with 1T/1C configuration, the initial reference level is also very important. As shown in Figure 3, the degradation rates of P_{S+} and P_{NS-} are different. It finally results in different degradations between the minimum of $V_{BL"1"}$ and the maximum of $V_{BL"0"}$ as shown in Figure 20. Degradation of $V_{BL"1"}$ is

much faster than that of $V_{BL"0"}$. Therefore the reference level must be shifted toward $V_{BL"0"}$ to locate it at center between $V_{BL"1"}$ and $V_{BL"0"}$ after HTS. Reliability of FeRAM with 1T/1C configuration is now under evaluation with modified ferroelectric capacitor process.

In summary the fabricated 64K bit FeRAMs with 2T/2C and 1T/1C cell configurations were evaluated for imprint and retention. The lifetime of the 2T/2C FeRAMs are estimated and correlated with the lifetime of ferroelectric capacitors. From the correlation of lifetime of FeRAMs and ferroelectric capacitors, the lifetime of FeRAMs at any HTS temperature can be extracted if the lifetime of ferroelectric capacitor is known. The 2T/2C FeRAM shows excellent reliability results. A 1T/1C FeRAM needs extra signal margin, which is corresponding to the summation of twice the sense amplifier sensitivity and reference level distribution. The set-up of initial reference level is very important for reliability of 1T/1C FeRAM because the degradation rate of ferroelectric capacitor is not symmetric.

VI. SUMMARY

The critical issues, the electrical degradation of the SBT-based ferroelectric memories due to especially the thermal stress and process impurities, regarding the process integration such as reactive ion etching (RIE), interlayer dielectrics, passivation, and packaging are reviewed. The superior performance of the 64kbit ferroelectric memories evaluated with critical reliability issues, imprint and retention degradation at high temperature, is consequent to the complete optimization of thermal stress and process impurities.

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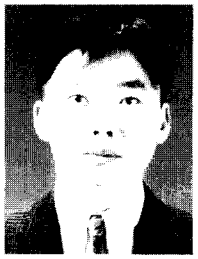

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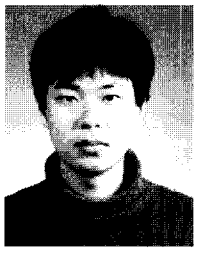

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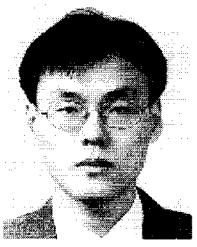

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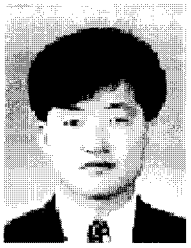

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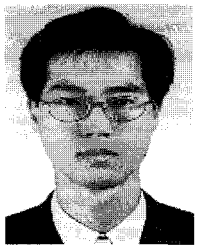

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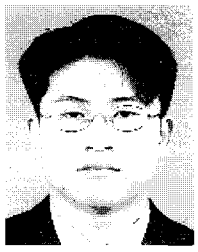

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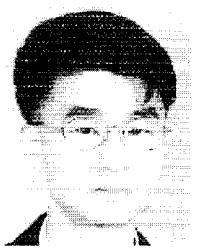

Chang-Goo Lee was born in Seoul, Korea, on April 12, 1969. He received the M.E. degrees in electronics engineering from Soongsil University, Korea, in 1995. He joined Hynix Semiconductor Inc., Ichon, Korea, in 1995, where he has been working on the CVD process development of DRAM's, and the process integration of FeRAM's.

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Young-Jin Park was born in Seoul, Korea, on Jan. 28, 1962. He received M.E. and Ph.D. degrees in materials engineering from Korea Advanced Institute of Science and Technology (KAIST), Korea, in 1987, and 1990, respectively. He had worked on DRAM development during 1990 ~ June, 1996 at Hyundai Electronics and July, 1996 ~ March, 2000 at Infineon Technologies. He is currently working on logic device development for 0.13 um and beyond, and FeRAM/MRAM development as an executive manager, and technical advisor for Hynix Semiconductor Incorporated.