A Word Line Ramping Technique to Suppress the Program Disturbance of NAND Flash Memory

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Abstract— **When the program voltage is applied to a word line, a part of the boosted channel charge in inhibited bit lines is lost due to the coupling between the string select line (SSL) and the adjacent word line. This phenomenon causes the program disturbance in the cells connected to the inhibited bit lines. This program disturbance becomes more serious, as the word line pitch is decreased. To reduce the word line coupling, the rising edge of the word-line voltage waveform was changed from a pulse step into a ramp waveform with a controlled slope. The word-line ramping circuit was composed of a timer, a decoder, a 8 b D/A converter, a comparator, and a high voltage switch pump (HVSP). The ramping voltage was generated by using a stepping waveform. The rising time and the stepping number of the word-line voltage for programming were set to 5μs- and 8, respectively,. The ramping circuit was used in a 512Mb NAND flash memory fabricated with a 0.15-µm CMOS technology, reducing the SSL coupling voltage from 1.4V into a value below 0.4V.**

Index Terms – **NAND Flash memory, Word Line Ramping Circuit, Program Disturbance, SSL Coupling, Word Line Slope**

I. INTRODUCTION

In the NAND flash memory [1-3], cells are connected in series between a bit line and a source line. A simplified structure of a NAND flash memory with two bit lines is shown in Fig. 1. The cells are connected in series with two select transistors, that is, the string select line (SSL) transistor and the ground select line (GSL) transistor. Data are stored in the form of charge within floating gates. The control gate of the cell to be programmed is driven into a high voltage in the range of 15~20V, while the corresponding bit line is biased at 0V, as shown in the inset of Fig.1. The control gates of all other cells which act as pass gates are driven into a medium voltage (V_{pass}) of around 10V. The bit-line voltage is transferred to the channel through the cells in series, so that the induced high voltage drop between floating gate and channel allows for the Fowler-Nordheim (FN) electron tunneling only at the cell to be programmed. The voltage of the unselected word lines (V_{pass} ~ 10V) was determined from the trade off between two needs. One is the need for these unselected cells to act as good pass gates independently of their threshold voltages. The other is the need for preventing the program disturbance in these unselected cells. This program disturbance can be avoided by limiting the electric field across the tunnel oxide of the unselected cells. The tunnel oxide field is limited also in the program inhibited cells which shares the same word line with the selected cells. This is accomplished by raising the voltage of bit lines to V_{cc}[1]. Thus, the channels of the program inhibited cells are precharged to V_{cc}-V_{th}. The corresponding SSL transistors are shut off after the precharge. When the program voltage (V_{pgm}) is applied to the selected word line after precharge, the channels of the inhibited cells are boosted[4] and the program inhibited cells are not programmed. To prevent the program disturbance at the inhibit cells, the boosted channel potential should be maintained while a high

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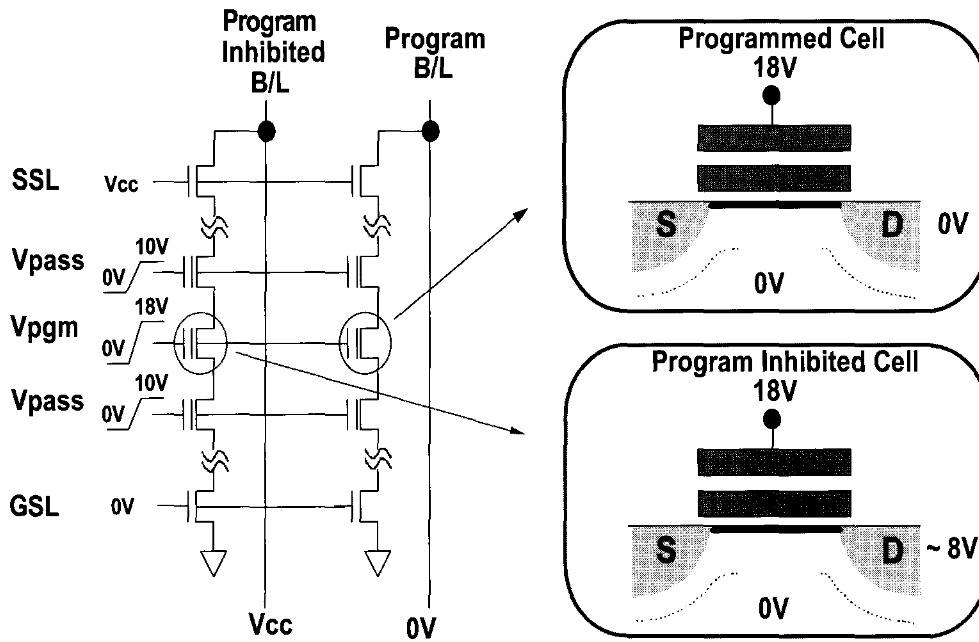

Fig. 1. Self boosted program inhibit scheme.

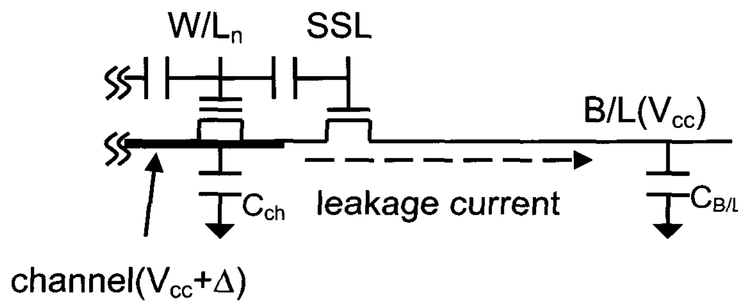

Fig. 2. Schematic of W/L_n to SSL coupling.

program voltage V_{pgm} is applied to the selected word line. A small leakage current in the inhibited channel causes a gradual decrease of the channel potential, which causes a severe program disturbance problem. The leakage current in the channel of the string consists of the junction leakage current and the off-state (subthreshold) leakage current. Although the junction leakage can be suppressed by a well cared process, the off-state leakage current through SSL or GSL is still a problem. The worst case occurs when the word line adjacent to the SSL is selected. Fig. 2 shows a schematic diagram showing the word line to SSL coupling problem in the program inhibited cells. The SSL transistor is turned off after precharge in this case. When the program voltage V_{pgm} is applied to the word line adjacent to the SSL, the SSL voltage level is boosted by a capacitive coupling from the adjacent word line where the program voltage is applied. This boost up of the SSL voltage level induces a off-state (subthreshold) leakage current through the SSL transistor. This reduces the charges in the channel regions underneath the program inhibited bit lines, which decreases the voltage level of the channel region of inhibited bit lines. This in turn increases the voltage drop across the tunnel oxide, which causes the program disturbance problem in the program inhibited cells. This problem is more serious with low V_{cc} because the precharge level is relatively lower than with high V_{cc} , which decreases the body effect of the SSL transistor hence the effective threshold voltage.

In this paper, a ramping circuit is proposed to control

the slope of the program voltage V_{pgm} to reduce the program disturbance in the program inhibited cells. The reduction of the V_{pgm} slope reduces the capacitive coupling. Section II shows how to decide the rising time and the stepping number of V_{pgm}. Section III shows how to implement the ramping circuit. Section IV concludes this work.

II. Rising Time And Number Of Stepping Of Program Voltage

Fig. 3 shows the peak coupling level between the SSL and the adjacent word line. The horizontal axis represents the rising time of the program voltage V_{pgm}, where the shape of V_{pgm} was assumed to be an ideal linear ramp. The peak level is 1.4V where the V_{pgm} rising time is 1μs and V_{cc} is 2V.

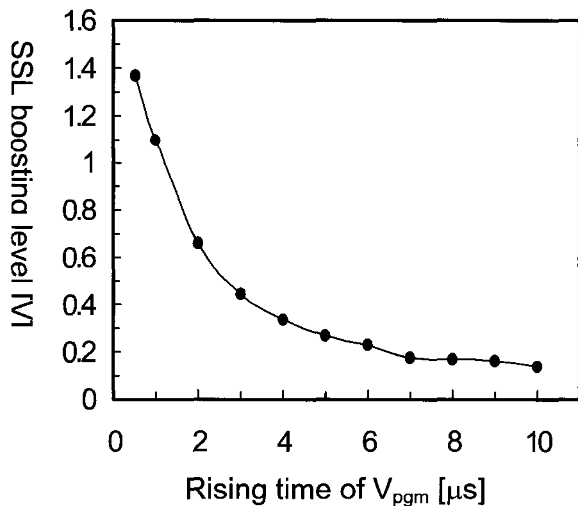

Fig. 3. The peak coupling between the word line and SSL versus the rising time of V_{pgm}

Fig. 4 shows the I_d-V_g characteristics of the SSL transistor for different values of V_{BS}(effective body bias). According to Fig. 4, the leakage current is about 200nA where the peak coupling level is about 1.4V(V_g=1.4V, V_{bs}=-2V). With the leakage current of 200nA, the precharged channel charge of the inhibited lines is swept away and that lowers the channel potential by 5V in 30 ns. In this case, it is impossible to inhibit the program disturbance in the program inhibited cells because the channel of the inhibited bit lines is not boosted. When the rising time of the program voltage is increased, the peak level is drastically decreased due to the reduction of the capacitive coupling. However, there is a trade off between the program performance and the suppression of a word line coupling into SSL. That is, the small rising slope suppresses the SSL coupling noise, but it takes a long time to reach the target program voltage. Therefore, it is necessary to adjust the program rising slope to satisfy both the program performance and the inhibit efficiency. According to Fig.3, the coupling from word line to SSL suppressing is rapidly decreasing with the increase of the V_{pgm} rising time until the V_{pgm} rising time is increased up to 5 μs. When the word line to SSL coupling is 0.4 V, the subthreshold current of the SSL transistor is lower than a few pA. Therefore the word line rising slope was set to 5 μs.

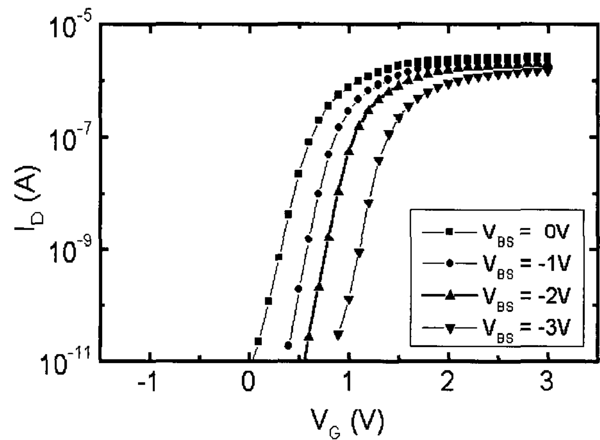

Fig. 4. I_d-V_g characteristic of SSL transistor for different values of body bias.

Several methods can be used to adjust the V_{pgm} slope. Since the program voltage V_{pgm} is generated from the charge pump, the slope of V_{pgm} can be adjusted by controlling the charge pump capacity. However, it is impossible to make the charge pump capacity be constant because the charge pump currents are varied with supply voltage. If we set the charge pump capacity in the low V_{cc} condition, the V_{pgm} slope is relatively steep in high V_{cc} and hence the coupling suppression efficiency is low. If we set the charge pump capacity in high V_{cc}, it will take long time to reach the target program voltage in low V_{cc}. Thus, the constant V_{pgm} slope method by adjusting the charge pump capacity is impractical. Therefore it is necessary to adjust the output voltage of the charge pump instead of the charge pump

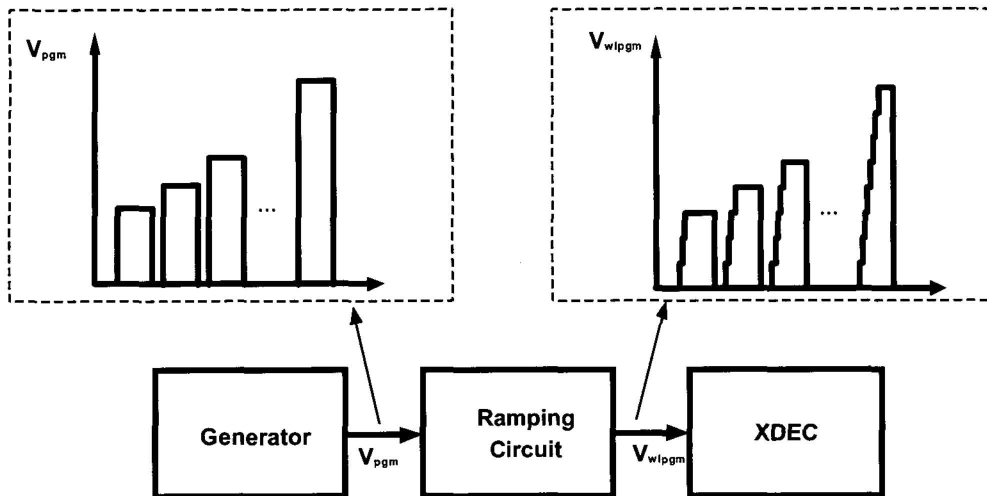

Fig. 5. Bloack diagram of a word line generator with ramping circuit.

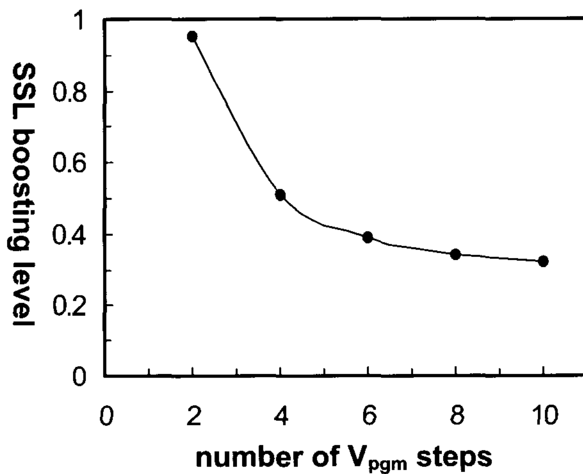

Fig. 6. Number of V_{pgm} steps within 5 μs at a ISPP step.

capacity. In order to adjust the output voltage of the charge pump, we adopt the ramping circuit generating V_{pgm} like the staircase form as shown in Fig.5. In implementing the ramping circuit, one of key issues is how many steps are required for a given 5 μs. If there are too many steps, the resultant circuit will be too complicated and the layout overhead will be excessive. If the number of steps is too small, the inhibit efficeincy will be decreased. Fig. 6 shows the word line to SSL coupling level with the number of V_{pgm} steps for the V_{pgm} rising time of 5 μs. The ramping efficiency is saturated after eight steps as shown in Fig. 6. Following these simulation results, we designed the word line ramping circuit to have eight V_{pgm} steps in 5 μs.

III. Configuration Of Ramping Circuit

Programming is performed using the incremental step pulse programming (ISPP) scheme [1], in which the selected word line voltage increases at every program cycle in order to minimize the number of the program cycle and programming time. Fig. 5 shows the block diagram of the V_{pgm} generator with the ramping circuit. The ramping circuit is placed between the charge pump generator and the X-Address decoder.

The ramping circuit is composed of a timer, a decoder, a 8-b D/A converter, a comparator, and a high voltage switch pump (HVSP) as shown in Fig. 7. The D/A converter divides the V_{wlpgm} at a given step. The HVSP raises V_{wlpgm} until the output of the D/A converter reaches the reference voltage (V_{ref}). At the next step, the change of input digital coding lowers the output level of the D/A converter below V_{ref} and the HVSP raises V_{wlpgm} until the V_{wlpgm} reaches the target value (V_{pgm}).

Fig.8 shows the simulated waveforms of the word line voltage and the SSL peak level for different values of supply voltage(V_{cc}).

As a result, we designed the word line ramping circuit to have eight ΔV_{pgm} steps in 5 μs so that the word line to SSL coupling is reduced to 0.4 V. Thus the resultant subthreshold leakage current of the SSL transistor is only a few pA and the channel voltage drop at the program inhibited cells is below 0.005V, which practically

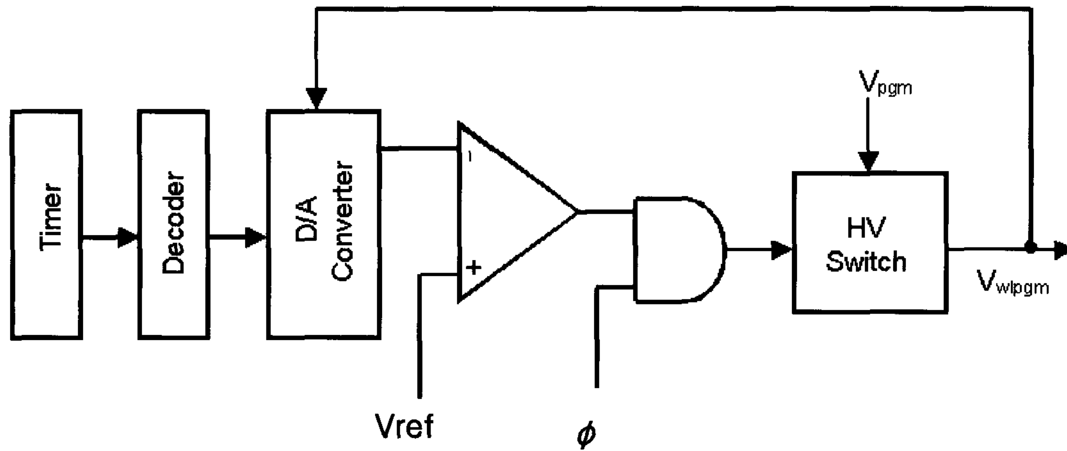

Fig. 7. Schematic diagram of ramping circuit.

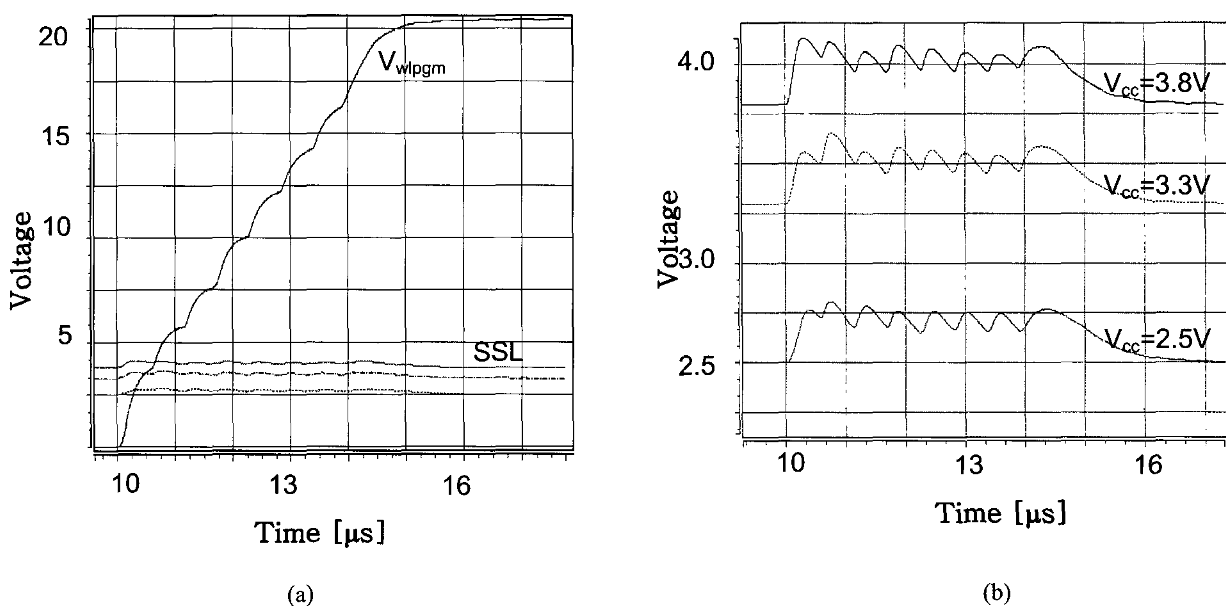

Fig. 8. Simulated waveform of (a) 5 μs-8steps word line with ramping circuit (b) SSL peak voltage according to various V_{cc}.

eliminates the program disturbance problem caused by the word line coupling

IV. Conclusion

A word line ramping circuit was proposed to reduce the program disturbance problem at the program inhibited cells. This was done by reducing the capacitive coupling from the word line to SSL. The word line voltage V_{pgm} was increased in a ramp waveform by using eight ΔV_{pgm} steps in 5 μs (rising time). The number of steps and the rising time was decided by taking into account of the program time and the process margin. In this way, the word line to SSL coupling is reduced to 0.4 V and the subthreshold leakage current of the SSL transistor is lower than a few pA. This ramping circuit was used in the 512Mb flash memory fabricated with a 0.15-μm CMOS technology

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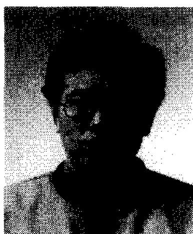

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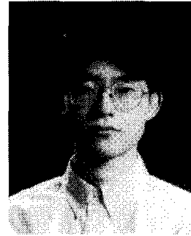

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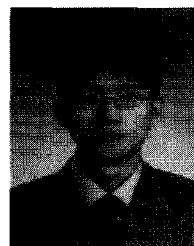

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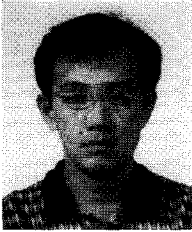

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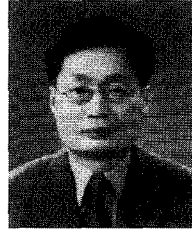

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