High-Speed Signaling in SDARM Bus Interface Channels : Review

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Abstract—**Three kinds of high-speed signaling methods for synchronous DRAM (SDRAM) bus interface channels (PC-133, Direct-Rambus, and SSTL-2) were analyzed in terms of the timing budget and the physical transmission characteristics. To analyze the SDRAM bus interface channels, loss mechanisms and the effective characteristic impedance method were reviewed and the ABCD matrix method was proposed as an analytic and yet accurate method. SPICE simulations were done to get the AC responses and the eye patterns of the three SDRAM bus interface channels for performance comparisons. Recent progress and future trend for SDRAM bus interface standards were reviewed.**

Index Terms—**SDRAM bus interface channel, high-speed signaling, PC-133, Direct-Rambus, SSTL-2**

I. Introduction

The clock frequency of CMOS chips crossed the 1GHz barrier [1-3]. However the chip-to-chip communication speed on the printed circuit board (PCB) is usually much lower than this. Thus the chip-to-chip communication speed usually limits the entire system performance. Especially the DRAM bus interface of a computer system forms the bottleneck in enhancing the performance of the entire computer system.

There are two approaches to improve the DRAM interface speed. One is to increase the chip-to-chip signal transmission speed on PCB, the other is the embedded-memory-logic approach where both DRAMs and CPU are placed on a single chip to achieve the high-speed interface due to the low on-chip capacitance loading. Although the embedded-memory-logic approach was expected to be very promising, it is not widely used yet due to the yield problem. Therefore, the first approach of increasing the chip-to-chip signal transmission speed on PCB is expected to be the main stream approach at least in the near future[4].

In conventional normal mode asynchronous DRAMs, the maximum data throughput usually cannot exceed 10MHz. To increase the data throughput using the conventional asynchronous DRAMs, the fast page mode and the EDO (Extended Data Out) mode were adopted by changing only the $\overline{CAS}$ signal and the column address signals. The data throughputs of 25MHz and 50MHz were obtained with the fast page mode and the EDO mode, respectively. To further improve the data throughput, synchronous DRAMs (SDRAMs) were invented. SDRAMs use an external system bus clock to synchronize the operations of the entire DRAM chip. The data throughputs of SDRAMs started from 66MHz and they were improved to 100MHz and 133MHz[5].

Section II shows the overview and the timing budgets of the SDRAM bus interface standards that are widely used nowadays in personal computer (PC) systems. Section III explains the loss mechanisms of transmission lines such as skin effect and dielectric loss, and the conventional effective characteristic impedance method and the ABCD matrix method for analyzing the SDRAM bus interface channels, which was newly proposed in this work. Section IV shows the SPICE simulation results and the performance comparisons of the currently used SDRAM bus interface channels. Section V shows the recent progress and future trend of the SDRAM bus interface standards. Section VI concludes this work.

II. Overview of SDRAM Bus Interface Standards

Currently, three kinds of standards for SDRAM bus

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Tabel 1. Comparison of SDRAM bus interface standard.

Standard		PC-133	Direct-Rambus	SSTL-2
Data rate (Mbps)		133	800	266
Parallel high-speed channel		64 DQ	30	64 DQ, 8 DQS
Data bandwidth (GB/s)		1.1	1.6	2.1
Input voltage levels		0.4, 2.4V (output)	1, 1.8V (output)	VTT±0.35V (AC input)
Supply voltage	VDDQ	3.3V	-	2.5V
	VTT	-	1.8V	1.25V
	VREF	1.4V(internal)	1.4V	1.25V

interface channels are widely used in the memory bus of computer systems. They are PC-133, D-Rambus (Direct-Rambus) and SSTL-2 (Series Stub Terminated Logic-2). The performance comparisons among these three standards are shown in Table 1.

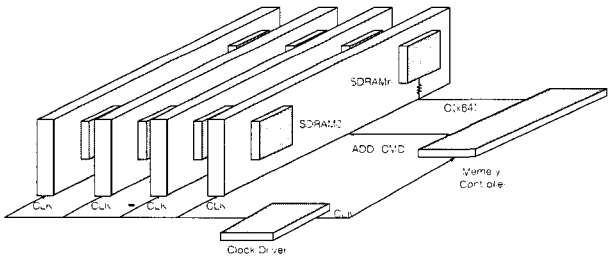


Fig. 1. PC-133 SDRAM bus interface system.

A. *PC-133*

The PC-133 standard uses the LVTTL (Low Voltage Transistor Transistor Logic) scheme for chip-to-chip interface[5]. Fig.1 shows the schematic of a PC-133 system. Up to four DIMM PCB cards can be installed on a main board and several SDRAM chips are installed in a DIMM card so that 64 bi-directional data lines are connected between the memory controller and the SDRAM chips located on a DIMM PCB. DIMM represents Dual In-line Memory Module, which is a PCB card where DRAM chips are attached on both sides. Clock signals are distributed to the memory controller and all the SDRAM chips on DIMM cards from a clock driver. 12-bit addresses and some command signals are sent to the SDRAM chips on DIMM PCBs from the memory controller. [6]

For the proper operation, the clock cycle time T_{cycle} must meet the following constraint.

$$2 \cdot T_{cycle} > t_{AC} + t_f + t_{setup} + t_{hold} + t_{skew} \quad (1)$$

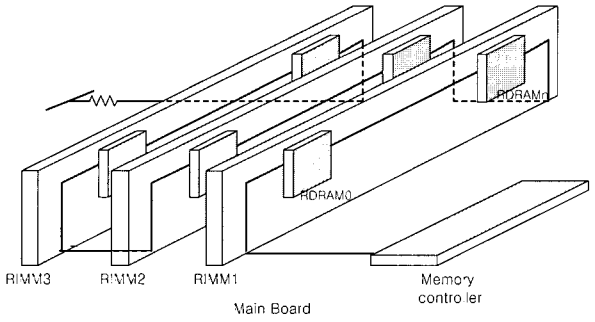
where t_{AC} is the clock-to-output delay of SDRAM, t_f is the time of flight from the SDRAM chip to the memory controller through the PCB transmission lines, t_{setup} is the set-up time of input latch and t_{skew} is the clock skew between the SDRAM clock and the memory controller clock. $2 \cdot T_{cycle}$ was used in Eq. (1) instead of T_{cycle}, since the CAS latency of 3 is used in the PC-133 interface standard. The typical values of t_{AC}, t_f, t_{setup}, t_{hold}, t_{skew} are 6ns, 1.5ns, 1.5ns, 0.8ns, 0.5ns, respectively. These parameter values satisfy the requirement shown in Eq. (1)[6].

B. *Direct-Rambus*

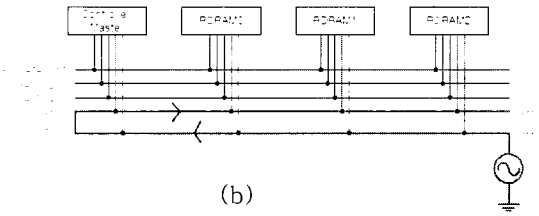
As shown in Fig. 1, there are 64 parallel data lines, 12 address lines, and command lines running on the printed circuit board of a PC-133 SDRAM bus interface system. The Rambus interface system was designed to have a small number of parallel lines running on PCB to enable a high-speed operation[7-9]. For this purpose, only 30 high-speed lines are running in parallel on the PCB of a Rambus interface system. These 30 high-speed lines include 18 bi-directional data (DQ) lines, 8 address lines, and two differential clock lines. Since there are only a few address lines and no command lines, in the Rambus interface, the addresses and commands are sent in a

packet form through the Rambus interface channel.

Fig. 2. (a) shows a simplified schematic of the Rambus interface system. Clock lines are not shown in Fig. 2. (a) for simplicity. A high-speed line starts at the memory controller on the main board PCB, enters a Rambus memory module, visits every Rambus DRAM chip on the module, returns to the main board, repeats the connections at the second module and the third module, and finally is terminated by a termination resistor on the main board. Up to 16 Rambus DRAM chips are located in a Rambus memory module. Three Rambus memory modules are used in a Rambus interface system. Fig. 2. (b) shows the electrical connections of the high-speed lines of the Rambus interface[10-11].



(a)



(b)

Fig. 2. Rambus interface system.

In the Rambus interface system, DLLs (delay locked loops) are used to reduce the clock-to-output delay (t_{AC} of Eq. (1)) by matching the transition time of data output to that of clock[8]. Also, one end of each high-speed line is terminated to improve the signal integrity. Each high-speed line is implemented as a strip line surrounded by two metal planes at the ground or VDD potential[9]. A ground line is inserted between two parallel high-speed lines to reduce crosstalk. As shown in Fig.2, the clock line follows the data or address line in both directions to reduce the clock skew and the delay due to the time of flight (t_f of Eq. (1)). Also open-drain output drivers are used to reduce reflections at the output driver. This was done by operating an NMOS open-drain output driver in saturation region so that it does not reflect signals due to its high small-signal output resistance[8].

For the proper operation of the Rambus interface system at the data rate of 800 Mbps, the half cycle time ($T_{cycle}/2$) must meet the following constraint.

$$\frac{T_{cycle}}{2} \geq \Delta t_{AC} + t_{setup} + t_{hold} + t_{skew} + \Delta t_f \qquad (2)$$

where T_{cycle} is 2.5ns. A half cycle ($T_{cycle}/2$) was used in Eq. (2) since data change at both rising and falling edges of clock. Δt_{AC} , t_{setup} , t_{hold} , t_{skew} , Δt_f are given to be 0.55ns, 0.2ns, 0.2ns, 0.1ns, 0.2ns, respectively. Δt_{AC} is the mismatch in the clock-to-output delay. Δt_{AC} is reduced drastically from $t_{AC} = 6.0ns$ of PC-133 due to the DLL circuit. t_{skew} is the clock skew. t_{skew} is reduced due to the use of the differential signaling for clock signals. Δt_f is the mismatch in delay due to the transmission channel. It includes the effects of crosstalk, inter-symbol interference, mismatches in the capacitance, inductance and resistance values of DRAM input pins[10][12].

C. *SSTL-2*

Fig. 3 shows the SSTL-2 (Series Stub Terminated Logic-2) SDRAM bus interface system. 2 in SSTL-2 represents that it uses the supply voltage of 2.5V. It is similar to the PC-133 standard except three differences. The first difference is that SSTL-2 uses 8 bidirectional data strobe (DQS) lines in addition to the 64 bidirectional data (DQ) lines. Each DRAM chip on a DIMM card is connected to one of eight data strobe lines[5,13]. These DQS signals sent from a transmitter are used for synchronization in the receiver side when reading the DQ signal sent from the same transmitter. Since the line length, the driver strength and the loading are matched for the DQS and DQ signals, this synchronization scheme reduces the clock skew (t_{skew}) and the mismatch in the time of flight (Δt_f). Since this synchronization scheme of SSTL-2 is based on sending the DQS and DQ signals simultaneously at the transmitter side, it is called the source synchronization

Table 2. Comparison of timing constraints between PC-133, Direct-Rambus, and SSTL-2.

Standard	PC-133	D-Rambus	SSTL-2
Clock-to-output delay	t_{AC} = 6ns	Δt_{AC} = 0.55ns	Δt_{AC} = 1.5ns
t_{setup}	1.5ns	0.2ns	0.75ns
t_{hold}	0.8ns	0.2ns	0.75ns
t_{skew}	0.5ns	0.1ns	0.5ns
Time of flight	t_f =1.5ns	Δt_f =0.2ns	Δt_f =0.25ns
Sum	10.3ns	1.25ns	3.75ns
Cycle time	T_{cycle} =7.5ns	$T_{cycle}/2$ =1.25ns	$T_{cycle}/2$ =3.75ns

scheme. The second difference is that the SSTL-2 interface uses a DLL circuit to reduce the clock-to-output delay (Δt_{AC})[14-16]. The third difference is that the SSTL-2 interface uses both series and parallel terminations to improve the signal integrity. Parallel terminations were done on the main board, and series terminations were done on DIMM cards.

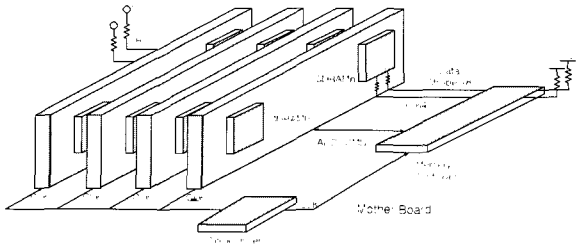


Fig. 3. SSTL-2 SDRAM bus interface system (DDR)

SSTL-2 uses a 133MHz clock with the cycle time T_{cycle} of 7.5ns and the data rate is 266Mbps due to the DDR (double data rate) operation, that is, data change at both rising and falling edges of clock. For the proper operation at the data rate of 266 Mbps, the following constraint must be satisfied.

$$\frac{T_{cycle}}{2} > \Delta t_{AC} + t_{setup} + t_{hold} + t_{skew} + \Delta t_f \qquad (3)$$

where Δt_{AC} , t_{setup} , t_{hold} , t_{skew} , and Δt_f are 1.5ns, 0.75ns, 0.75ns, 0.5ns, 0.25ns. t_{skew} represents the skew between DQ (data signal) and DQS (data strobe signal)[5].

D. *Comparison of timing constraints*

Table 2 summarizes the comparison of timing constraints between the three SDRAM bus interface standards.

III. Methodology For Channel Analysis

For the analysis of high-speed SDRAM bus interface channels, the transmission line analysis is usually required. The loss mechanisms of transmission lines such as the dielectric loss and the skin effect need to be considered for high-speed data transmissions. Usually SDRAM chips are connected between a transmission line (a bus interface channel) and ground in parallel and also in uniform spacing to increase the memory capacity of a system. This connection of SDRAM chips to a transmission line lowers the characteristic impedance of transmission line, slows down the signal propagation speed along the transmission line, and increases the propagation loss.

This chapter presents the conditions which require the transmission line analysis, two analysis methods for transmission lines, and the comparison between loss mechanisms of transmission line. The above-mentioned two analysis methods include the conventional effective characteristic impedance method and the ABCD matrix

method proposed in this work.

A. *Conditions which require Transmission Line Analysis*

When the data rates of SDRAM bus interface channels exceed several hundred MHz, the transmission line analysis must be used for the SDRAM bus interface channels. Whether a signal line in a SDRAM bus interface channel needs a transmission line analysis or not depends on the frequency components of a signal. If the length of a signal line is larger than one-eighth the wave length(λ_{knee}) of the highest frequency(f_{knee}) component of a signal, the transmission line analysis is required. That is, the condition for transmission line analysis to be required can be stated as

$$l_{TL} > \frac{1}{8} \cdot \lambda_{knee} \tag{4}$$

where l_{TL} is the length of a transmission line. This (1/8)·λ_{knee} criterion was rather arbitrary[19]. If the length of a signal line is equal to λ_{knee} /8, the amplitude of the highest frequency(f_{knee}) sinusoidal signal reaches $1/\sqrt{2}$ times the peak amplitude at one end of the signal line when the amplitude of the signal is 0 at the other end.

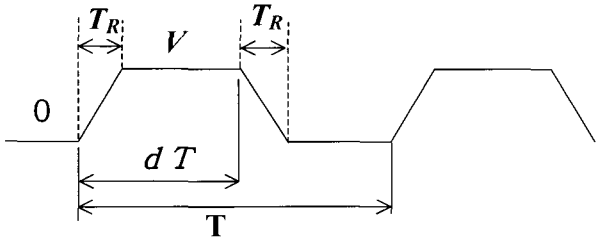


Fig. 4. A voltage signal waveform $v_s(t)$.

A digital signal waveform $v_s(t)$ is shown in Fig. 4, where d is the duty and T_R is the rise time. Since $v_s(t)$ is a periodic signal with a period of T, it can be represented by a Fourier series, as shown in Eq. (5.a).

$$v_s(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos\left(2\pi \cdot \frac{n}{T} t\right) \tag{5.a}$$

$$a_0 = V \cdot d \tag{5.b}$$

$$a_n = 2Vd \cdot \frac{\sin(n\pi \cdot d)}{n\pi \cdot d} \cdot \frac{\sin\left(n\pi \cdot \frac{T_R}{T}\right)}{n\pi \cdot \frac{T_R}{T}} = 2Vd \cdot \sin c(n\pi d) \cdot \sin c\left(n\pi \cdot \frac{T_R}{T}\right) \tag{5.c}$$

where n/T corresponds to the frequency of harmonic components. The envelope of a_n in Eq.(5.c) reveals that there is a significant amount of energy distributed up to the frequency f_{knee} [19,20], where

$$f_{knee} = \frac{0.5}{T_R} \tag{6}$$

Substitution of Eq.(6) into Eq.(4) gives the condition which requires the transmission line analysis, as follows.

$$l_{TL} > \frac{1}{4}(v \cdot T_R) \tag{7}$$

where v is the signal propagation velocity along the transmission line and the relation of $v = f_{knee} \cdot \lambda_{knee}$ was used in the derivation of Eq.(7). $v \cdot T_R$ in Eq.(7) represents the rise time length which corresponds to the length of signal propagation during the rise time T_R.

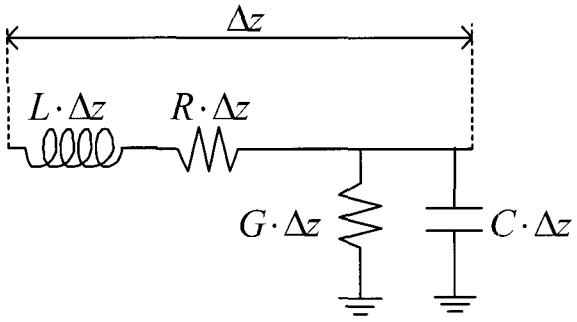


Fig. 5. Equivalent circuit of a section of transmission line.

B. *Lossy Transmission Line*

Base transmission lines without DRAM chips connected experience losses at high signal frequencies. This high frequency loss of transmission line is mainly caused by the skin effect and the dielectric loss. Fig.5 shows the equivalent circuit of an infinitesimally small section Δz of a transmission line. L and C represent the inductance and the capacitance per unit length. R is the resistance per unit length mainly due to the skin effect. G is the conductance per unit length due to the dielectric loss.

A single-trip transfer function $H(j\omega)$ through a

transmission line of length l without reflections can be written as

$$H(j\omega) = e^{-\sqrt{(R+j\omega L)(G+j\omega C)}\cdot l} = e^{-\alpha\cdot l}\cdot e^{-j\omega\sqrt{LC}\cdot l} \quad (8.a)$$

$$\alpha = \frac{1}{2}\cdot\left(\frac{R}{\sqrt{L/C}} + G\cdot\sqrt{\frac{L}{C}}\right) \quad (8.b)$$

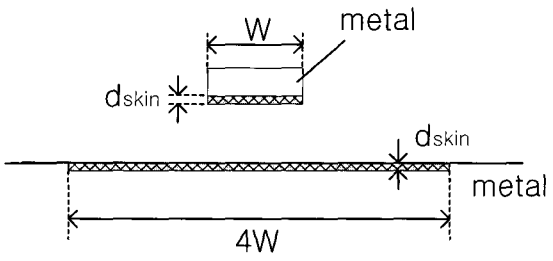


Fig. 6. Cross section of a transmission line to show skin effect.

The origins of R and G are explained in the following paragraphs. The skin effect refers to the phenomenon that the resistance increases as the signal frequency increases because the current flows only through the narrow cross section of metal electrode near the surface at high frequencies. Fig.6 shows the cross section of a transmission line, where the gray area represents the cross section of metal in which the current flows. The thickness of this cross section is called the skin depth d_{skin}, which can be represented as

$$d_{skin} = \frac{1}{\sqrt{\pi f \mu \sigma_{metal}}} \quad (9)$$

where f is the signal frequency, μ is the magnetic permeability of metal, σ_{metal} is the conductivity of metal. The resistance of the return path on the ground plane must be included in the calculation of the series resistance R. The current is assumed to be distributed along $4W$ on the ground plane, where W is the width of the upper metal section[18].

Since the DC resistance is negligible compared to the resistance due to the skin effect, the series resistance R per unit length can be calculated as the sum of the resistance due to the skin effects on the upper metal section and the ground plane.

$$R = \frac{1}{W\sigma_{metal}d_{skin}} + \frac{1}{4W\sigma_{metal}d_{skin}} = R_s\sqrt{f} \quad (10.a)$$

$$R_s = \frac{1.25}{W}\sqrt{\frac{\pi\mu}{\sigma_{metal}}} \quad (10.b)$$

When the thickness of the upper metal section is significant compared to W, W in the first term of Eq. (10.a) is replaced by W+2*(*metal thickness*).

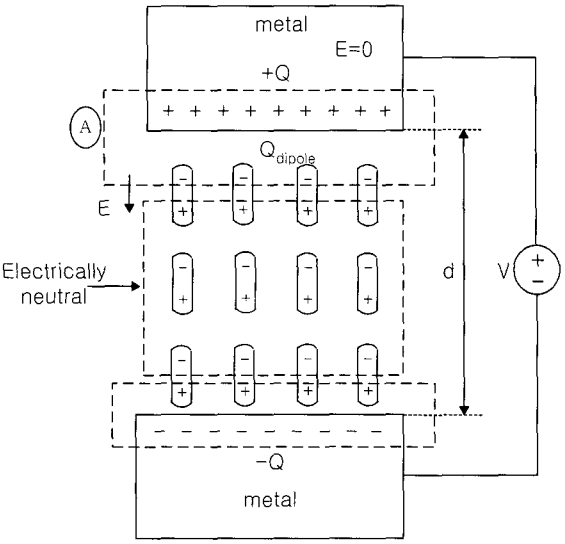


Fig. 7. Origins of dielectric constant $\varepsilon_0\cdot\varepsilon_R$ and loss tangent tan δ.

When an electric field is applied to a dielectric material(insulator), electric dipoles are formed in the molecules of dielectric material as shown in Fig.7. The electric field E inside the dielectric material is determined by the applied voltage V and the separation d between the two metal electrodes, such that, $E = V/d$. Due to the dipoles of dielectric material the charge Q on the metal electrode becomes larger than $\varepsilon_0 E$, where ε_0 is the dielectric constant of free space or air. This can be verified by applying the Gauss law on the closed loop A shown in Fig.7. The dipole charge Q_{dipole} is also proportional to the electric field E.

$$\varepsilon_0 E - 0 = Q - Q_{dipole} \quad (11.a)$$

$$Q = \varepsilon_0 E + Q_{dipole} = \varepsilon_0\cdot\varepsilon_R\cdot E \quad (11.b)$$

Thus the dipoles of dielectric material increase the dielectric constant. Capacitance C is defined to be

$$C = \frac{Q}{V} = \frac{\varepsilon_0\varepsilon_R}{d} = \frac{\varepsilon}{d} \quad (12)$$

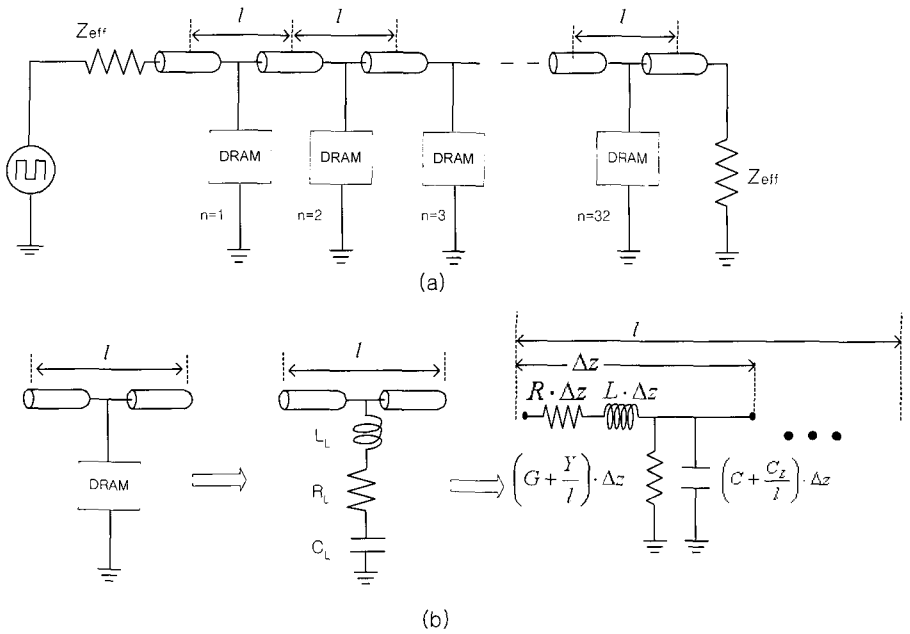


Fig. 8. Analysis of a transmission line with DRAM chips connected in uniform spacing.

When a sinusoidal voltage with an angular frequency ω is applied to the capacitor, the current through the capacitor is $j\omega Q = j\omega C \cdot V$. When the polarity of the capacitor voltage is reversed, the charge distribution of electric dipole is also reversed. When the frequency of the capacitor voltage is very high, the dipole cannot follow the voltage change instantaneously and there is a time delay between the movement of dipole and the voltage change. This delay components of dipole movement cause losses. This loss component is represented by an imaginary part in the complex representation, such that $\varepsilon = \varepsilon_0 \varepsilon_R$ is changed to $\varepsilon \cdot (1 - j \cdot \tan\delta)$. $\tan\delta$ is called the loss tangent. The capacitance C is replaced by $\varepsilon = \varepsilon_0 \varepsilon_R$. Therefore the current through the capacitor I_{cap} can be written as

$$I_{cap} = j\omega C \cdot (1 - j \cdot \tan\delta) \cdot V = j\omega C \cdot V + \omega C \cdot \tan\delta \cdot V \quad (13)$$

$\omega C \cdot \tan\delta$ is equal to G, the conductance per unit length of transmission line, such that

$$G = \omega \cdot C \cdot \tan\delta = G_d \cdot f \quad (14.a)$$

$$G_d = 2\pi \cdot C \cdot \tan\delta \quad (14.b)$$

The loss tangent $\tan\delta$ is about 0.035 in the FR4 material.

C. *Effective Characteristic Impedance Method*

When DRAM chips are connected to a transmission line in uniform spacing as shown in Fig.8.(a), the propagation velocity along this loaded transmission line is decreased and the loss is increased compared to the case without DRAMs. The pin impedance of a DRAM chip is modeled by a series connection of L_L, R_L, C_L as shown in the middle section of Fig.8.(b). When the DRAM spacing l is less than $T_R \cdot v$, the loaded transmission shown in Fig.8.(a) can be treated as a uniform transmission line with the effects of DRAM pin loadings distributed uniformly along the transmission line. T_R and v are the rise time of the incident signal and the propagation velocity, respectively. The condition $l < (T_R \cdot v)$ is a loosened condition compared to that shown in Eq.(7). The steps of distributing the effect of DRAM pin loading uniformly along the transmission line are shown in Fig.8.(b). It is difficult to decrease the DRAM spacing l below $1cm$ due to the limitation of DRAM chip size. The additional loss term Y due to the loading of DRAM chips can be represented as[21],

$$Y = \frac{4\pi^2 R_L C_L^2 f^2}{(1 - 4\pi^2 f^2 \cdot L_L C_L)^2} \quad (15)$$

The effective characteristic impedance Z_{eff} and the propagation velocity v_{eff} of the loaded transmission line are represented by

$$Z_{eff} = \sqrt{\frac{L}{C+\frac{C_L}{l}}} = \frac{Z_o}{\sqrt{1+\frac{C_L}{C \cdot l}}} \quad (16)$$

$$v_{eff} = \frac{1}{\sqrt{L\left(C+\frac{C_L}{l}\right)}} = \frac{v}{\sqrt{1+\frac{C_L}{C \cdot l}}} \quad (17)$$

where Z_o and v are the characteristic impedance and the propagation velocity of the unloaded transmission line respectively. The low loss approximation ($R<<\omega L$, $(G+Y/l)<<\omega(C+C_L/l)$) was used in the derivation steps.

D. *ABCD Matrix Method*

Although the effective characteristic impedance method gives simple analytic equations, it cannot explain the micro reflections which occur when the length of transmission line is not long enough to attenuate reflections. Usually SPICE simulations using the lossless(T model) or lossy(W model) transmission line models are widely used for the analysis of DRAM bus interface channels. Although SPICE simulation gives accurate results, it dose not give analytic equations which can be used as design guides. The ABCD matrix method gives both accurate and analytic equations.

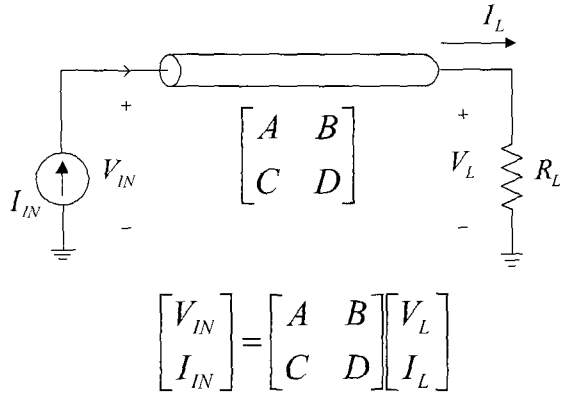


Fig. 9. ABCD matrix.

Fig.9 shows the usage of ABCD matrix for circuit analysis. An input current source I_{IN} is applied to a transmission line. We want to get V_{IN}, V_L and I_L in terms of I_{IN}. Using the load relation $V_L = I_L \cdot Z_L$ and the matrix equation shown in Fig.9, we can get the following analytic equations, as desired.

$$V_{IN} = \frac{Z_0}{\sqrt{1+\frac{C}{C_0 l}}} \quad (18.a)$$

$$V_L = \frac{1}{C+\frac{D}{Z_L}} \cdot I_{IN} \quad (18.b)$$

$$I_L = \frac{\frac{1}{Z_L}}{C+\frac{D}{Z_L}} \cdot I_{IN} \quad (18.c)$$

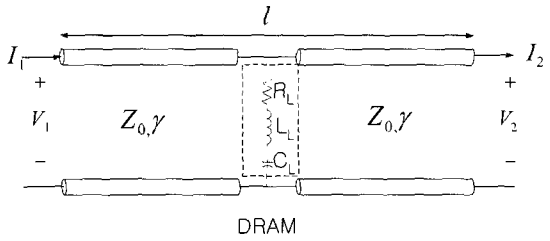


Fig. 10. A unit section of loaded transmission.

When circuit blocks are connected in cascade, the resultant ABCD matrix is the matrix multiplication of the ABCD matrix of each circuit block. Fig.10 shows a cascade connection of a unloaded transmission line of length $l/2$, a DRAM input pin loading, and another unloaded transmission line of length $l/2$. The ABCD matrix which relates $[V_1,I_1]$ and $[V_2,I_2]$ can be written as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh\left(\gamma \cdot \frac{l}{2}\right) & Z_o \sinh\left(\gamma \cdot \frac{l}{2}\right) \\ \frac{1}{Z_o}\sinh\left(\gamma \cdot \frac{l}{2}\right) & \cosh\left(\gamma \cdot \frac{l}{2}\right) \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ Y_L & 1 \end{bmatrix} \cdot \begin{bmatrix} \cosh\left(\gamma \cdot \frac{l}{2}\right) & Z_o \sinh\left(\gamma \cdot \frac{l}{2}\right) \\ \frac{1}{Z_o}\sinh\left(\gamma \cdot \frac{l}{2}\right) & \cosh\left(\gamma \cdot \frac{l}{2}\right) \end{bmatrix} \quad (19)$$

$$Z_o = \sqrt{\frac{(R+j\omega L)}{(G+j\omega C)}} \quad (20.a)$$

$$\gamma = \sqrt{(R+j\omega L)(G+j\omega C)} \quad (20.b)$$

$$Y_L = (R_L + j\omega L_L + \frac{1}{j\omega C_L})^{-1} \quad (20.c)$$

Another advantage of the ABCD matrix method is that

the V, I at any position of transmission line can be derived analytically in terms of the source variables.

Comparison of an AC response for the 32nd DRAM chip in a Rambus channel shown in Fig.11 demonstrates an excellent match between the ABCD matrix method and the HSPICE simulation using a lossy transmission line model(W-model).

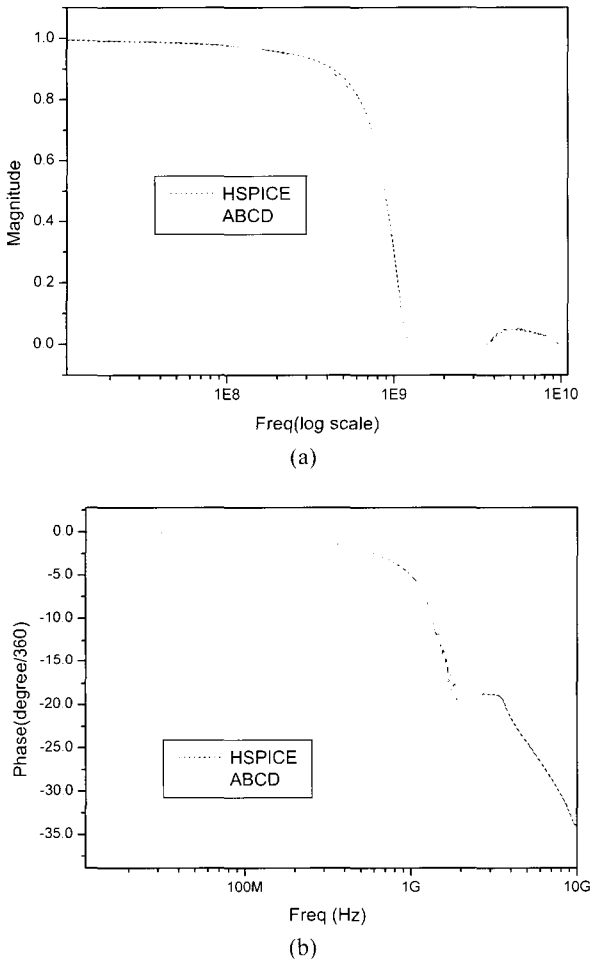


Fig. 11 Comparison of AC responses of D- Direct-Rambus channel using the ABCD matrix and HSPICE.

The steps to get the eye patterns of output signal using the ABCD matrix method are shown in Fig.12. A 7-bit PRBS (pseudo random binary sequence) signal is used to generate a unique bit pattern with a period of 127 bits. In the signal waveform shown in Fig. 4, the period T is set to 127 clock cycles and the duty cycle d is set to 1/127. Combination of the 7-bit PRBS bit-pattern and the frequency spectrum shown in Eq.(5) gives the frequency spectrum of the incident PRBS signal. Multiplication of some ABCD matrices to the frequency spectrum of the PRBS signal gives the frequency spectrum of the output signal. The inverse Fourier transform on the resultant frequency spectrum gives the time-domain eye pattern of the output signal.

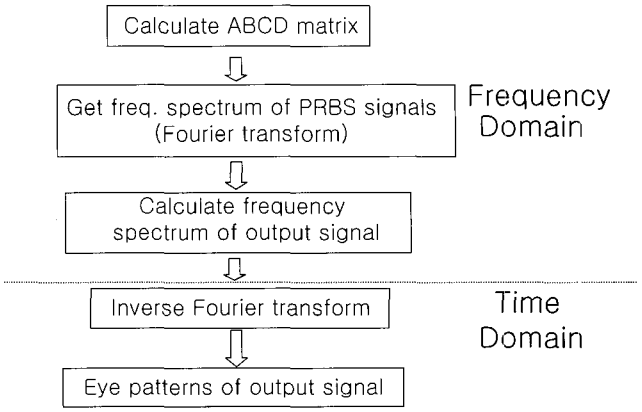


Fig. 12. Steps for eye pattern generation using the ABCD matrix method.

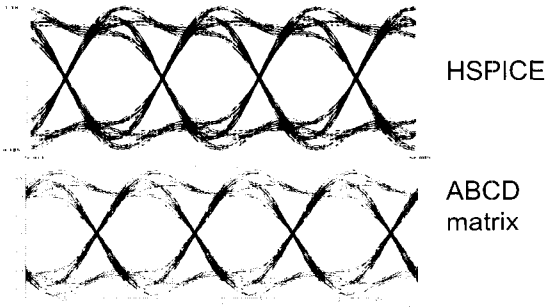


Fig. 13. Comparison of eye patterns generated by HSPICE and the ABCD matrix method (32nd DRAM chip in D-Rambus channel)

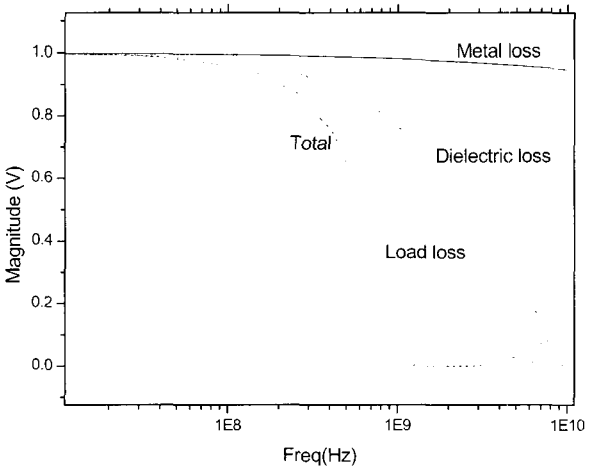


Fig. 14. Losses versus frequency in the uniformly loaded transmission line (32nd DRAM in D-Rambus)

Fig.13 shows the comparison of eye patterns generated by HSPICE(*W*-model) and the ABCD matrix method for the output voltage at the 32nd DRAM pin from the controller when a 7-bit PRBS signal is applied at the controller output in the Direct-Rambus channel. Exact match can be found between the two methods.

Table 3. Parameters for a loaded transmission line used in the calculation of Fig. 14.

Dielectric material	FR-4
Z_0	45Ω
Metal width(W)	31mil
Metal thickness	14mil
Dielectric thickness	1.37mil
ε_R	4.8
L	0.28uH/m
C	0.14nF/m
Z_{eff}	28Ω
G_d	30.66pS/Hz/m
R_s	41.1mΩ/$\sqrt{Hz}$/m
R_L	10Ω
C_L	2.2pF
L_L	4nH

E. *Comparison of loss mechanisms*

In the uniformly loaded transmission line shown in Fig.8.(a), there are three kinds of loss mechanisms. They are the skin effect loss, the dielectric loss, and the load loss. The load loss is generated by the DRAM input pin impedance. The attenuation constants due to the skin effect loss, the dielectric loss, and the load loss are proportional to $\sqrt{f}$, f, f^2 as can be seen in Eq.(10.a), Eq.(14.a), and Eq.(15) respectively. Thus the load loss will be dominant at extremely high frequencies. However, the cross-over frequency of the three loss mechanisms depends on the geometry of transmission line. When the transmission line width W is small, the skin effect loss is dominant over the other two losses over a wide frequency range. Fig.14 shows the attenuation due to the above-mentioned three loss mechanisms. The ABCD matrix method was used for the calculations. The parameters used in the loss calculation of Fig. 14 are shown in Table 3.

VI. Transmission Characteristics of SDRAM Bus Channels

SPICE simulations were performed to get the AC response and the eye patterns for the PC-133, Direct-Rambus and SSTL-2 SDRAM bus channels. A lossy transmission line model (*W*-model) was used in the SPICE simulations.

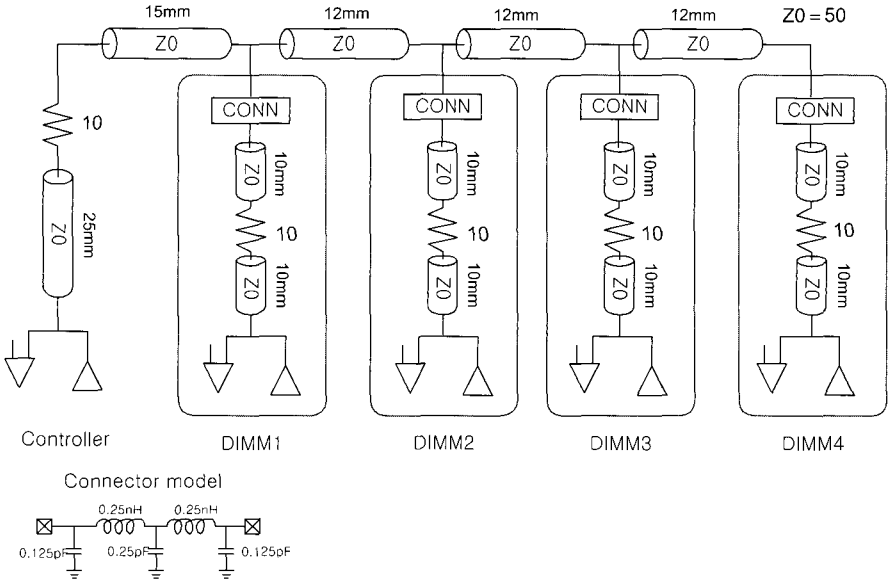


Fig. 15. A PC-133 SDRAM bus channel.

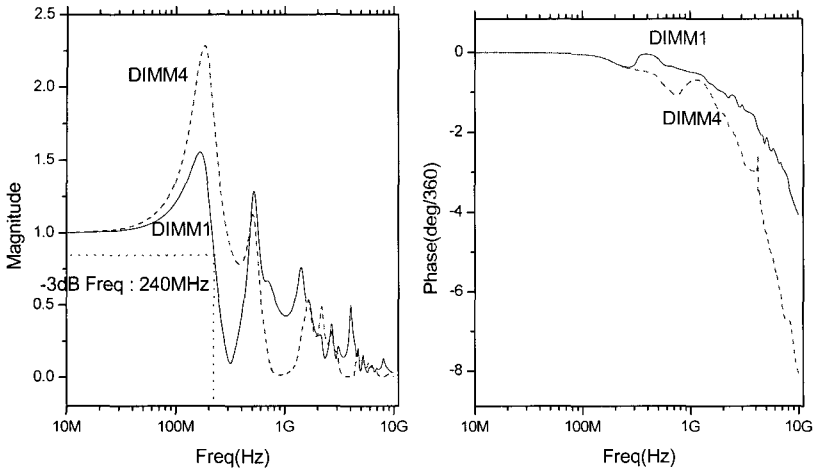


Fig. 16. AC response of a PC-133 channel.

Table 4. LVTTL specifications.

V_{IL}	V_{IH}	V_{OL}	V_{OH}
≤ 0.8V	≥ 2.0V	≤ 0.4V	≥ 2.4V

Table 5. Parameters of a 50Ω transmission line.

Dielectric material	FR-4
Z_0	50Ω
Metal width(W)	26mil
Metal thickness	14mil
Dielectric thickness	1.37mil
ε_R	4.8
L	0.32uH/m
C	0.12nF/m
G_d	27.07pS/Hz/m
R_s	50.2mΩ/$\sqrt{Hz}$/m

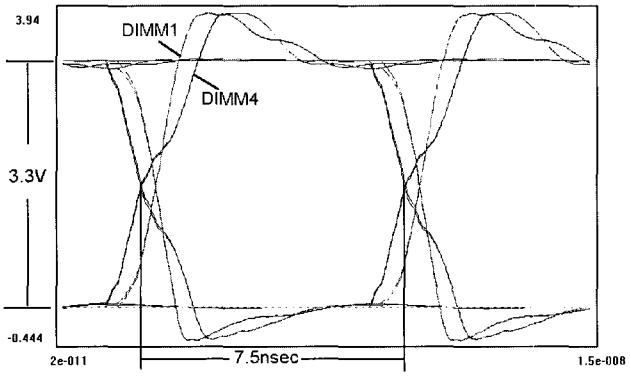


Fig. 17. Eye pattern of a PC-133 channel.

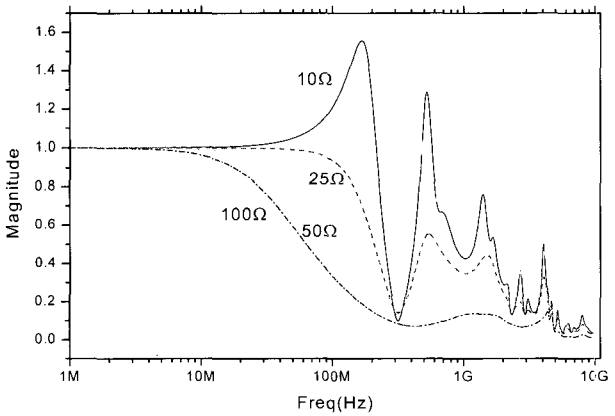


Fig. 18. AC response of a PC-133 channel at DIMM1 with different values of R.

A. *PC-133*

Fig. 15 shows one of 64 bidirectional data channels in a PC-133 SDRAM bus interface system shown in Fig. 1[5,16-17]. Full-swing (0, 3.3V) output drivers are used to drive the channel. Output voltage levels follow the LVTTL standard shown in Table 4. Channels are not terminated. 10Ω series resistors are used as damping resistors to reduce reflections. The geometry and electrical parameters of transmission line used in this

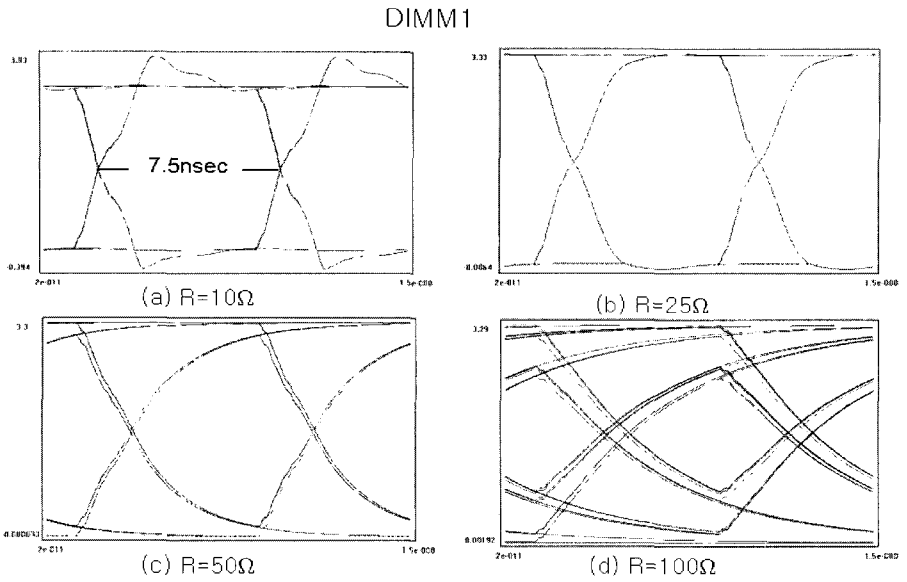


Fig. 19. Eye patterns of a PC-133 channel at the data rate of 133Mbps for different values of R (a) 10Ω, (b)25Ω, (c) 50Ω, (d) 100Ω.

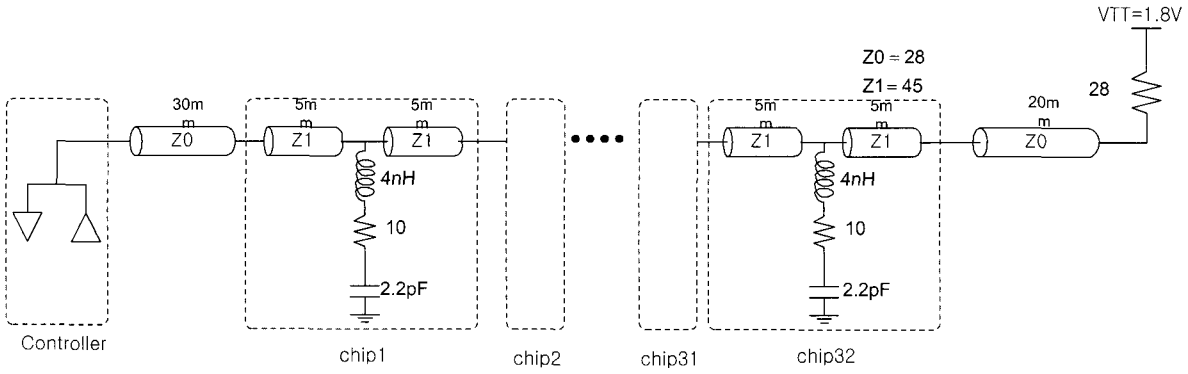


Fig. 20. A Direct-Rambus channel.

simulation are shown in Table 5. IBIS model[22] was used for the input and output drivers of SDRAM and memory controller.

Table 6. Effect of damping resistor R in a PC-133 channel.

Damping R	f_{-3dB}	Time of flight (t_f)
10 Ω	237 MHz	1.15ns
25 Ω	169 MHz	1.37ns
50 Ω	79.3 MHz	2.02ns
100 Ω	37.2 MHz	3.66ns

Fig. 16 shows the AC response of a PC-133 channel. The worst case –3dB frequency is 240 MHz, which corresponds to the data rate of 480 Mbps. This predicts that the PC-133 channel won't experience much ISI (inter symbol interference) until the data rate is lower than 480 Mbps. Fig. 17 shows the eye patterns of voltage signals at SDRAM pins when a PRBS voltage signal is applied at the memory controller. Since the data rate is 133 Mbps and it is much lower than the –3dB data rate of 480 Mbps, there are no ISI components (spreads in the time axis) in the eye pattern. The rise time of the input signal from 0 to 3.3V is set to 1ns in the SPICE simulations. The 10 Ω damping resistor in Fig. 15 reduces the high-frequency reflections. Increasing the resistance value of this damping resistor reduces both reflections and the f_{-3dB} frequency, as shown in Fig. 18 and Fig. 19. The reduction of f_{-3dB} below 66 MHz

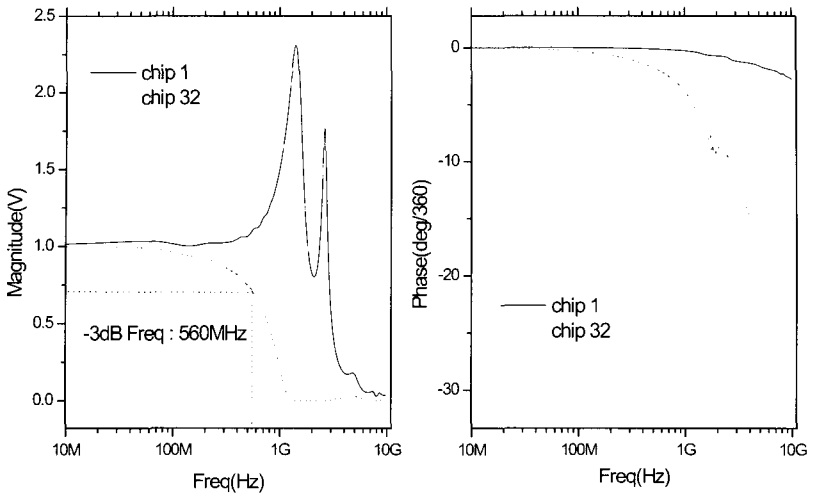


Fig. 21. AC response of a Direct-Rambus channel.

Table 7. Specification on the *R, L, C* values of a DRAM input pin.

	C_{kin}	ΔC_{in}	L	ΔL	R
PC-133	5.3pF	-	3.3nH	-	-
SSTL-2	4.5pF	± 0.5pF	3.98nH	-	-
D-RAMBUS	2.2pF	± 0.06pF	4nH	1.8nH	10 Ω

results in the ISI components at the data rate of 133Mbps as shown in Fig. 19 (d) for the case of R=100 Ω , where the signal cannot change by a full swing (3.3V) during one clock period (T_{cycle}). When R is 25 Ω , the reflected signals almost disappear due to the series terminations as in the SSTL case.

The disadvantage of increasing the value of damping resistor R is that it increases the time of flight t_f due to the increase of RC time constant. Table 6 tabulates the values of f_{-3dB} and t_f at different values of R.

B. *Direct-Rambus*

Fig. 20 shows a Direct-Rambus channel, where up to 32 Rambus DRAM chips are connected directly to a transmission line without stubs. The series connection of a 4nH inductor, a 10 Ω resistor and a 2.2pF capacitor represents the impedance of a Rambus DRAM pin. The characteristic impedance (Z_1) of the base transmission line where DRAM chips are connected is set to a value between 40 Ω and 60 Ω . The characteristic impedance (Z_0) of the transmission lines where DRAM chips are not connected is set to 28 Ω . The effective characteristic impedance of the transmission lines where DRAM chips are connected is set to be 28 Ω by adjusting the DRAM spacing ℓ , such that $Z_1/\sqrt{1+(2.2p/(C\cdot\ell))}$ =28 Ω , where C is the capacitance per unit length of the base transmission line without DRAM chips attached, and ℓ is the distance between DRAM chips[18]. The geometry and electrical parameters of the transmission line used in this simulation are shown in Table 3.

The mismatches in the values of capacitance, inductance and resistance of input pin shown in Fig.20 gives a variation of time of flight (Δt_f) which slows down the operating speed as shown in Eq. (2). To reduce Δt_f , the Rambus interface standard requires a very tight criterion especially in the mismatches of input pin capacitance(ΔC). Table 7 shows the specifications of the values of capacitance, inductance and resistance of a DRAM input pin for the three SDRAM interface standards. SPICE simulation for the Direct-Rambus interface specification showed that the worst case Δt_f is about 70ps between the two cases when the input pin capacitance is 2.2+0.06pF at all 32 DRAMs attached to a Rambus channel and when it is 2.2-0.06pF at all 32

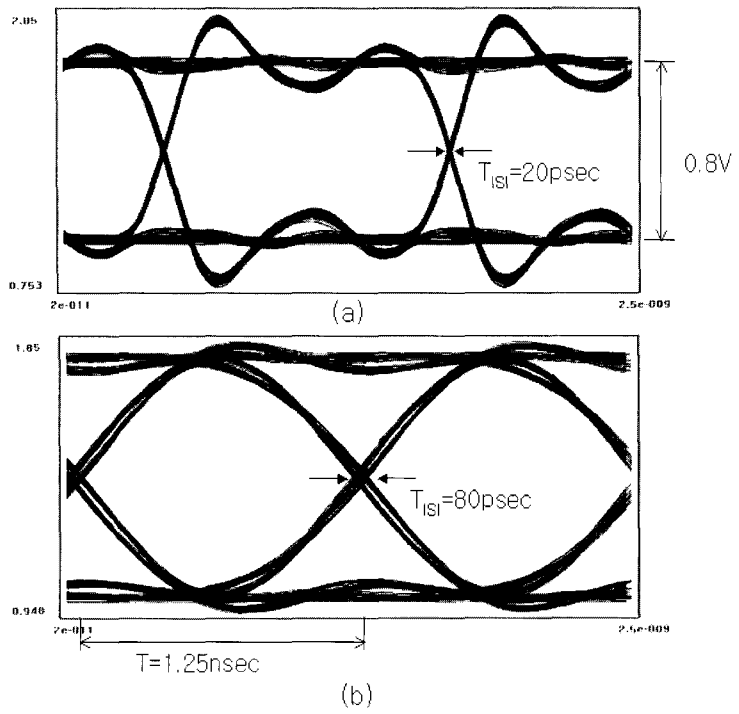


Fig. 22. Eye patterns of a Direct-Rambus channel (a) chip1 (b) chip32.

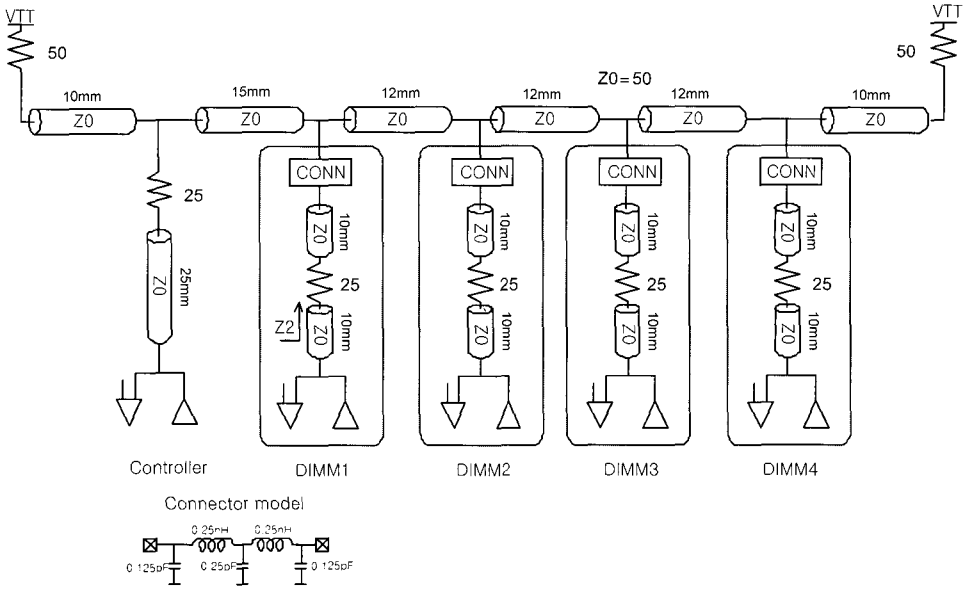


Fig. 23. A SSTL-2 (PC-266) channel.

DRAMs, and that the worst case Δt_f for the variations of input pin inductance is 30ps. The sum of these two Δt_f values must be accounted for in the Δt_f specification of 200ps shown in Table 2, along with the Δt_f values due to the ISI(inter symbol interference), the PCB layout error and the crosstalk noise.[12]

Fig. 21 represents the AC response of a Direct-Rambus channel from SPICE simulations. The input signal is applied at the memory controller output. Chip 1 represents the closest DRAM chip from the memory controller. Chip 32 represents the 32nd DRAM chip (the farthest DRAM chip) from the memory controller. Fig. 22 shows the eye patterns of a Direct-Rambus channel at chip 1 and chip 32 at the data rate of 800Mbps. The time

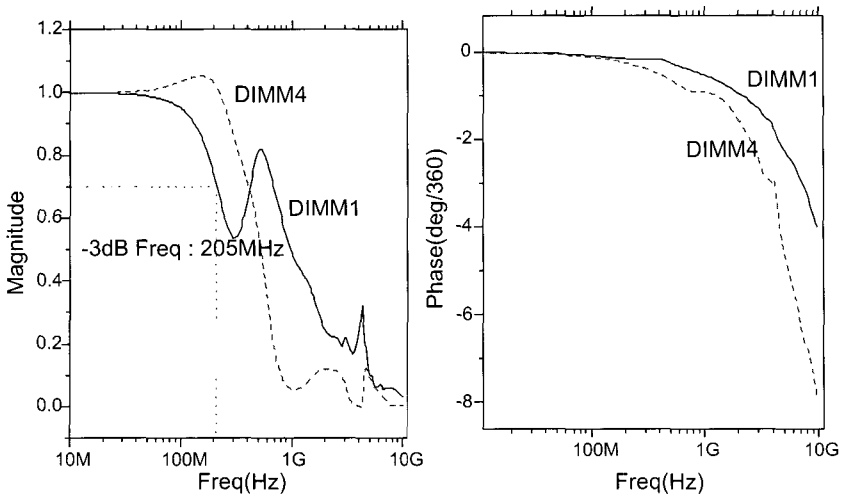


Fig. 24. AC response of SSTL-2 channel.

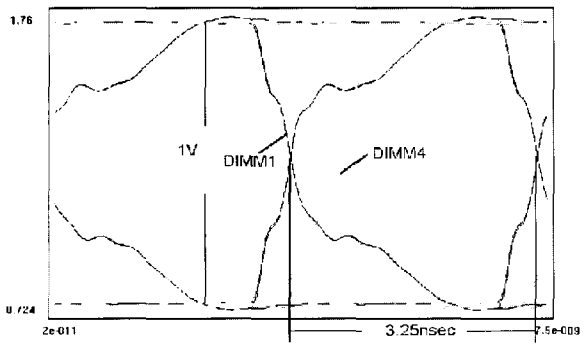


Fig. 25. Eye pattern of SSTL-2 channel.

Table 8. Comparison of f_{-3dB} and power consumption of a Direct-Rambus channel when $Z_0 = 28\Omega$ and 50Ω.

Z_0	f_{-3dB}	Power consumption
50 Ω	388 MHz	15mW
28 Ω	560 MHz	27mW

jitter due to ISI is 20ps and 80ps for chip 1 and chip 32, respectively. The time jitter due to ISI is generated by the bandwidth limitation of channel.

The predecessor of the Direct-Rambus standard is the Concurrent-Rambus, where the effective characteristic impedance (Z_0) of transmission line is 50 Ω and the data rate is 600 Mbps. In the Direct-Rambus standard, Z_0 is reduced to 28 Ω to increase the data rate to 800 Mbps. However the power consumption is larger for Z_0 =28 Ω than for Z_0 =50 Ω. Table 8 shows the comparison of f_{-3dB} and the power consumption when Z_0 is 28 Ω and 50 Ω in a Direct Rambus channel. Z_0 is the effective characteristic impedance and also the value of termination resistors. f_{-3dB} was calculated from the SPICE simulation for the 32nd DRAM position.

C. *SSTL-2*

Fig. 23 shows a SSTL-2 SDRAM channel. Parallel terminations were done at both ends of the channel on the main board by using two 50 Ω resistors. Also the series terminations were done by 25 Ω resistors. The stub of length 10mm on a DIMM card is required for the electrical connection between the connector and the SDRAM chip located on a DIMM card. Neglecting the length of the upper stub (the stub closer from connector) on a DIMM card, the impedance Z_2 looking up into the 25 Ω resistor is 25+(Z_0 / 2) = 50 Ω [17]. Thus there is no reflection for the signals going up into the main transmission line from the DIMM card. The geometry and electrical parameters of transmission line used in this simulation are the same as those of PC-133, which were shown in Table 5. IBIS model was used for the I/O drivers of SDRAM.

Fig. 24 shows the AC response of a SSTL-2 channel from SPICE simulations. The worst case f_{-3dB} is 205 MHz, which corresponds to the data rate of 410 Mbps. Fig.25 shows the eye pattern of a SSTL-2 channel at the data rate of 266 Mbps. Since the data rate is lower than 2* f_{-3dB}, there are no ISI (Inter Symbol Interference) components observed in the eye pattern.

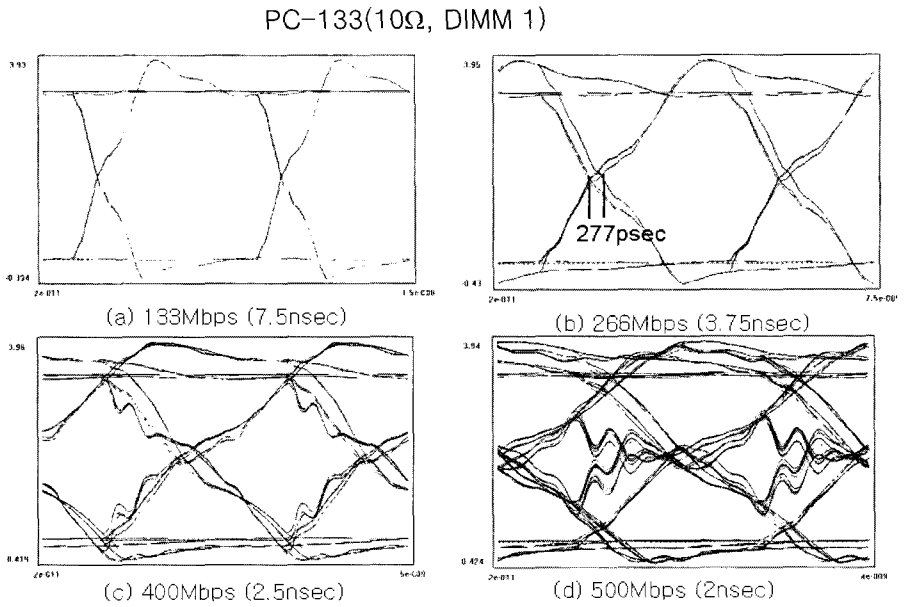


Fig. 26. Eye patterns of a PC-133 channel (R=10Ω) at different data rates.

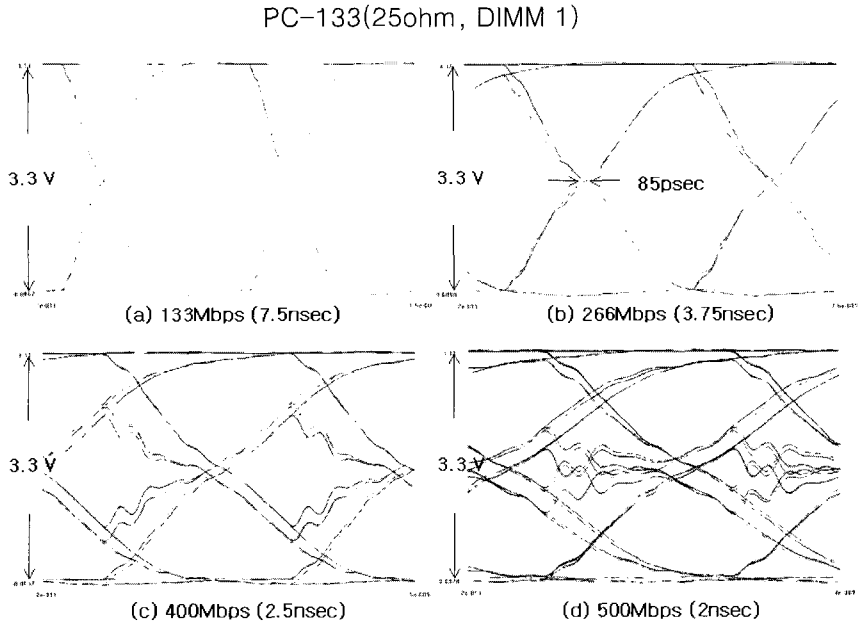


Fig. 27. Eye patterns of a PC-133 channel (R=25Ω) at different data rates.

D. *Data Rate Bottlenecks*

To find whether the channel is the bottleneck in increasing the data rate for the three SDRAM bus interface standards mentioned before, eye patterns were generated by SPICE simulations at the data rates higher than the standard rate shown in Table 1.

Fig. 26, Fig.27, Fig.28 and Fig. 29 show the eye patterns for the PC-133 with R=10 Ω , the PC-133 with R=25 Ω , the Direct-Rambus and the SSTL-2 channels, respectively. As long as the eye patterns are concerned, the PC-133 is expected to work at the data rates up to 266 Mbps (twice the standard data rate), as can be seen from Fig. 26 and Fig. 27. At the data rate of 266 Mbps, the PC-133 channel with R=25 Ω gives cleaner but slightly smaller eyes than the PC-133 channel with R=10 Ω , as shown in Fig. 26 and Fig. 27. However, the time jitter is much larger for the case of R=10 Ω .

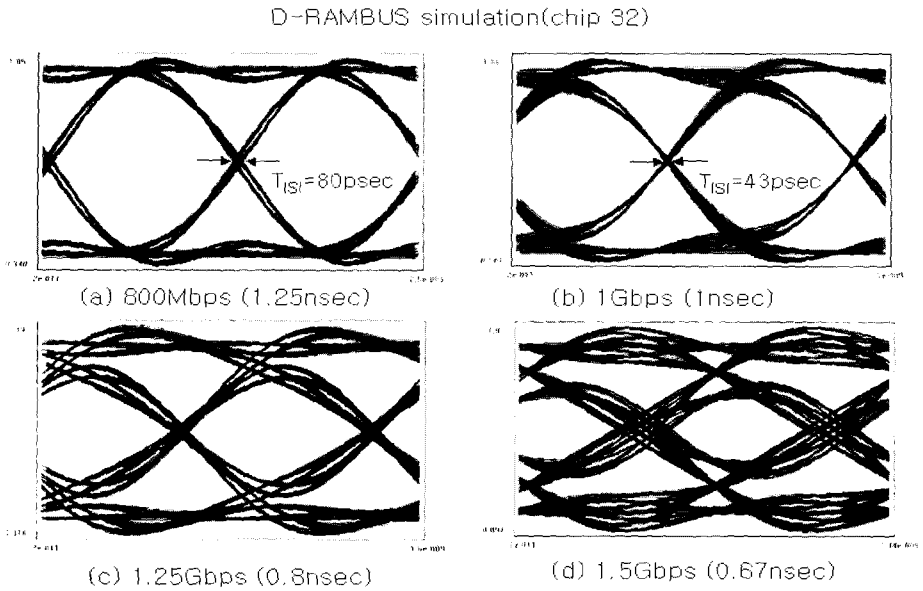


Fig. 28. Eye patterns of a D-Rambus channel at different data rates.

Table 9. Trends of SDRAM bus interface.

	PC-133	D-Rambus, SSTL-2	Future
Clock	Common clock	Source Synchronous	Modified Source Synchronous[25,26], CDR[27,28]
Signaling Scheme	Single-Ended 3.3V(LVTTL)	Single-Ended, 0.8V, 1V	Differential 0.35V (LVDS[29])
DRAM Connection	Multi-drop	Multi-drop	Point-to-Point

Although the time jitter is caused by reflections for the case of R=10 Ω, it is caused by ISI (inter symbol interference) due to the bandwidth limitation for the case of R=25 Ω. Therefore it is expected that there is an optimum value of the damping resistor R in the range between 10 Ω and 25 Ω, with respect to time jitter, eye opening and channel delay t_f (Table 6). The Direct-Rambus channel is expected to work at the data rates up to 1Gbps (25% larger than the standard rate), as can be seen in Fig. 28. The SSTL-2 channel is expected to work at the data rates up to 333 Mbps (25% larger than the standard data rate), as can be seen in Fig. 29. Therefore the channel is not a bottleneck in increasing the data rate.

Although the channels have some margins in data rate, it is difficult to increase the data rate beyond the standard rate shown in Table 1 due to the timing constraint shown in Table 2. The clock-to-output delay (t_{AC} or Δt_{AC}) shown in Table 2 is related to the output circuitry. The setup and hold times are related to the input circuitry. It can be seen from Table 2 that the above-mentioned delays related to the input and output circuitry dominate the time budget. Therefore more works are required to improve the input and output circuitry to increase the data rate, especially for the PC-133 and SSTL-2 channels.

V. Recent Progress and Future Trend

Recently, the Rambus company proposed a multi-level PAM (pulse amplitude modulation) scheme where 4-level digital data are used instead of binary data. Although this scheme can save the bandwidth, it is

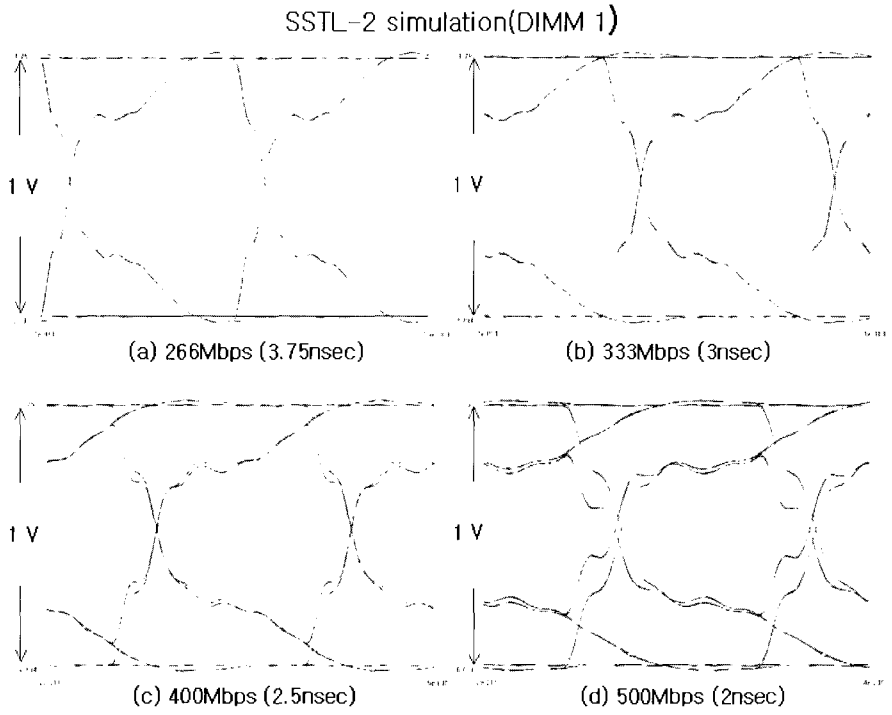


Fig. 29. Eye patterns of a SSTL-2 channel at different data rates.

losing in noise margin. The 2Gb/s transmission was demonstrated with four DRAM chips by sending data at the symbol rate of 1Gsymbol/s[23]. However, it is not clear whether this scheme can be practically used in the near future due to the noise margin problem.

Although it is difficult to predict the future trends, it is expected that the SDRAM bus interface standard will follow the trends shown in Table 9 [24].

A clock signal is required for the SDRAM operation. In the PC-133 standard, a common clock is distributed to all chips from a clock source, as shown in Fig. 1. In the Direct-Rambus and SSTL-2 standards, the clock or data-strobe line follows the data lines in PCB layout to reduce the mismatch in time of flight Δt_f. This clocking method of D-Rambus and SSTL-2 is called the source synchronous clocking, which means that the data and clock (or data-strobe) signals start at the same time from the source and reach the destination at the same time since they follow the same length of transmission lines. However, there is a pin-to-pin skew due to the mismatches in loadings and the transmission line length. To compensate for this pin-to-pin skew, modified source synchronous clocking schemes were proposed [25, 26]. During the setup stage after the power-on, the pin-to-pin skew was measured by sending clock signals from both clock and data pins of the controller chip, and comparing the timing differences between the received clock and data signals of each pin at each DRAM chip. The timing difference with respect to clock at each pin of a DRAM chip is recorded as digital data, which are used to generate an optimum clock by interpolation from the multi-phase clocks generated by DLL. This generated clock is used to synchronize data at the controller [25] or at a DRAM chip[26].

In the future, the CDR(clock data recovery) is expected to be used for synchronization of data and clock signals of SDRAM bus. Since the CDR scheme extracts the clock signals from data, there is no longer a synchronization problem between data and clock. However, it requires a CDR circuitry for each data pin of SDRAM chip. Due to this hardware overload, it is not clear whether the SDRAM interface will use the CDR scheme or not.

Since many parallel data lines are used in SDRAMs, a single-ended signaling scheme is being in used in the SDRAM bus interface channels. Also the multi-drop scheme is being used to increase the memory capacity of SDRAMs. If the data rate increases beyond 2Gb/s, the SDRAM bus interface standard is expected to use a differential signaling scheme with a point-to-point

connection. This trend was already confirmed in the PCI parallel bus of personal computers. Due to the barrier in performance enhancements, the PCI bus is expected to be replaced by a differential bus with a point-to-point connection such as InfiniBand [27] or RapidIO[28].

V. Conclusion

High-speed signaling methods for SDRAM bus interface were reviewed in terms of the timing budget and the transmission characteristics along the physical transmission lines. Three SDRAM bus interface channels which are widely used at the present time are chosen for comparison. They are the PC-133, the Direct-Rambus, and the SSTL-2 channels. Timing budgets were analyzed in term of the clock-to-output delay (t_{Ac}, Δt_{AC}), the input delay (setup time and hold time), the channel delay (t_f, Δt_f), and the clock skew (t_{skew}). Loss mechanisms of transmission lines and the effective the characteristic impedance method for uniformly-loaded transmission line analysis were reviewed. The ABCD matrix method was proposed as an analytic and yet accurate method for the analysis of SDRAM bus channels. The transmission characteristics were analyzed for the above-mentioned three SDRAM bus channels by using the AC responses and the eye patterns generated from SPICE simulations. In the PC-133 channel, it was suggested that the value of the series damping resistor of $10\,\Omega$ is not optimum in terms of data rate, and that the optimum value lies between $10\,\Omega$ and $25\,\Omega$. The recent progress and future trend for SDRAM bus interface standards were reviewed. At the data rate beyond 2Gb/s, it is expected that the SDRAM bus interface standard will likely be changed to a differential scheme with point-to-point connection.

Acknowledgment

This work was supported by Samsung Electronics Company, IDEC and the BK 21 program of the Ministry of Education and Human Resources Development of Korea. The authors thank Prof. Young Hee Kim of Changwon National University for helpful discussions.

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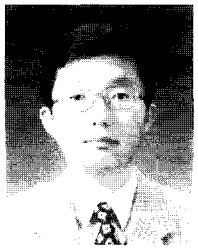

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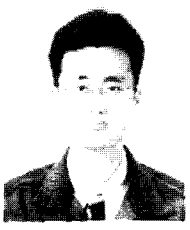

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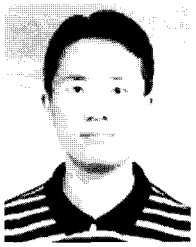

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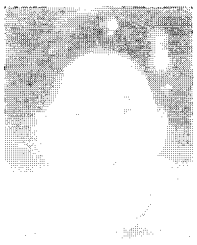

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