A Technique for Analyzing LSI Failures Using Wafer-level Emission Analysis System

Yasuhisa Higuchi, Yasumasa Kawaguchi, and Tatsumi Sakazume

Abstract—**Current leakage is the major failure mode of semiconductor device characteristic failures. Conventionally, failures such as short circuit breaks and gate breakdowns have been analyzed and the detected causes have been reflected in the fabrication process. By using a wafer-level emission-leakage failure analysis method (in-line QC), we analyzed leakage mode failure, which is the major failure detected during the probe inspection process for LSIs, typically DRAMs and CMOS logic LSIs. We have thus developed a new technique that copes with the critical structural failures and random failures that directly affect probe yields.**

Index Terms—**Emission microscope, standby current failure, hot carrier injection mechanism, inverted confoca-laser microscope.**

I. INTRODUCTION

Recently, semiconductor devices have come to be developed and fabricated in a short period of time. However, as wiring is further miniaturized, locating failures has become difficult, and the failure analysis time has consequently increased. Conventionally, several analysis methods have been employed to reduce the time required to develop new products and stabilize the mass production yield. For example, CIM (Computer Integrated Manufacturing) data is compared based on the wafer inspection and probe inspection results. Direct physical analysis based on the FBM (Failure Bit Map) is another measure for the analysis. To concurrently develop a failure analysis technique for new devices, strategic development is required. This strategic development is very important especially for the development of element techniques, for the introduction of equipment and for the accumulation of various know-how. By promoting this failure analysis activities based on the experiences and in corporation with equipment manufacturers as in Fig 1, we can suppress the cost and reduce the time as required.

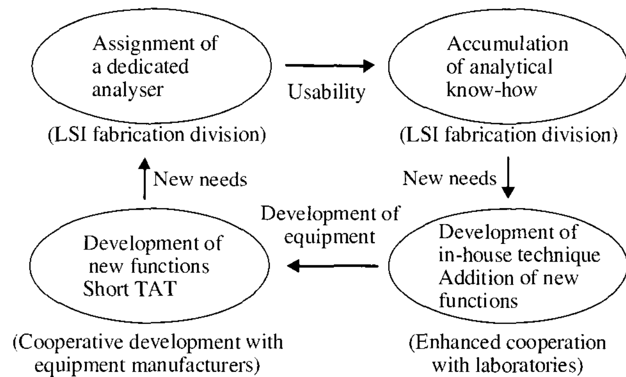

Fig. 1. Failure analysis activities.

Emission analysis has been an effective method of analyzing the leakage mode failures that occupy the greater part of LSI pellet inspection failures[1,2,3]. Most of standby current failure, EASY/DC failure and minor bit failure are causes of leakage mode failure of short circuit, breakage and gate breakdown (Fig 2, Table 1). In emission analysis, a highly sensitive camera is used to detect faint lights. These faint lights are generated by hot carriers (Fig 3), plasma leakage or latch up. Plasma leakage induced faint light is observed when an electric field is concentrated on abnormal sections in a semiconductor device and latch up induced light is infrared. According to the emission points, failure points in a transistor are located. The failure-point hit rate is estimated to be 95% or higher and the technique is very effective. In current LSIs, however, metal wiring has a

Manuscript received February 10, 2001; revised March 12, 2001.
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Table 1. Failure modes and its positioning by emission analysis.

Reason of failure	Origin	Positioning
Stand by current failure	Gate breakdown	Possible
	Short circuit between wiring	Impossible
	Wiring break	Depends on the case
	Breakdown by static electricity	Possible
DC/EASY failure	Gate breakdown	Possible
	Short circuit between wiring	Impossible
	Wiring break	Depends on the case
Minor bit failure	Diffusion leakage	Possible
	High contact resistance	Impossible

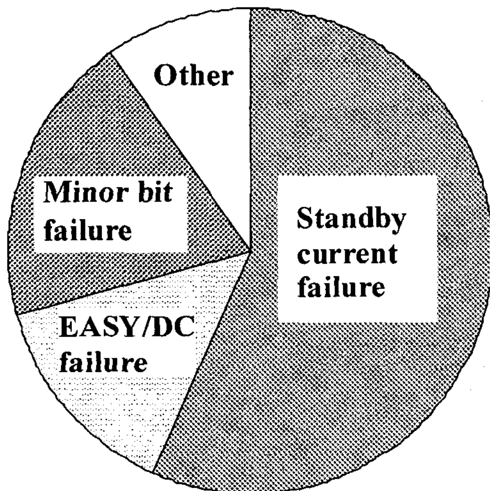


Fig. 2. Contents of pellet-inspection failure of general purpose DRAMs.

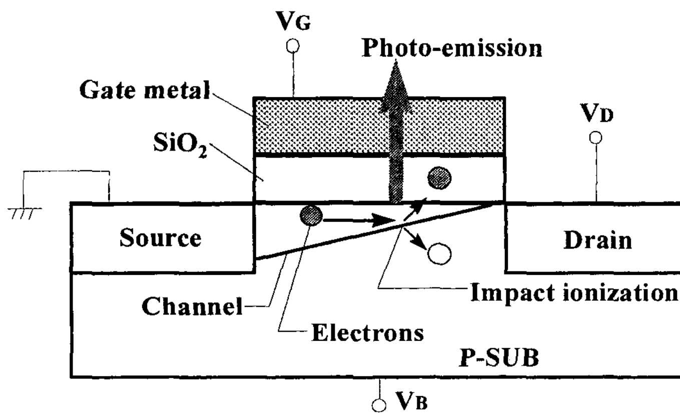


Fig. 3. Hot carrier injection mechanism.

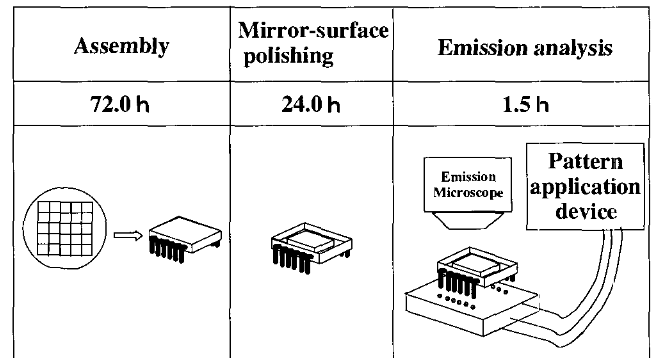


Fig. 4. Emission analysis flow using the conventional technique(Flip-chip).

multilayer structure, and pellets are configured for flip-chip mounting. Therefore, it is difficult to observe LSI from its surface. In addition, failures do not appear without applying signal patterns to LSI. So, in the conventional technique, a signal is applied to a package. Moreover, a pre-processing is required to apply signals to assembled LSI and to observe an emission image from the back of the chip. This increases the number of fabrication steps and costs. There was thus a real demand for the development of shorter analysis TAT. An example of the pre-processing that is required to observe an emission image by using the conventional flow is shown in Fig 4. The purpose of this work is to reduce analysis TAT by introducing wafer level emission leakage failure analysis method. The target of analysis TAT was set to spend less than half a day which is roughly 1/8 of the time currently needed.

II. PERFORMANCE AND FUNCTION OF THE NEW TECHNIQUE

We have developed a wafer-level emission leakage failure analysis system (Fig 5). This is a system whereby signals are applied by a probe that makes contact with the upper surface of the wafer, the pattern image is taken by a camera from the back surface via a glass stage using an inverted laser microscope. The emission image is observed using an infrared detector, and both images are then overlaid. For the improvement of productivity and cost reduction, the prober specification was determined as a maximum of 800 bonding pads and 4000 CCB(Controlled and Collapsed Bonding) bumps. This enables us to use the same probe card as is used in mass production probe test step, such as cantilever or spring probe. Conventionally, the failure analysis TAT in packaged form (from assembly to pre-processing for analysis) has been about 100 hours. The new technique has significantly reduced the process time, to about 2.5 hours. In addition, as all the area over the wafer is analyzed, it becomes possible to compare the failure analysis data with the other inspection data. The relationship between failure distribution and foreign particles distribution, for example, may give us an information if the failure is originated from particle. Same comparison is also possible for a registration data. By using this technique, the position of structural failure that causes leakage at both developmental and production stage can be located immediately. The resulting data can be smoothly reflected in the process that causes failure.

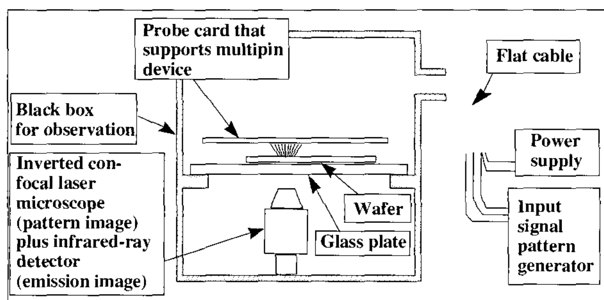


Fig. 5. Overview of wafer-level emission leakage failure analysis system.

We have developed the following two techniques. One is a technique in which a signal application probe makes contact with the upper surface of a wafer and the data is analyzed from the back surface of the wafer via a glass stage, the other is a emission data detection technique. By the way, There are two inherent disadvantages in this new technique in comparison with the conventional technique. They are optical aberrations and pattern inversion and both of them comes from the concept of the new technique: back side analysis. They were, however, solved by superimposing two sets of images: the pattern images obtained by using a inverted laser microscope, and the emission image obtained by using an infrared detector.

The following shows the performance and the function of this system.

Wafers to be analyzed

It must be possible to analyze 125-mm wafers and 200-mm wafers. A maximum of 800 pads and 4000 CCB bumps must be supported.

Probing method

The cantilever or spring probe used in probe inspection must be supported. The probe card must be the same as that used on the actual fabrication line.

Alignment method

The X, Y and Z directions of the stage must be adjustable. The alignment conditions must be observed on a monitor.

Placement of wafers

Both 125-mm wafers and 200-mm wafers must be fixed in place by vacuum suction at the wafer's periphery.

Camera-shooting function

An emission image is captured from the wafer's back surface by using a C-CCD(Cooled-Charge Coupled Device). The wave-length of an emission image ranges from 300 nm to 1100 nm. Even a large chip can be observed within a single screen at a minimum magnification (x 0.5). When capturing a pattern image from the back of the wafer, infrared laser that is not affected by the wafer's thickness must be used. Both images are then superimposed. Table 2 shows the items that were analyzed when developing the new technique.

Table 2. Items analyzed and considered for the new technique.

No.	Subject	Analyzed Items
1	Degree of mirror-surface of a pattern image and the dependency of wafer thickness on a pattern image	Preparation of sample Pattern image using infrared laser Confirmation of emission image
2	Wafer suction	Degree of wafer warpae Dependence on wafer thickness
3	Thickness of stage glass	Logical calculation of the degree of glass warpage and wafer break when load is applied
4	Stage moving range	Investigation of the probe card and jigs that are currently in use
5	Wafer alignment accuracy	Preparation of cantilever, samples of spring probes, and jigs Confirmation using actual machine

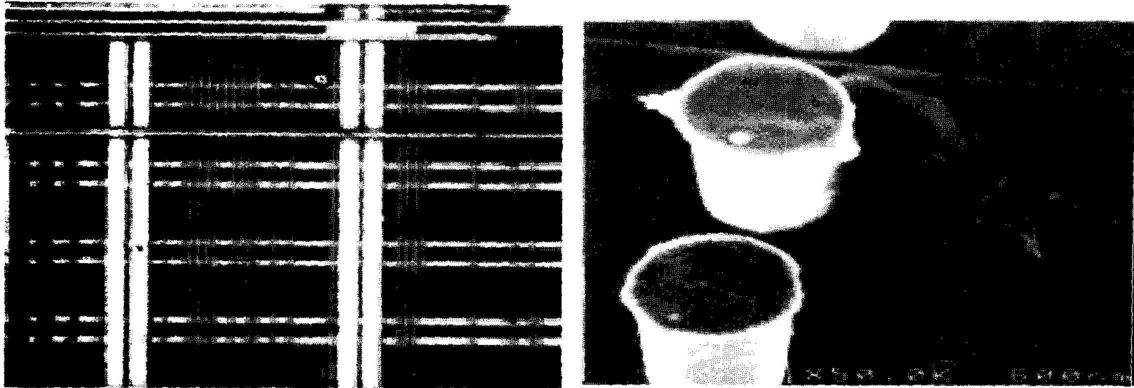


Fig.6. (Example 1) Localization of the failure point by the new technique.

III. Results and Discussion

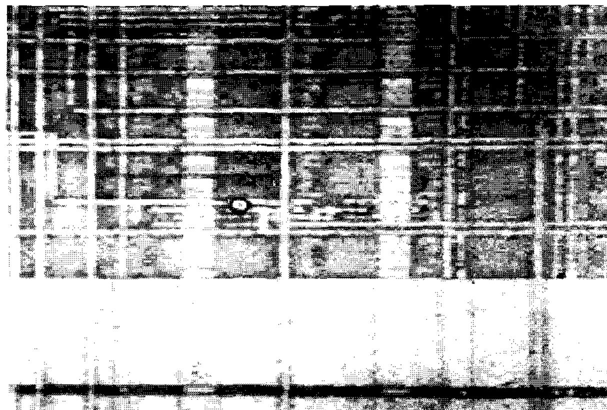
Two examples of analysis by using the new technique are shown in Figures 6 and 7. In the upper column, a photograph showing the results of emission analysis obtained by using this technique is shown. For both examples, the pattern image and emission image of a transistor were observed clearly. The lower column is an SEM photograph in which a light emission point is physically analyzed. In Figure 6, the contact hole plug, at voltage of Vss, is short circuited to gate, at voltage of Vdd, by foreign particle. Figure 7 proves that the gate oxide has in fact broken.

Table 3. Comparison of analysis TATs (man-hours) for conventional and the new.

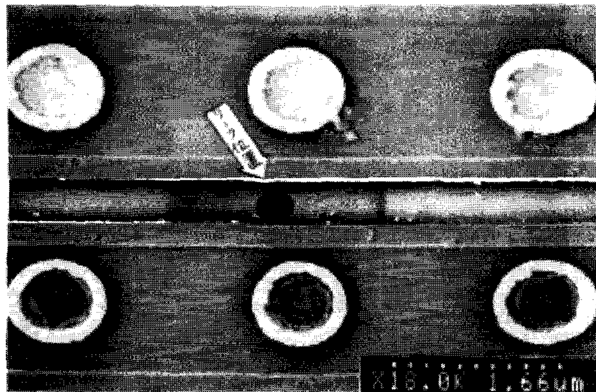
Analysis method	Conventional technique	New technique
Assembly	72.0h	0
Back-surface polishing	24.0h	1.0h
Emission analysis	1.5h	1.5h
Total	97.5h	2.5h

Table 3 is a comparison of analysis TATs (man-hours) Between conventional technique and new technique. By using the new technique, assembly steps can be omitted, and the time required for pre-process-ing(assembling and polishing) and consequently the analysis cost can be

significantly reduced when analyzing failure samples found in the probe inspection step.



(a)



(b)

Fig. 7. (Example 2) Localization of the failure point by the new technique

IV. CONCLUSIONS

We have developed a new wafer-level emission leakage failure analysis method (in-line QC) to locate the position of leakage mode failures, the major type of failure detected in the probe inspection step for LSIs, typically DRAMs and CMOS logic LSIs. By using this technique, we have reduced the time required to locate the failure position of critical structural failures and random failures that directly affect probe yields to 1/40. As the resulting data identify the point of failure at higher hit rate and show the clearer picture, it can be smoothly reflected into the process that causes failure. By comparing the analyzed data with other wafer scale distribution data as foreign particles or registration, for example, we can add various analytical functions to this technique.

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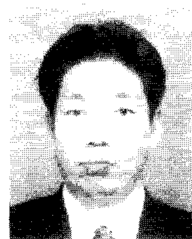

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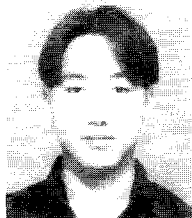

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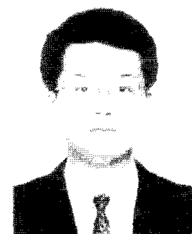

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