Current Status and Prospects of FET-type Ferroelectric Memories

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Abstract— **Current status and prospects of FET-type FeRAMs (ferroelectric random access memories) are reviewed. First, it is described that the most important issue for realizing FET-type FeRAMs is to improve the data retention characteristics of ferroelectric-gate FETs. Then, necessary conditions to prolong the retention time are discussed from viewpoints of materials, device structure, and circuit configuration. Finally, recent experimental results related to the FET-type memories are introduced, which include optimization of a buffer layer that is inserted between the ferroelectric film and a Si substrate, development of a new ferroelectric film with a small remnant polarization value, proposal and fabrication of a 1T2C-type memory cell with good retention characteristics, and so on.**

Index Terms— **Ferroelectric, FeRAM, ferroelectric-gate FET, data retention, $SrBi_2Ta_2O_9$, $(Bi,La)_4Ti_3O_{12}$.**

I. INTRODUCTION

As modern portable electronic devices such as mobile phones and notebook computers become more and more popular, there is a confirmed increase in the demand for non-volatile memories. Among various non-volatile memories, FeRAM (ferroelectric random access memory) has a unique feature such that the power consumption is lowest, and therefore research and development of FeRAM are being conducted actively in many semiconductor companies. So far, FeRAMs with capacities up to 256 kbits have been mass-produced for smart tag and computer game applications. Furthermore, if FeRAMs with several hundreds megabits are produced in the future, they may replace all memories such as DRAM (dynamic RAM), E^2PROM (electrically erasable programmable read only memory), and flash memory, except for high speed SRAM (static RAM).

The memory cell of the present FeRAM is composed of a ferroelectric capacitor and an MOSFET (metal-oxide-semiconductor field effect transistor) for cell selection[1], as shown in Fig. 1(a), and in the "read" operation, voltage pulses with the same polarity are applied to the capacitor and the polarization reversal current of the ferroelectric film is detected. Thus, the stored data are destroyed during the "read" operation and it is necessary to rewrite them at the end of the operation. In the category of FeRAM, there is another type of memory cell called an FET-type, in which a ferroelectric capacitor is replaced with a ferroelectric-gate FET (an FET whose gate insulator film is composed of a ferroelectric material), as shown in Fig. 1(b). In the FET-type cell, the "read" operation is non-destructive, because "0" and "1" data are written in the ferroelectric film as the direction of polarization and they can be readout as a difference of the drain current of the FET. There is also a possibility that the MOSFET for cell selection is omitted in Fig. 1(b) and each cell is composed of a single ferroelectric-gate FET [2], which s particularly important from a viewpoint of high-density integration.

However, fabrication of the ferroelectric-gate FET is very difficult, because the constituent elements in the ferroelectric film easily diffuse into a Si substrate during the annealing process for crystallizing the film. Thus, the electrical properties of the interface become very poor and no commercially available devices have been fabricated yet. In this paper, problems of ferroelectric-gate FETs are first described and the optimum materials, device structure, and circuit configuration for realizing a long data retention time as well as excellent interfacial

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properties are discussed. Finally, the current status of the ferroelectric-gate FETs and related devices are introduced.

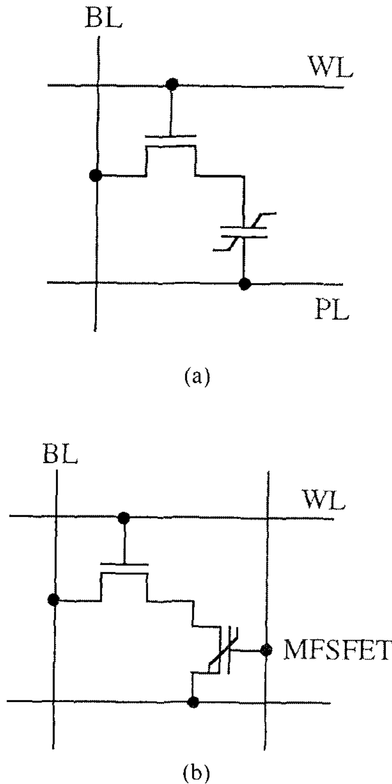

Fig. 1. Circuit configuration of ferroelectric random access memories. (a) Destructive readouttype and (b) Non-destructive readout type. BL, WL, PL, and MFSFET in the figure show bit line, word line, plate line, and an ferroelctric-gate FET, respectively.

II. Key Factors to Improve Data Retention Characteristics

A. *Problems in Ferroelectric-gate FETs*

A typical sheet carrier density in the channel region of a MOSFET is about $2x0^{12}$ cm^{-2}, assuming that t_{OX} = 30 nm and V_G -V_T= 3 V, where t_{OX} is the oxide thickness, V_G is gate voltage, and V_T is the threshold voltage. This value corresponds to a charge density of 0.32μC/cm^2, and thus, in the application to ferroelectric-gate FETs, the remnant polarization value of a ferroelectric film is not necessary to be large, if it is effectively used to induce carriers on the semiconductor surface. However, if a ferroelectric film is directly deposited on a Si surface, it is generally difficult to form a good interface between them, because constituent elements in both materials easily diffuse each other, and because a transition layer is formed at the interface.

In order to improve the interface properties, a buffer layer is often inserted between a ferroelectric film and Si substrate, which is composed of either a dielectric material (MFIS structure, M; metal, F; ferroelectric, I; insulator, S; semiconductor) or a stacked structure of conductive and dielectric materials (MFMIS structure). However, insertion of the buffer layer causes a new problem that the data retention time becomes short, and thus the retention time in most reported results is the order of a few hours, except for the recent studies on MFIS and MFMIS diodes[3], [4]. The short retention time in the MFIS and MFMIS structures originates from the fact that a dielectric capacitor is equivalently connected in series to the ferroelectric capacitor, as explained in the following.

When the power supply voltage is off and the gate terminal of the FET is grounded, the top and bottom electrodes of the two capacitors are short-circuited. At the same time, electric charges ±Q appear on the electrodes of the both capacitors due to the remnant polarization of the ferroelectric film and due to the charge neutrality condition at a node between the two capacitors (the FI interface in the MFIS structure or the floating gate M in the MFMIS structure). The Q - V relation for the buffer layer capacitor is Q = CV, and thus, the relation in the ferroelectric capacitor becomes Q = -CV under the short-circuited condition, where C is capacitance of the buffer layer. That is, the direction of the electric field in the ferroelectric film is opposite to that of the polarization. This field is known as a depolarization field and it reduces the data retention time significantly, particular when C is small.

Another point to be considered is the leakage current of both the ferroelectric film and the buffer layer. If the charge neutrality at a node between the two capacitors is destroyed by the leakage current, electric charges on the electrodes of the buffer layer capacitor disappear, which means that carriers on the semiconductor surface disappear and the stored data can not be readout by drain current of the FET, even if the polarization of the ferroelectric film is retained.

B. *Optimization of materials and device structures*

B.1 Necessary Conditions for Buffer Layer and Ferroe-lectric Materials

In order to minimize the depolarization field in the ferroelectric film, the buffer layer capacitance C must be as large as possible. This condition means that a thin buffer layer with a high dielectric constant is preferable. Another important point is to reduce the leakage current of both a ferroelectric film and a buffer layer, as discussed above. That is, the thinnest limit of the buffer layer thickness is determined by the leakage current.

Concerning the ferroelectric material, it is preferable to have a square-shaped P-V (polarization vs. voltage) hysteresis loop, as well as its leakage current is small. It is expected in a ferroelectric film with a square-shaped hysteresis loop that the polarization is not reversed even if a small depolarization field is generated. Concerning the polarization state of the ferroelectric film, use of the fully polarized state seems to be more important to obtain a long retention time than that of the partially polarized state where the P-V hysteresis curve draws a minor loop.

B.2 Optimization of Device Structures

Improvement of the data retention characteristics is further discussed from a device structure viewpoint. It is well known that dielectric constants of ferroelectric films are generally much higher than those of dielectric buffer layers. Thus, if both the ferroelectric and buffer layer capacitors are formed in the same size, most external voltage is applied to the buffer layer and only a little is to the ferroelectric film. In order to solve this mismatch problem on the dielectric constant, it is necessary to make the ferroelectric capacitor area smaller and also to make the film thicker. However, if a too thick ferroelectric film is used, the operation voltage of the FET becomes high. Thus, there is a limitation in the film thickness to be used.

The other problem is the mismatch of induced charge. The remnant polarization values of PZT and SBT are about 40μC/cm^2 and 10μC/cm^2, respectively, and they can induce the same density of positive and negative charges to the electrodes of a capacitor. These values are generally much larger than the maximum charge density induced by a dielectric film. For example, the maximum induced charge density of SiO_2 is about 3.5μC/cm^2 for

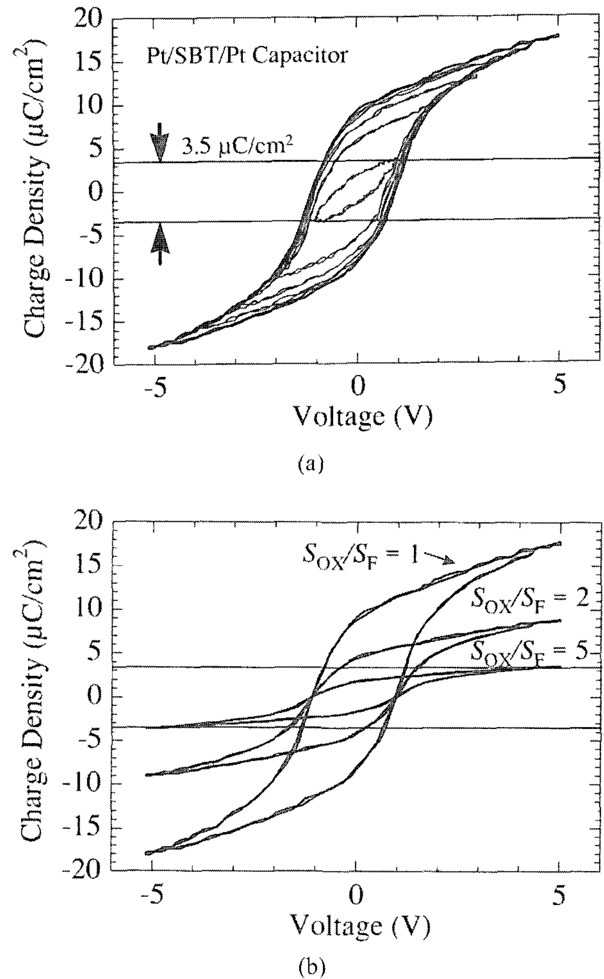

Fig. 2. (a) Induced charge density mismatch between SBT and SiO_2, and (b) variation of the hysteresis loop by optimization of capacitor area.

an electric field of 10 MV/cm and the film breaks down for the higher electric field. Thus, if a ferroelectric capacitor with a large remnant polarization is connected in series to a SiO_2 capacitor with the same area, and if a sufficiently high voltage is applied across the both capacitors, the SiO_2 film breaks down before the saturation polarization of the ferroelectric film is reached. This situation is illustrated in Fig. 2(a) for a combination of SBT and SiO_2. As shown in the figure, only a small hysteresis loop of SBT can be used under the condition that the SiO_2 buffer layer does not break down. It should be noted that this condition is independent of the film thickness of both capacitors.

In order to solve the mismatch problem on induced charge, it is necessary to form an MFMIS structure and to optimize the area ratio between the ferroelectric

capacitor and the buffer layer capacitor. That is, in order to use the saturation polarization of the ferroelectric film effectively, it is important to make the ferroelectric capacitor area small. If the area of an SBT capacitor is reduced to 1/5 of that of an SiO_2 capacitor, the vertical scale of the P – V characteristic equivalently becomes 1/5 as shown in Fig. 2(b), and the saturation polarization curve can be drawn in the region where the polarization value does not exceed the maximum induced charge density of SiO_2 (± 3.5μC/cm^2)[5]. These results suggest that combination of planar capacitors (MFM parts) and three-dimensional FETs (MIS parts) is important to integrate MFMIS-FETs with the optimized area ratio in high density. It is interesting to note that this design concept is opposite to that of DRAM.

III. Recent Results on Fabrication of Fettype Ferams

A. *MFMOS-FET with a SiO_2 buffer layer*

A.1 Relation between the Buffer Layer Thickness and the Area Ratio

A typical value of the area ratio (S_{OX}/S_F) between the SiO_2 and SBT capacitors is 5, as shown in Fig. 2(b). However, since this value was derived assuming that any power supply voltage is used, it may be changed when the supply voltage is fixed at a constant value. In the following, the polarization characteristics of a ferroelectric film in an MFMOS (O; oxide) structure are analyzed under a fixed bias condition and their validity is experimentally checked through investigation of the characteristics of MFMOS-FETs with various area ratios[6]. In this analysis, the experimental data for various minor loops of an SBT capacitor are used.

The polarization hysteresis loops were measured for a 300-nm-thick SBT film, which was deposited by the conventional sol-gel spin-coating technique and annealed for crystallization at 750℃ for 30 min in O_2 atmosphere. When a power supply voltage V_{SUP} is applied to the MFMOS structure, a relation that $V_{SUP} = V_F + V_{OX}$ holds, where V_F is the voltage across the ferroelectric capacitor and V_{OX} is the voltage across the SiO_2 film and the depletion layer of the Si surface. Then, the induced charge density Q_{OX} at the electrode of MOS capacitor is expressed as $Q_{OX} = C_{OX}V_{OX} = C_{OX}(V_{SUP} - V_F)$, where C_{OX} is the oxide capacitance per unit area. Since Q_{OX} is also related to the polarization P in a form that $PS_F = Q_{OX}S_{OX}$, the operation analysis of the MFMOS capacitor can be conducted graphically.

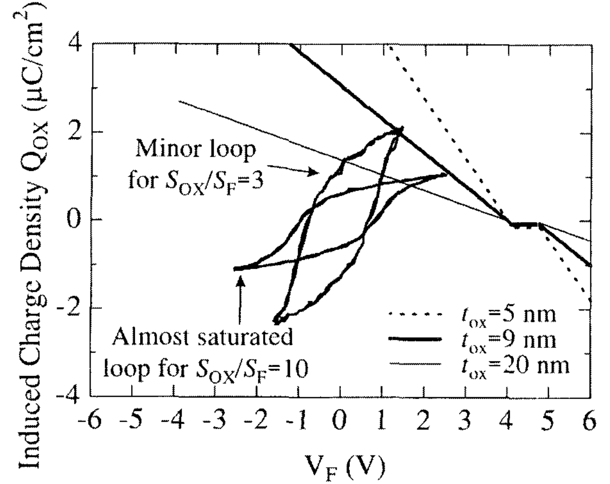

Fig. 3. Relationship between the induced charge density Q_{OX} and the voltage V_F across the ferroelectric capacitor.

Figure 3 shows the Q_{OX} - V_F relationship calculated for different values of SiO_2 thickness (t_{OX}) and the area ratio. In this figure, the V_{SUP} value was fixed at 5 V. The two hysteresis loops in the figure were selected from a set of experimental data so that their edges were in contact with the thick solid line corresponding to the case of t_{OX} = 9 nm. As can be seen in the figure, the polarization hysteresis is almost saturated for S_{OX}/S_F = 10, but not for S_{OX}/S_F = 3. By selecting appropriate hysteresis loops, it is possible to determine the degree of saturation, which is defined by the ratio of the remnant polarization (P'_r) in the selected curve to that (P_r) in the fully saturated polarization curve. The degree of saturation can be derived as functions of t_{OX} and the area ratio, as shown in Fig. 4(a) and it is expressed by a universal curve when the horizontal axis is normalized as shown in Fig. 4(b)[7]. As can be seen from the figure, a rough measure to obtain well-saturated polarization curve under the assumed power supply voltage is $S_{OX} > S_F t_{OX}$ (nm), that is, the area ratios larger than 5 and 10 are necessary for t_{OX} = 5 nm and t_{OX} = 10 nm, respectively.

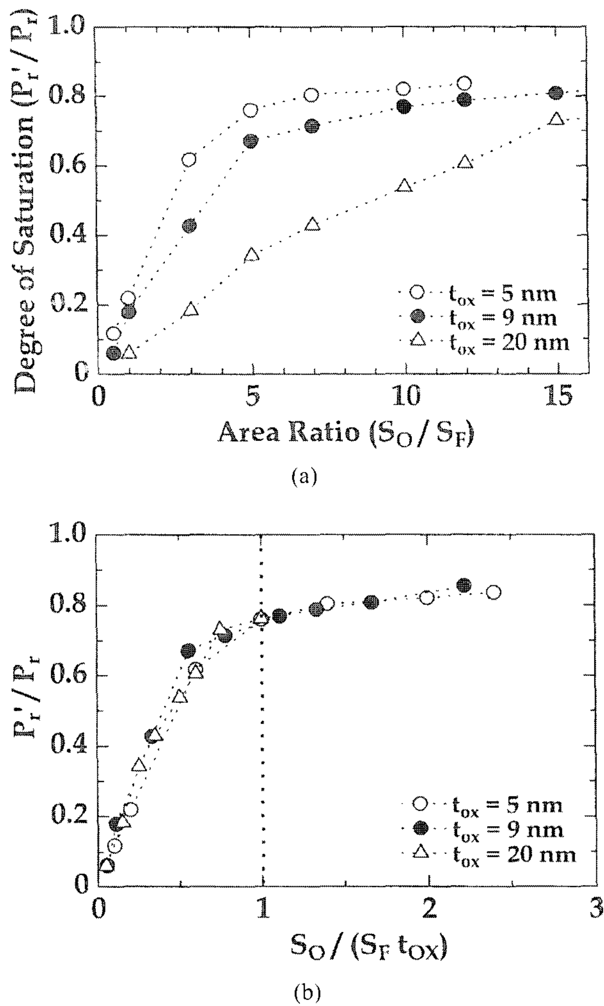

Fig. 4. Relationship between the area ratio (S_{OX}/S_F) and the degree of polarization saturation (P'_r/P_r), and (b) relationship between $S_{OX}/(S_F t_{OX})$ (1/nm) and P'_r/P_r.

A.2 Fabrication of MFMOS-FETs

Based on the above consideration, MFMOS-FETs were fabricated on an SOI structure. First, the device region was separated into islands with rectangular shapes using plasma etching. Then, Si islands were oxidized for passivation and the source and drain regions were formed by ion implantation. After the gate windows of MFMOS-FETs were formed by wet chemical etching, a 9-nm-thick gate SiO_2 layer was grown by thermal oxidation at 950℃ for 15 min in dry-O_2 ambience and annealed at the same temperature for 20 min in N_2 ambience to improve the film quality. For the floating gate electrode, Pt(80nm)/Ti(4nm) was deposited by an e-gun evaporation method and patterned by a lift-off process.

Then, a ferroelectric SBT film was deposited by the liquid source misted chemical deposition (LSMCD) method, and annealed at 750℃ for 30 min in O_2 ambience for crystallization. The final thickness of the SBT film was about 150 nm. As the top gate electrode, Pt (60nm) was deposited by e-beam evaporation and patterned by reactive ion etching using Ar gas. Finally, contact holes were formed by wet chemical etching and Al interconnection and electrode pads were formed by the lift-off process.

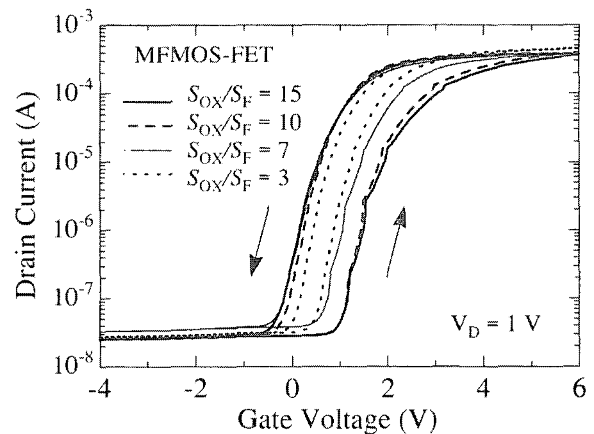

Fig. 5. I_D-V_G characteristics of the fabricated MFMOS-FETs with S_{OX}/S_F values of 3, 7, 10 and 15.

The memory operations of the fabricated MFMOS-FETs were examined by measuring the I_D - V_G characteristics, as shown in Fig. 5. Counterclockwise hysteresis loops were obtained, as shown by arrows, which indicates that the threshold voltage is shifted due to the ferroelectric nature of SBT film. As can be seen from the figure, the memory window increases from 0.35 V to 1.40 V as the S_{OX}/S_F ratio is changed from 3 to 15, and it is almost saturated at the S_{OX}/S_F ratio larger than 10. These results agree well with the calculations of Fig. 4(b).

Next, in order to measure the retention characteristics, a programming input pulse of +6V or -4V was first applied for 100 ms to write "on" and "off" states, and then the drain current was continuously measured by maintaining V_G at 0.8V and V_D at 0.1V. Figure 6 shows the data retention characteristics of the fabricated FETs. In the case that S_{OX}/S_F = 3, the initial on/off ratio of drain current is as small as 7.0, because of the narrow memory window width, as shown in Fig.5. On the other

hand, in the case that S_{OX}/S_F = 15, the drain current on/off ratio is larger than 1800 initially, and remains at a value larger than 200 even after about 10 hours have elapsed, although it gradually decreases with time. It is concluded from these results that the data retention characteristic of MFMOS-FETs is much improved compared with that of conventional FETs in which a ferroelectric film is directly deposited on Si. It is also concluded from comparison of Fig. 4(b) with Fig. 6 that the saturated polarization characteristic is very important for the improvement of the data retention characteristics.

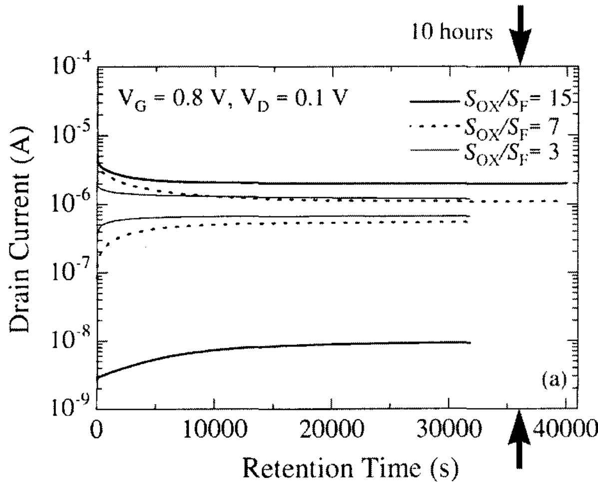

Fig. 6. Data retention characteristics of the fabricated MFMOS-FETs.

B. *MFMIS-FET with a high-dielectric-constant buffer layer*

B.1 Selection of a high-dielectric-constant buffer layer

As discussed in the previous section, in order to obtain the excellent retention characteristics in an MFMIS-FET with a small area ratio (S_{OX}/S_F), it is necessary to use a thin buffer layer. However, for a SiO_2 layer thinner than 3 nm, the leakage current due to direct tunneling of electrons can not be neglected. Thus, in this section, use of a high-dielectric-constant material is discussed, by which the buffer layer thickness can be equivalently reduced beyond the tunneling limit of SiO_2. As an example, the results for a double-layer buffer structure composed of SiON and $SrTa_2O_6$ (STA) are described.

First, Si (100) wafers were thermally nitridized using an RTA (rapid thermal annealing) furnace at 1050℃ for 5 sec in NH_3 atmosphere. The SiO_2-equivalent thickness of the surface dielectric layer was about 2 nm and this value did not change by increase of the nitridation time up to 60 sec, nor by the subsequent annealing process at 850℃ for 1 hour in O_2 atmosphere. Then, a dielectric $SrTa_2O_6$ film was deposited using sol-gel spin-coating technique and it was crystallized by annealing at 900℃ for 3 min in O_2 atmosphere. Total film thickness of the buffer layer ranged from 30 to 60 nm.

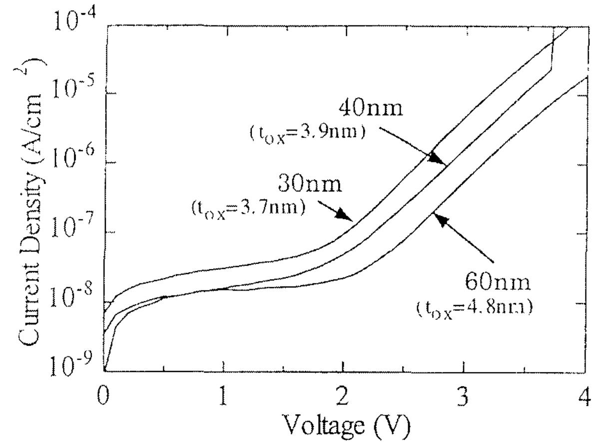

Fig. 7. Leakage current densities of the $SrTa_2O_6$/SiON structure.

The dielectric constant of $SrTa_2O_6$ was calculated to be about 110 by measuring the difference of accumulation capacitance among the samples with different film thicknesses. The SiO_2-equivalent film thickness of a 30-nm-thick $SrTa_2O_6$ film was about 3.7 nm, including the SiON layer. Then, I - V (current vs. voltage) characteristics of Al/$SrTa_2O_6$/SiON/Si diodes were measured. Typical results are shown in Fig. 7, which indicates that the leakage current density of a 30-nm-thick film is less than 5×10^{-8} A/cm^2 up to 2.0 V [8]. This value is about 2 orders-of-magnitude smaller than the theoretically predicted tunneling current of an SiO_2 film with the same thickness. It was also found from C - V and I - V characteristics that the induced charge at 2.0 V was about 2.2μC/cm^2.

B.2 Fabrication of MFMIS-FETs

Using the buffer layer described above, p-channel FETs with MFIS and MFMIS structures were fabricated [8], in which SBT was used as a ferroelectric film and the area ratio between the MFM and MIS parts was optimized in the MFMIS structure. The gate SBT film

was formed using sol-gel spin-coating technique with crystallization annealing at 800℃ for 1 hour in O_2 atmosphere. Figure 8(a) and (b) show I_D - V_G characteristics of FETs with (a) the MFIS structure (the area ratio is 1), and (b) the MFMIS structure (the area ratio is 5.9). As can be seen from the figures, the obtained memory window is much wider in the MFMIS structure, even if the gate material and film thickness are the same for the both structures.

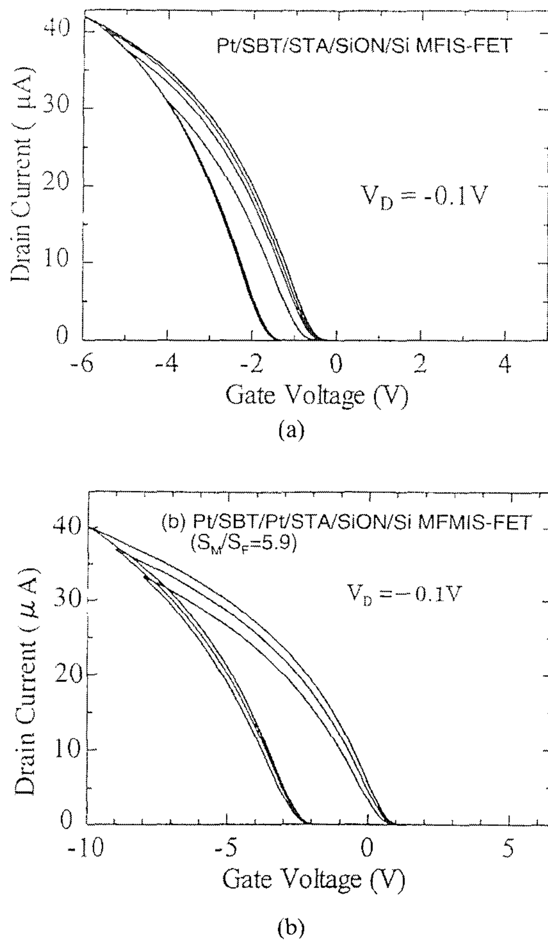

Fig. 8. I_D-V_G characteristics of FETs with (a) $Pt/SBT/SrTa_2O_6/SiON/Si$ structure, and (b) $Pt/SBT/Pt/SrTa_2O_6/SiON/Si$ structure.

Typical retention characteristics for these devices are shown in Fig. 9, in which the variation of drain currents of "on" and "off" states is plotted. In this figure, the dotted lines show the result for an FET with the Pt/SBT/Si gate structure. Since there exists a transition layer with poor electrical properties between SBT and Si, the retention time is the order of 1 hour. When the gate structure is changed to $Pt/SBT/SrTa_2O_6/SiON/Si$, the retention characteristic is improved, as shown in dashed lines. The solid lines show the characteristic for an FET with the gate structure of $Pt/SBT/Pt/SrTa_2O_6/SiON/Si$, and in this case the area ratio between the MIS and MFM parts is optimized to be 5.9. This figure clearly shows that the retention characteristic is much improved by optimizing the area ratio. The current on/off ratio at a retention time of 10 hours is larger than 10^3 in this case.

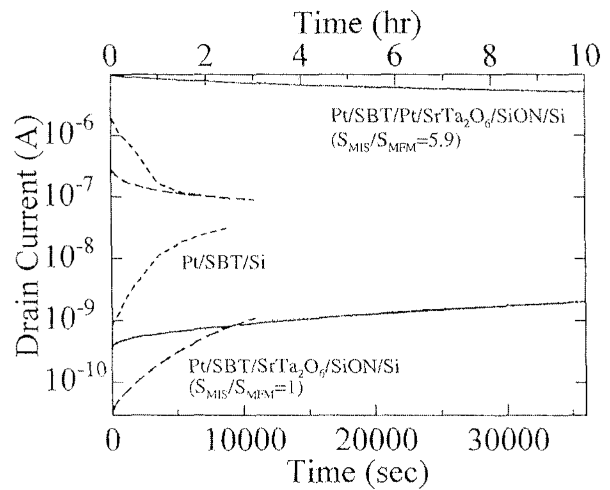

Fig. 9. Time dependence of drain currents of various ferroelectric-gate FETs.

In this section, an example of a high-dielectric-constant buffer layer was shown. The selection standard of such a buffer layer is similar to that of the high-dielectric-constant gate insulator, which is now actively being investigated for fabrication of ultra-small MOSFETs with the gate length shorter than 0.1μm. Therefore, it is expected that a common high-dielectric-constant material is used for the both applications. However, it should be noted that the upper limit of the leakage current density is completely different between the two applications. That is, the acceptable level of the leakage current density is $1x10^{-9}$ A/cm^2 or less in case of the buffer layer of the MFIS or MFMIS structure, whereas it is often on the order of 1 A/cm^2 in case of the gate insulator of ultra-small MOSFETs.

C. *Development of New Ferroelectric Materials*

It is concluded from the discussions in the previous chapter that a key factor to obtain the excellent retention

characteristics of ferroelectric-gate FETs is to use the saturated polarization of the ferroelectric film. Therefore, when such materials as PZT and SBT are used in the FETs, it is necessary to form an MFMIS structure and to adjust the area ratio between the MFM and MIS parts, so that their large remnant polarization values can be used effectively. However, it is disadvantageous from a viewpoint of high-density integration to design the MIS part in a large area. Thus, it is desirable to develop a new ferroelectric material by which the area ratio close to unity can be realized. This material is necessary to have a small remnant polarization value and its hysteresis loop is preferable to be square-shaped. In this experiment, c-axis oriented $(Ba,La)_4Ti_3O_{12}$ (BLT) is adopted as a promising candidate to satisfy the above conditions, and the crystallographical and electrical properties of the BLT films are investigated.

C.1 Si_3N_4 Buffer Layer

Si_3N_4 is a good oxygen diffusion barrier and it has a higher dielectric constant than SiO_2. Thus, it is a good candidate of a buffer layer in the MFIS structure. Actually, a thermal oxinitride layer was used in the structure discussed in the previous section, but it was too thin to be used alone for preventing the leakage current. Another important method to form a Si_3N_4 layer is plasma-enhanced nitridation of Si surface and excellent interface properties have been reported when NH_3 gas or a mixing gas of N_2 and H_2 is used [9]. In this film, however, high-density hydrogen atoms are incorporated and they terminate the dangling bonds located in the film and at the interface. Since hydrogen atoms are released from the film during high temperature annealing, this film can not be used as a buffer layer for depositing a ferroelectric film.

In order to solve these problems, we used N and/or N_2 radicals, which were generated by a RF plasma cell manufactured by SVT Associates Inc [10]. In the experiment, (100)-oriented Si wafers were dipped in HF solution to remove native oxide and to form H termination on the surface. They were loaded into a UHV chamber in a few minutes and heat-treated in the chamber for surface cleaning. Then, the wafers were kept at various temperatures and the surface was exposed to N and/or N_2 radicals for 1 hour. The temperature dependence of the Si_3N_4 layer thickness is shown in Fig. 10. The thickness was evaluated by wavelength dispersive ellipsometry calibrated by XPS (X-ray photoelectron spectroscopy) method. The open circles in the figure represent the nitridation results by N_2 radicals. It is evident that the film thickness saturates at 1.7 nm, virtually independent of the substrate temperature. The time dependence also showed that the saturation of the growth occurred at 1.7 nm for all temperatures in case of the nitridation by N_2 radicals. This phenomenon can be explained by a hypothesis that diffusion of N_2 radicals is prevented by the Si_3N_4 layer, which has already been formed.

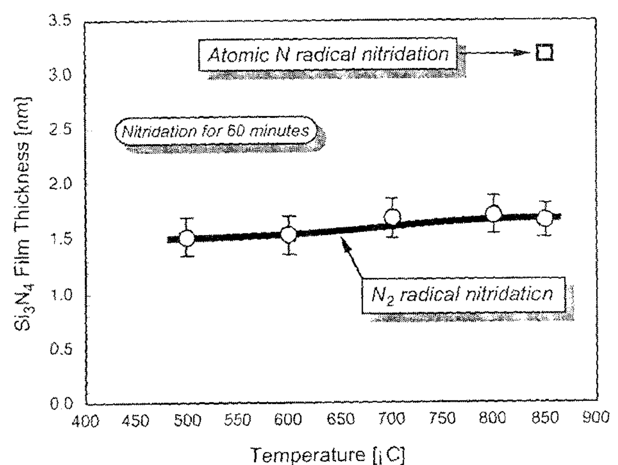

Fig. 10. Substrate temperature dependence of Si_3N_4 layer thickness formed by N and N_2 radical nitridation.

Then, nitridation conditions were so changed by increasing RF power that much more N radicals were generated. The intensity of N radicals was measured by using plasma emission spectroscopy. The result is shown in the figure with an open square. Although we have only a single datum in this figure, it is evident that the film thickness is much increased by use of atomic N radicals. In this case, the obtained thickness was 3.3 nm. The apparent difference of the film thickness is probably due to the fact that the size of a N radical is smaller than that of a N_2 radical, which is the same as that of a N_2 molecule.

Next, the electrical characteristics of the Si_3N_4 layer formed by N radicals were measured by fabricating MIS capacitors. The nitridation was carried out at room temperature using atomic N radicals and annealed at 950℃ for 30 min in pure nitrogen. With this post thermal treatment, the Si_3N_4 layer showed higher electrical performance. The results are shown in Fig. 11. The equivalent thickness to SiO_2 of the Si_3N_4 layer was

3.7 nm. Although the sample was heat-treated at 950℃, no hysteresis was observed, as shown in Fig. 11(a) and the interface state density of this capacitor was estimated to be 3.7×10^{11} $cm^{-2}eV^{-1}$ near the mid-gap of Si. This result means that the carrier traps and fixed charges do not increase in this MIS diode during the post thermal treatment, because hydrogen atoms are not used for eliminating the dangling bonds in the MIS structure. The I - V characteristics of this sample are shown in Fig. 11(b). As can be seen from the figure, the leakage current density at ±2V was less than 2×10^{-6} A/cm^2, which is acceptable for the gate insulator in most advanced MOSFETs.

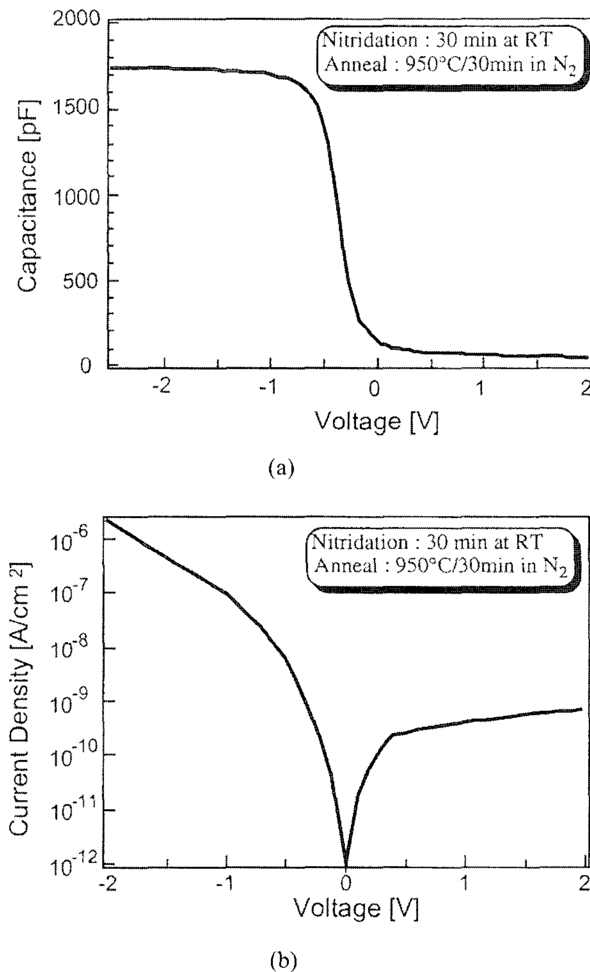

Fig. 11. (a) C-V and (b) I-V characteristics of MIS diodes with a Si_3N_4 layer formed by Nadicals.

C.2 Formation of $(Bi,La)_4Ti_3O_{12}$ Films

$Bi_4Ti_3O_{12}$ has a Bi-layered crystal structure and its spontaneous polarization values are about 50μC/cm^2 along a-axis and about 4μC/cm^2 along c-axis. This material is known as the first ferroelectric film used for fabrication of a ferroelectric-gate FET on a Si substrate [11]. It has also been shown that MFIS diodes with a $Bi_4Ti_3O_{12}/Bi_2SiO_5/Si$ structure have such an excellent retention characteristic that the capacitance values kept at the accumulation and inversion states in the hysteresis loop do not change for 11 days [3]. On the other hand, concerning the fatigue characteristic, both results showing fatigued and fatigue-free properties have been reported and no conclusion has been obtained yet. In the meanwhile, it was reported last year that substitution of 10 to 20 % of Bi atoms with La atoms was effective in solving the fatigue problem of this film [12]. Thus, in the present experiment, $(Bi,La)_4Ti_3O_{12}$ films with a fixed La content of 0.75 were used and the optimum conditions to form c-axis-oriented films on the amorphous Si_3N_4 layer were investigated.

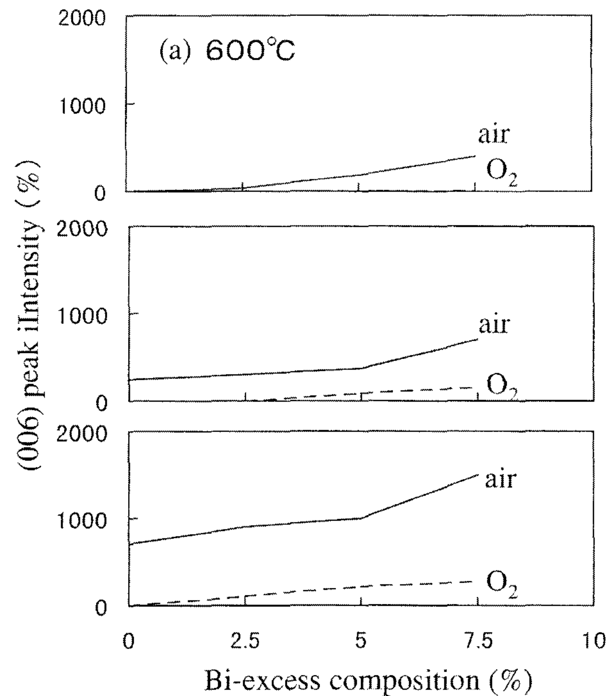

Fig. 12. Relations between Bi-excess composition and XRD (006) peak intensity.

BLT films were formed using sol-gel spin-coating technique, in which 2.5 to 7.5% excess-Bi solutions were used and the film thickness was fixed at 100 nm using a single spin-coating process. First, the crystallization conditions were investigated by changing annealing

temperature and ambience, where the pre-annealing temperature was fixed at 400℃. At a crystallization temperature of 700℃, many reflection peaks corresponding to the c-axis of a BLT film were observed in XRD patterns. However, since (117) peak was also observed in the patterns, the annealing conditions were further optimized.

Typical results are shown in Fig. 12 [13], in which the intensity of (006) peak is plotted as a measure of the preferred orientation of c-axis. It can be seen from the figure that the peak intensity becomes stronger in air ambience, at the higher annealing temperature, and at the larger Bi composition. It can also be seen that the crystallization characteristics at 800℃ in O_2 ambience are almost the same as those at 600℃ in air. It is concluded from these results that BLT films are crystallized in air more easily than in O_2 ambience regardless the annealing temperature. It was also found that BLT films were almost perfectly oriented to c-axis at an annealing temperature of 800℃.

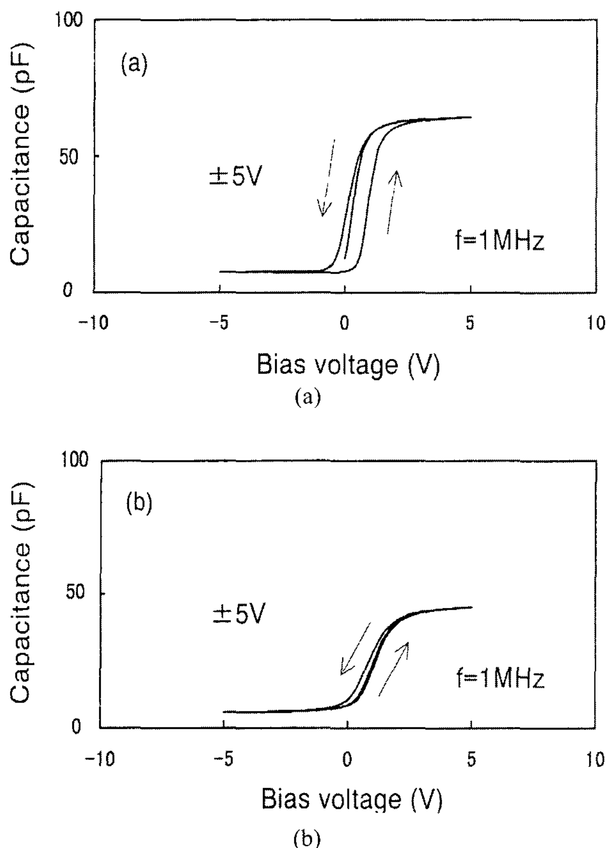

Fig. 13. C-V characteristics of Pt/BLT/Si_3N_4/Si diodes. (a) c-axis-oriented film and (b) randomly oriented film.

In order to ascertain the effectiveness of the c-axis-oriented film, C – V characteristics were measured for both c-axis-oriented and randomly oriented films. The BLT films were formed by spin-coating 10% excess-Bi solution on n-type Si wafers covered with 3-nm-thick Si_3N_4 layers. The crystallization annealing conditions were the same (at 800℃ in air) for the both samples, but the pre-annealing temperature was changed to obtain the randomly oriented film. The C – V characteristics for the Pt/BLT(100nm)/Si_3N_4(3nm)/Si structures are shown in Fig. 13. As can be seen from the figure, the memory window width in the c-axis-oriented film is about 1.2 V for a voltage scan of ±5 V. On the other hand, the hysteresis width of the film, which contains (117) crystallites, is very narrow for the same voltage sweep amplitude. This difference can be explained by the difference of the remnant polarization values in the film. It was also found from a preliminary experiment of 3 hours that the data retention characteristic of the c-axis-oriented film was much better than that of the randomly oriented film.

D. *Proposal and Fabrication of Novel 1T2C-type Ferroelectric Memory*

D.1 Structure and "write" operation

As discussed in chapter 2, in the MFIS and MFMIS structures, the depolarization field is inevitably generated in the ferroelectric film, when the gate electrode is grounded. The field then produces drift current flowing through the both ferroelectric film and buffer layer, as well as it decreases the remnant polarization itself. Since the current destroys the charge neutrality condition of the floating gate, the charges on the semiconductor surface are removed after the passage of time. Thus, in these structures, it is very difficult to retain the data for a long time. In this section, in order to solve this problem, a novel FET-type FeRAM, in which the depolarization field is not generated in the ferroelectric film, is proposed [14] and the operation principle is experimentally demonstrated.

An equivalent circuit of the memory cell is shown in Fig. 14, in which two ferroelectric capacitors are connected to the gate of a usual MOSFET. It is assumed that the material and area of the capacitors are the same and only their thickness is different. In order to write "0"

or "1" datum in this memory, positive or negative voltage is applied between the terminals A and B. Here, the data "0" and "1" are defined as shown in Figs. 14(a) and (b), respectively. In this structure, the MOS gate capacitor C_{OX} is necessary to be relatively small, because for a very large C_{OX} the floating gate potential is virtually grounded and the "write" voltage is not sufficiently applied to the ferroelectric capacitor. However, if the substrate potential of MOSFET is appropriately biased during the "write" operation, the restriction for C_{OX} is not necessary to be taken into account.

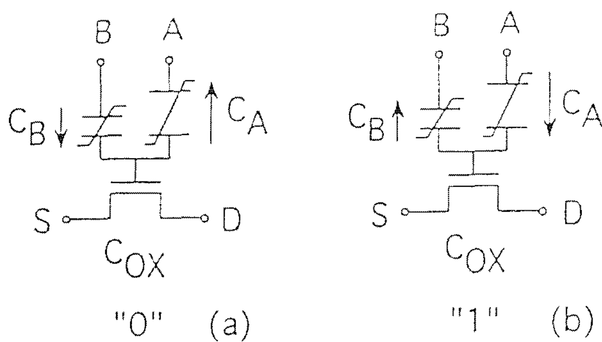

Fig. 14. An equivalent circuit of the 1T2C-type memory and the polarization directions of data "0" and "1".

When the polarization values of the both capacitors are the same, an equal amount of positive and negative charges appears on the electrodes of the capacitors C_A and C_B, and thus no charge appears on the electrode of capacitor C_{OX}. Under this condition, the floating gate potential which is given by $V_{OX} = Q_{OX}/C_{OX}$ is zero and no depolarization field is generated for both C_A and C_B, when the terminals A and B are grounded. It is evident that the retention time of this memory is as long as that of the usual 1T1C type memories, in which ferroelectric capacitors are short-circuited when the power supply voltage is off.

D.2 Non-destructive "read" operation

In order to readout the storage data, a positive pulse voltage V is applied to the terminal B, the terminal for the thinner ferroelectric film, keeping the Si substrate grounded and the terminal A open. When the written datum is "0", no polarization reversal occurs by the "read" pulse and few electrons are induced on the Si surface, as shown in Fig. 15(a). On the contrary, when the written datum is "1", polarization of the capacitor C_B is reversed and many electrons are induced on the Si surface, as shown in Fig. 15(b), which means that the drain current flows in the n-channel MOSFET. After the "read" pulse is removed, that is, both terminals A and B are grounded, the polarization direction of the capacitor B with a lower coercive voltage is automatically reversed so that the total energy of the system becomes minimum. This model is essentially correct, if the capacitance C_{OX} is infinitely small. For a finite C_{OX}, however, a more precise discussion is necessary, as shown in the following.

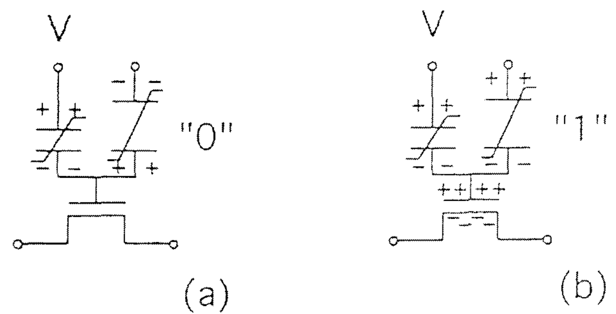

Fig. 15. Schematic of"read" operation.

First, for simplicity of discussion, an ideal Q-V hysteresis curve is assumed for the capacitor C_B, as shown in Fig. 16, where Q_B and V_B are the induced charge on the electrode and the voltage across C_B, respectively. When the terminal A is open, the charges on the electrodes of C_A can not move, and therefore the charge distribution between C_B and C_{OX} can be calculated, assuming that the floating gate between them has the initial charge of $\pm Q_{BR}$, where Q_{BR} is the remnant polarization of the capacitor B. Under this condition, the load line representing the capacitor C_B does not pass the origin of the Q-V plane, but passes either a point (0, Q_{BR}) for the data "0", or (0,- Q_{BR}) for the data "1", as shown in Fig. 16.

It is evident from Fig.16 that the "read" pulse does not destroy the "0" datum, while it changes the "1" state from the original position L. If the applied voltage V is sufficiently large, the operation point moves along the outermost hysteresis loop and comes back to a new position M. The direction of electric field in the film is the same as that of polarization, as long as it is located in the third quadrant, and thus no depolarization field is generated. However, this voltage produces the

depolarization field in C_A, and the remnant polarization of C_A decreases until the remnant polarization values of both capacitors are equal and the depolarization field in C_A disappears (the position N in Fig.16).

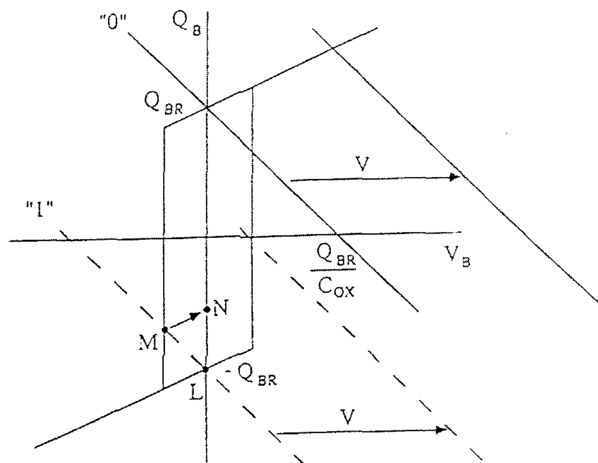

Fig. 16. Explanation of the operation principle using an ideal Q_B-V_B hysteresis curve.

Since decrease of the remnant polarization in C_A is on the order of several hours to several days, the position M does not change significantly, even if the "read" operation is frequently repeated in a short time, and the data are expected to be retained, if the "refresh" (rewrite) operation is conducted once an hour or once a day. The explanation in Fig. 16 is not directly related to the capacitor C_A, which means that the coercive voltage of the capacitor A is not necessarily larger than that of the capacitor B, or the ferroelectric film in C_A is not necessarily thicker than that in C_B, although a thicker film is preferable from a viewpoint of the data retention.

D.3 Layout for high-density integration

In order to realize a high-density memory, a cell structure shown in Fig. 17 is proposed, which is a simple extension of the single-transistor-cell-type memory [2]. In this structure, Si stripes, each of which acts as MOSFETs connected in parallel, are placed on an insulating substrate, floating gate electrodes are placed along the stripes on the gate SiO_2 layer, and double conductive stripes embedded in a ferroelectric film are placed along and perpendicular to the Si stripes. The size of the floating gate and the width of the double conductive stripes are so determined that overlap areas between the floating gate and the first conductive stripe, and the floating gate and the second stripe are equal, as shown in the inset of the figure. Thus, the capacitors C_A and C_B can be formed on the floating gate without any precise mask alignment.

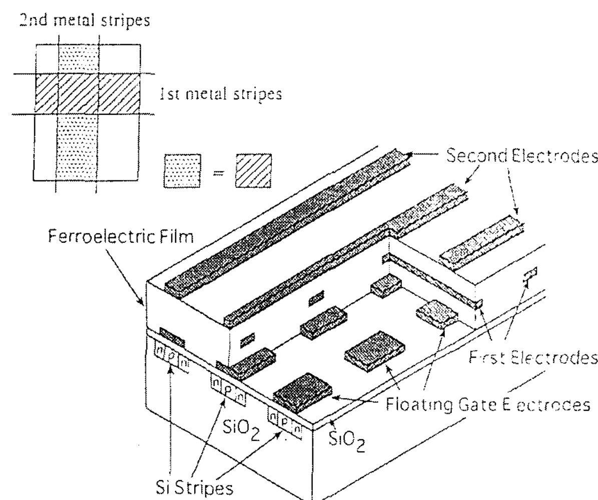

Fig. 17. Integration of the 1T2C-type memory on an SOI structure.

D.4 Experimental results

The operation of the 1T2C-type memory cell discussed above was demonstrated using an SOI substrate [15]. In fabrication of the cell, SBT was used as a ferroelectric film and Pt was used as the top and floating gate electrodes. Channel length and width of the FET are 5μm and 50μm, respectively. The area ratio between the MOS capacitor and one of the ferroelectric capacitors was chosen as 10 and the same film thickness was used for the both capacitors. The P-V characteristics measured between the two top electrodes showed a relatively large remnant polarization of 8.9μC/cm^2 ($2P_r$) and the polarization was well saturated at a high voltage. The I_D-V_G plot measured using one of the ferroelectric capacitors also showed good hysteresis characteristic and the characteristics of C_A and C_B were almost the same.

Next, in order to write a datum "1", voltage pulse signals of +4 V, 100 ms and –4 V, 100 ms were applied to C_A and C_B, respectively. For a datum "0", the polarity of the "write" pulses was inverted. For the "read" operation, voltage pulses V_R ranging from 0.5 to 4 V were applied to the terminal B. Figure 18 shows variation of the drain current of the FET by application of a "read" pulse of 2.5 V. It can be seen form the figure

that the drain current increases only in the period when the "read" pulse is applied to the gate, and it almost comes back to the initial value when the pulse is removed. It can also be seen that the drain current during the "read" operation is very different between the data "1" and "0". In this case, the ratio of the drain current was about 430.

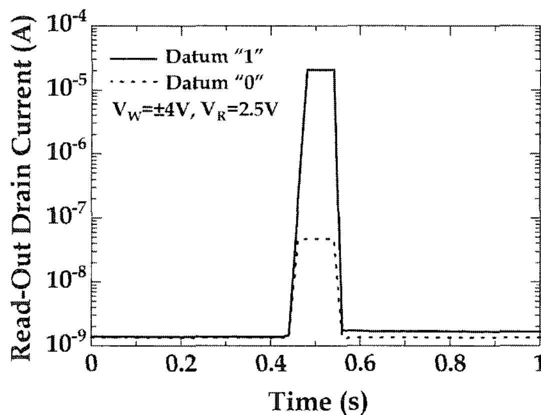

Fig. 18. "Read"operations of 1T2C-type ferroelectric memory cell.

Finally, the possibility of the non-destructive "read" operation and the data retention characteristics of the fabricated cells were investigated. Concerning the "read" characteristic, it was found that variation of the drain currents for both "1" and "0" data was negligible even after the "read" operation shown in Fig.18 was repeated for 1000 times. It was also found in the retention characteristic that the drain current did not change even if the stored data were readout after they had been retained for 10^5 sec. This period was much longer than the retention time of the usual MFMOS-FET (about 10^4 sec), which was realized using the same cell by polarizing the two ferroelectric capacitors in the same direction. It is concluded from these results that the 1T2C-type cell is one of the most promising ferroelectric memories having both features of non-destructive data readout and excellent data retention characteristics.

IV. Summary and Future Prospects

The current status of FET-type ferroelectric memories was reviewed. It was described that the largest problem in the FET-type FeRAM was the short retention time in data storage, and some solutions to this problem were discussed from viewpoints of materials, device structure, and circuit configuration. Finally, our recent results, which were considered to be useful in realizing FET-type FeRAMs, were introduced.

Social interests and expectation to FeRAMs have increased in the recent years. They are not only to the present 1T1C-type memories, but also to the FET-type memories. Based on this background, we started the "Research and Development of Next Generation Ferroelectric Memories" project sponsored by Ministry of International Trade and Industry, Japan in 1999. The goal of this project is to solve various problems of FET-type FeRAMs and to realize ferroelectric memories with a feature of non-destructive readout. The scheduled period of the project is 5 years and the total budget is about 2 billion yens (about 18 million dollars).

As I showed above, we have been solving some materials problems and have demonstrated the basic operation of the 1T2C-type memory cell. Therefore, development of the integration technology of these devices seems to be most important in the next step. In fabrication of a memory cell array, it is preferable from a viewpoint of high-density integration that each cell does not have an additional MOSFET for cell selection. In order to realize this type of cell, however, it is necessary to solve the data "disturb" problem in the "write/read" operation. In the case of FET-type FeRAM, the "disturb" problem in the "write" operation is particularly significant, because the writing method is essentially the simple matrix method, in which positive and negative voltages are applied to the row and column electrodes, respectively. Thus, step-by-step optimization of various parameters for decreasing the "write/ read" voltage seems to be most important to solve this problem.

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REFERENCES

[1] S.S. Eaton, D.B. Butler, M. Parris, D. Wilson, H. McNeille; IEEE Intern. Solid State Circuits Conf. Digest of Technical Papers, p.130, 1988.

[2] H. Ishiwara, T. Shimamura and E. Tokumitsu; Jpn. J. Appl. Phys. 36, p. 1655, 1997.

[3] T. Kijima and H.Matsunaga; Jpn. J. Appl. Phys., 38, p. 2281, 1999.

[4] Y. Fujimori., T.Nakamura, and A.Kamisawa.; Jpn. J. Appl. Phys., 38, p. 2285, 1999.

[5] H. Ishiwara; Mater. Res. Soc. Sympo. Proc. 596, p. 427, 2000.

[6] S-M. Yoon, E.Tokumitsu. and H.Ishiwara; Jpn. J. Appl. Phys., 39, p. 2119, 2000.

[7] H. Ishiwara; Proc. Intern. Sympo. Applications of Ferroelectrics, Hawaii, Aug. 2000 (in press)

[8] E. Tokumitsu, G.Fujii, and H.Ishiwara : Jpn. J. Appl. Phys., 39, p. 2125, 2000.

[9] Y. Saito, K. Sekine, M. Hirayama, and T. Ohmi; Jpn. J. Appl. Phys., 38, p. 2329, 1999.

[10] Y. Fujisaki, T. Kijima, and H. Ishiwara; Jpn. J. Appl. Phys. 39, Pt.2, L1075, 2000.

[11] S.Y. Wu; IEEE Trans. on Electron Devices, ED-21, p. 499, 1974.

[12] B.H. Park, B.S. Kang, S.D. Bu, T.W. Noh, J. Lee, and W. Jo; Nature, 401, p. 682, 1999.

[13] T. Kijima and H. Ishiwara; Ext. Abstracts of Intern. Conf. on. Solid State Devices and Materials, Sendai, No.LC-1-3, p. 302, 2000.

[14] H. Ishiwara.; Ext. Abstracts of Intern. Conf. on. Solid State Devices and Materials, Hiroshima, No. D-3-5, p. 222. 1988.

[15] S-M. Yoon and H. Ishiwara; 2000 Intern. Electron Device Meeting, San Francisco, No.13.6.

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