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지연고장 점검을 위한 효율적인 IEEE 1149.1 바운다리스캔 설계

(An Efficient IEEE 1149.1 Boundary Scan Design for At-Speed Delay Testing)

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요 약

현재의 IEEE 1149.1 바운다리스캔 표준안은 보드나 내장 코어의 연결선상의 지연고장은 점검 할 수 없다. 본 논문에서는 표준안에 위배되지 않게 TAP 제어기를 수정함으로 시스템 클럭 속도에서 지연고장을 점검 할 수 있는 기술을 개발하였다. 실험을 통해서 본 논문에서 제안한 방법이 기존의 방법보다 추가되는 면적이 적음을 보였다.

Abstract

Delay defects on I/O pads, interconnections of a board, or interconnections among embedded cores can not be tested with the current IEEE 1149.1 boundary scan design. This paper introduces a simple design technique which slightly modifies the TAP controller to test delay defects at system speed. Experimental design shows that the technique proposed requires much less area than a commercial approach.

Ⅰ. Introduction

Boundary scan design is a design for testability technique to simplify the application of test patterns for the detection and diagnosis of different faults at levels of packages(e.g. chips, modules, boards, backplanes). In-circuit test based on the bed-of-nails probing technique makes it possible to test each chip and the interconnections among chips. However it requires the automatic test equipment to probe each chip pin and the increasing use of surface mounting techniques make it difficult to perform in-circuit test. Boundary scan is aiming to improve the card level testability by embedding a dedicated boundary scan register or making use of the part of the scan register in each chip. IBM boundary scan design has been developed in support of reduced pin count test latches belong to the scan register[1]. IEEE 1149.1 and interconnect test where the boundary scan boundary scan design which uses an explicit test protocol is becoming a widely adopted industry standard[2].

The conceivable defects on the interconnections among chips can be modeled as stuck-at, bridging, delay, and intermittent faults. A few test pattern

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generation algorithms for static faults have been developed[3][4]. Although couple of papers have been presented for the testing of dynamic faults, extra hardware for each boundary scan cell is required[5][6] and the internal scan chain information, which is not available in general, must be known to test system delay[7][8]. Boundary scan is used to test delay defects on I/O pads at wafer or package levels[9].

In Figure 1, the signal launched by updateclk is captured by captureclk, but the interval between updateclk and captureclk is 2.5 TCKs, thus delay defects on I/O pads can not be tested with the current IEEE TAP controller. Even if the 2.5 TCKs are shortened to 1 TCK, since the TCK is in general

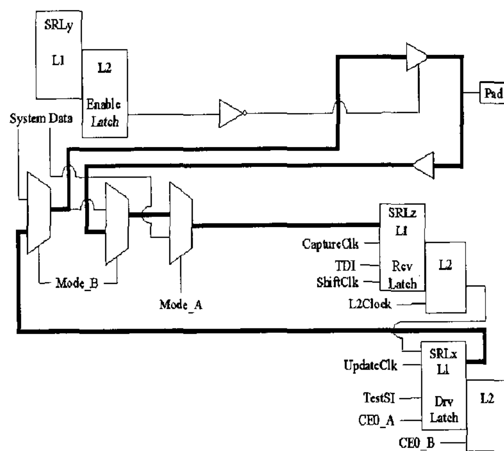

그림 1. 바운다리 스캔을 사용한 I/O 패드에서 지연고장 점검

Fig. 1. Testing delay defects on I/O pads using boundary scan.

much slower than the system clock, additional modification is necessary to multiplex system clock until the signals launched are to be captured. We have developed an efficient boundary scan design technique which can test delay defects at system clock speed in addition to static defects with minimal area overhead while fully complying the IEEE 1149.1 standard.

This paper is organized as follows. In section 2, IEEE 1149.1 standard and interconnect test generation techniques are briefly reviewed and the problem for testing delay defects with boundary scan design is discussed in section 3. A new technique to postpone the Update-DR is depicted in section 4 and simple system clock multiplexing method is introduced in section 5. Experimental results are presented in section 6 followed by conclusions.

Ⅱ. IEEE 1149.1 Boundary Scan and Interconnect Testing

IEEE boundary scan architecture consists of Test Access Ports(TAP), TAP controller, instruction and data registers. Test Data Input(TDI), Test Data Output(TDO), Test Clock(TCK), and Test Reset (TRST) constitute the TAP and TRST can be used optionally. Each input and output pins of a chip is connected to input and output boundary scan cells respectively. IEEE boundary scan instructions can be classified into compulsory ones such as BYPASS, EXTEST, and SAMPLE/PRELOAD and optional ones such as CLAMP, HIGHZ, and RUNBIST. TAP controller is a finite state machine with 16 states which mainly enable to apply patterns to data and instruction registers and to observe the test responses. The interconnect faults on a board can be summarized as follows :

1. S-at-1 and S-at-0 : The conventional stuck at fault model.

2. S-open : The fault model for CMOS implementations which models any open net fault as either a pull-up or pull-down circuit. Initialization and transition patterns, that is, a two pattern test is required to detect a stuck-open fault.

3. Shorted Nets Faults : AND, OR, OPEN, DOMINATOR : The fault model for shorted nets faults can be classified into AND, OR, OPEN and DOMINATOR type faults. Suppose two nets : (A, B) are shorted and let the logic values at each net be V(A) and V(B) respectively then :

(a) An AND type short results in logic 0 if either net is logic 0.

(b) Conversely an OR type short results in logic 1

if either net is logic 1.

(c) We call A DOMINATES B if V(A) appears at both nets regardless of V(B). Similarly B DOMINATES A if V(B) always appears at both nets regardless of V(A).

4. Delay fault: '0-> 1' or '1-> 0' transition can not reach the receiver within a specified amount of time.

This paper introduces a new technique which makes it possible to test delay defects in addition to the static interconnect faults with the EXTEST instruction. The method to apply and observe interconnect test patterns and state transitions of the Test Mode Selector can be summarized as follows :

1. EXTEST instruction is read and decoded. The state transition is :

RESET-> IDLE-> Scan-DR-> Scan-IR-> Capture-IR-> Shift-IR-> …-> EXIT1-IR-> Update-IR->

2. Interconnect test patterns are serially applied through the boundary scan register. The correspon-ding state transitions :

Scan-DR-> Capture-DR-> Shift-DR->…-> EXIT1-DR->

3. Test patterns read are applied to Update latch and the signals are propagated to input Boundary Scan Cells(BSC) in parallel. The corresponding state transitions :

Update-DR-> Scan-DR-> Capture-DR->

4. Test responses captured are shifted out through BSCs to TDO. The corresponding state transitions :

Capture-DR-> Shift-DR->…-> EXIT1-DR ->

Update-DR and Update-IR states are active on the falling edge of the TCK while all the others are on the rising edge. The timing diagram of the above step 3) can be drawn as Figure2. Update-DR is active on the dotted line, and Cature-DR is active on the bold line, thus 2.5 TCKs is required from Update-DR to Capture-DR. That is, it can be seen that it takes 2.5 TCKs from the application of interconnect test patterns through output BSCs to the observation of test responses on input BSCs.

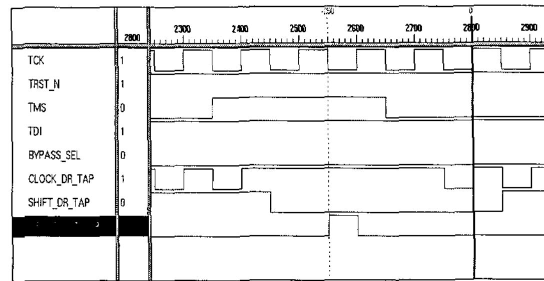

그림 2. 타이밍 도를 통해 본 2.5 TCKs 문제
Fig. 2. Timing diagram revealing 2.5 TCKs problem.

Ⅲ. Problems on the Detection of Delay Defects with IEEE Boundary Scan Design

Although the number of TCK cycles has no relevance on the detection of static interconnect faults, the test responses must be observed in a TCK cycle to detect delay defects. Since the delay defects can not be tested with IEEE boundary scan design, either the state diagram of TAP controller or boundary scan cells must be changed. In order to reduce the cycle time between Update and Capture in the BSC shown in Figure 3, the signal has to be either captured 1.5 TCK earlier as the left dotted circle or updated 1.5 TCK later as the right dotted circle.

Early capture latch is added for the delay defects as Figure 4 in[5]. Early capture latch of dotted circle takes a signal earlier at the activation of the capture

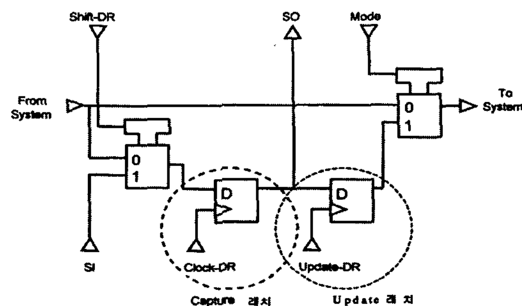

그림 3. Capture 래치 또는 Update 래치 변경에 의한 지연고장 점검
Fig. 3. Detection of delay defects by changing either Capture or Update Latch.

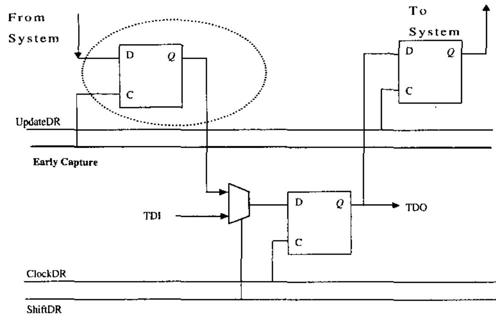

그림 4. Early Caputre 래치를 이용한 지연고장 점검
Fig. 4. Delay detection by Early Capture Latch.

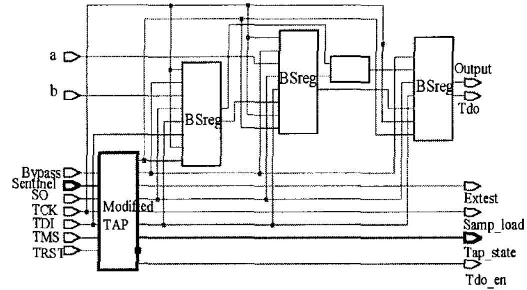

그림 5. 수정된 바운다리 스캔의 상위수준 블록도
Fig. 5. High level block diagram of modified boundary scan design.

signal. However the normal signal has to be passed through the extra latch thus delayed, and the extra latch must be added to each boundary scan cell. We introduce a different boundary scan design technique which simply inserts a block in the TAP controller instead of each boundary scan cell. The delay detection capability is added to EXTEST instruction, thus EXTEST can be used to test not only static but also delay faults.

Which method does result in smaller area overhead between 1.5 TCK late Update and 1.5 TCK early Capture? If the IEEE boundary scan design is precisely looked into, the ClockDR signal depends on both Capture-DR and Shift-DR, thus both signals must be active for the early Capture. On the other hand, since the Mode(selector of the multiplexor) chooses the lower one by EXTEST instruction, the late Update requires changing only Update-DR signal. Therefore we decide to change the Update-DR signal.

Ⅳ. Detection of Delay Defects by Changing UpdateDR

Synopsys CAD tool has been used to change the IEEE boundary scan design. The following factors need to be considered in describing the circuit with boundary scan components supported by Design Ware.

1. Is the Optional Device Identification register used?
2. Is user specified test data register used?
3. How many instructions are to be supported? (to decide the width of instruction register)
4. Does the boundary scan cell operate in synchronous mode or asynchronous mode with respect to TCK?

We have not used optional device identification and user specified test data register. The width of the instruction register is set to two bit. Figure 5 shows the synthesized circuit from high level description. Two inputs and one output sample core is located in the right side and three associated boundary scan latches are around the core. Modified TAP controller is shown in the left side. The detailed circuit diagram of the modified TAP controller is shown in Figure 6.

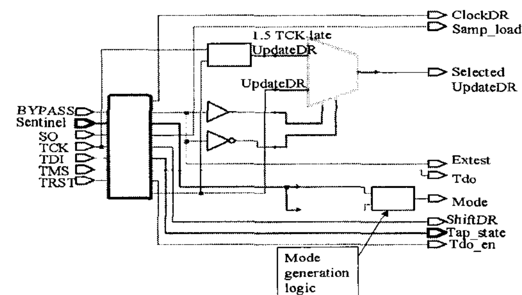

그림 6. 지연고장점검을 위해 변경된 TAP제어기의 상세도
Fig. 6. Detailed description of TAP controller modified for delay testing.

The late UpdateDR signal is driven to the Selected-UpdateDR signal only when EXTEST

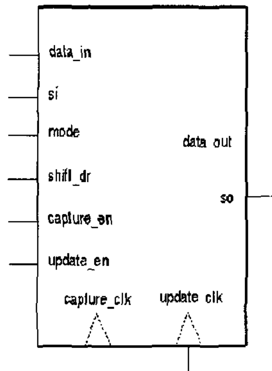

그림 7. Synopys 라이브러리의 Type-1 바운다시 스캔 셀

Fig. 7. Type-1 boundary scan cell in Synopsys library.

instruction is active. Mode generation logic, which generates mode signals for input and output BSCs upon different instructions, is located in lower right side. We have embedded the late UpdateDR block into the Modified TAP controller component so that user can easily change the boundary scan design for delay defects simply by exchanging the TAP block.

Figure 7 shows a type-1 boundary scan cell provided by Synopsys library[11]. For asynchronous boundary scan chains, the update-en is tied to logic one and update-clk is connected to UpdateDR from TAP controller. For synchronous boundary scan chains, update-en is tied to UpdateDR from TAP controller and update-clk are connected to TCK signal.

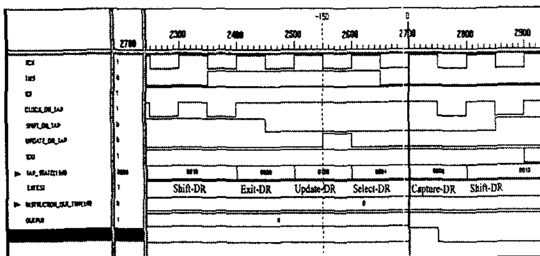

그림 8. UpdateDR부터 CaptureDR까지 1 TCK 소요.

Fig. 8. 1 TCK cycle from UpdateDR to CaptureDR in Asynchronous mode.

The simulation result for 1.5 late UpdateDR is shown in Figure 8. In order to change the UpdateDR only for EXTEST instruction, the decoded signal for EXTEST is designed to activate the late UpdateDR. It can be seen that the rising edge of Update_DR is postponed by 1.5 TCK than Update_DR_TAP, thus the interval between Update_DR and Clock_DR_TAP becomes 1 TCK. In synchronous boundary scan chains, captured data are updated on the rising edge of TCK while the Update-DR is one. For both asynchronous and synchronous boundary scan cells, the TAP is modified so that Update_DR is active 1.5 TCK later than the Update_DR_TAP with the excution of EXTEST instruction.

V. At-speed detection of delay defect

All the JTAG instructions orchestrated with the TCK, which is provided by off-chip tester, are well performed for the static testing. Although the standard design has been augmented to catch the signal in 1 TCK cycle, since the test clock is in general much slower than the system clock, still it is not sufficient to test delay defect at system speed. We propose a simple clock multiplexing technique in this paper.

Observation : Notice that the external TCK must be used on Shift-DR state to draw the test data from the TDI pin. Because the system clock is required only from Update-DR to Capture-DR state, by switching the TCK to system clock only during that interval at-speed delay test can be performed.

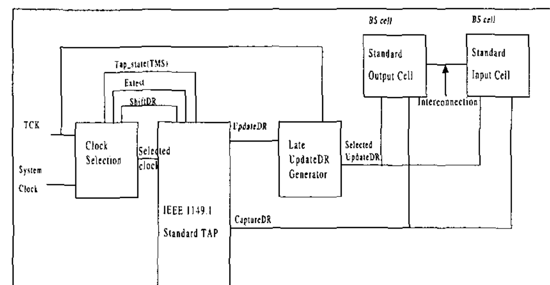

그림 9. 실시간 지연고장점검을 위한 블록도

Fig. 9. Block diagrams of our design for the at-speed delay testing.

As shown in figure 9, the time in which the system clock is required can be pointed out by using three signals(Tap state or TMS, Extest, ShiftDR). Late updateDR and clock multiplexing blocks are additionally required in our method. Figure 10 simulation result shows that late update method using system clock instead of TCK capture the updated signal in 1 system clock. The TAP states operated by system clock include Exit1-DR, Update-DR, Select-DR-Scan, and Capture-DR with Extest Instruction.

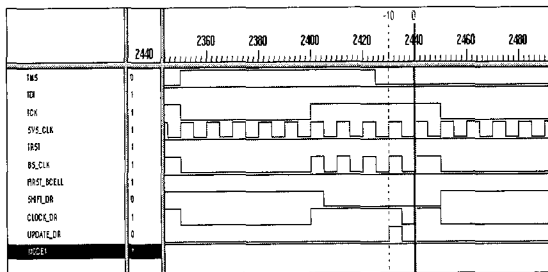

그림 10. 1 시스템 클럭에 동작함을 보이는 시뮬레이션 결과

Fig. 10. Simulation result for the signal captured in 1 system clock.

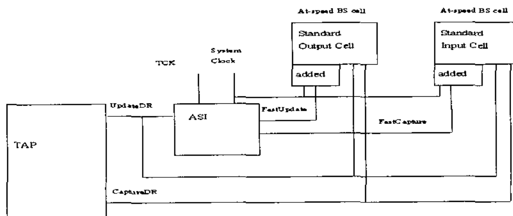

그림 11. Logic vision에서 제시한 방법

Fig. 11. Logic vision method in brief.

표 1. TMS320C6701 DSP 칩에 대한 추가 하드웨어 비교

Table 1. Comparison of hardware overhead for TMS320C6701 DSP chip.

	Our method	Logic Vision
TAP	Late update (8 gate + 3 f/f) Clock select (21 gate +1f/f)	ASI Controller (minimum 21 gate + 1 f/f)
Cell	No	232 * (2Mux + 1 f/f) / Cell
Sum	29 gate + 4 f/f 29 + 8 = 37 gates	232(3 + 2) = 1160 gates

Table 1 compares our approach with Logic Vision.[11]. As can be noted from the figure 11 Logic Vision modifies each boundary scan cell along with the additional control logic. It can be seen that our method requires 39 additional logic gates which are about 30 times smaller than the Logic Visions approach for the TI TMS320C6701 DSP chip.

Ⅵ. Conclusions

IEEE 1149.1 boundary scan TAP controller is simply modified to change the interval between CaptureDR and UpdateDR, thus to be able to test delay defects with EXTEST instruction. Furthermore by multiplexing the system clock from Update-DR to Cature-DR state, at-speed delay testing is feasible with our approach. Conventional 2log(n) interconnect test patterns are augmented to 2log(n+2). The method proposed can be usefully applied to test delay defects on I/O pads and interconnections among boundary scanned IP cores.

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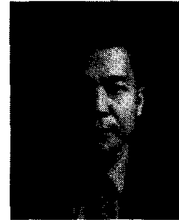

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