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쵸크랄스키 Silicon 단결정의 Large Pit과 Flow Pattern defect의 열적 거동과 Large Pit의 소자 수율에의 영향

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Thermal Behavior of Flow Pattern Defect and Large Pit in Czochralski Silicon Crystals and Effects of Large Pit upon Device Yield

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Abstract The thermal behavior of Flow Pattern Defect (FPD) and Large Pit (LP) in Czochralski Silicon crysatl was investigated by applying high temperature annealing (≥1100℃) and non-agitated Secco etching. For evaluation of the effect of LP upon device performance/yield, commercial DRAM and ASIC devices were fabricated. The results indicated that high temperature annealing generates LPs whereas it decreases FPD density drastically. However, the origins of FPD and LP seemed to be quite different by not showing any correspondence to their density and the location of LP generation and FPD extinction. By not showing any difference between the performance/yield of devices whose design rule is larger than 0.35 ㎛, LP seemed not to have detrimental effects on the performance/yield.

Key words: Czochralski silicon crystal, Flow pattern defect, Large pit, Non-agitated Secco-etching, Device yield, design rule

1. Introduction

Since Yamagishi et al.[1)] reported that Flow Pattern Defects (FPDs) revealed by non-agitation Secco etching in Czochralski (Cz) Silicon (Si) crystals have a detrimental effect on gate oxide integrity, several researchers investigated the nature of FPD and proposed that FPD is associated with interstitial type dislocation loops[2)], vacancy-related defects[3)], or voids.[4)]

It is generally accepted that FPD density of Cz Si wafers can be reduced by heat-treating at relatively high temperature, and by performing crystal growth with slow crystal growth rate.[5)] However, Sadamitsu et al.[6)] proposed that even though slow Cz crystal growth rate (~0.4 ㎜/min) can be effective to reduce FPD density drastically it generates large pits (LPs) that are large dislocation loops with a diameter about 10-30㎛. In addition, Takeno et al.[7)] suggested that octahedral voids which observed inside the OISF (oxidation induced stacking fault)-ring of crystals grown with fast crystal growth rate, 1.4 ㎜/min and interstitial type dislocation loops which generated outside the OISF-ring in very slowly grown crystals with ~0.4 ㎜/min are revealed either as FPDs or Secco etch pits (SEPs) by non-agitation Secco etching for 30 min., and since they loose their chemical properties it is difficult to find flow patterns after high temperature heat treatment in dry O_2 ambient while the defects themselves remain stable.

Even though the slow pulled crystal is accepted, as a material that can get GOI properties compatible to that of epi wafers[8)], its thermal behavior and effects on device performance / yield are not clarified yet. The data of slow pulled wafers that have been reported were extremely rare and hard to interpret the effect of LP itself.[9)]

In this study, to investigate the thermal behavior of LP in Cz Si crystal, we evaluated the changes in morphology and radial density profile of FPD and LP in fast-pulled (0.7 ㎜/min) and slow-pulled (0.4 ㎜/min) crystals through various thermal cycles at the temperatures higher than 1100℃. On the other hand, to understand the effect of LP upon device performance/yield,

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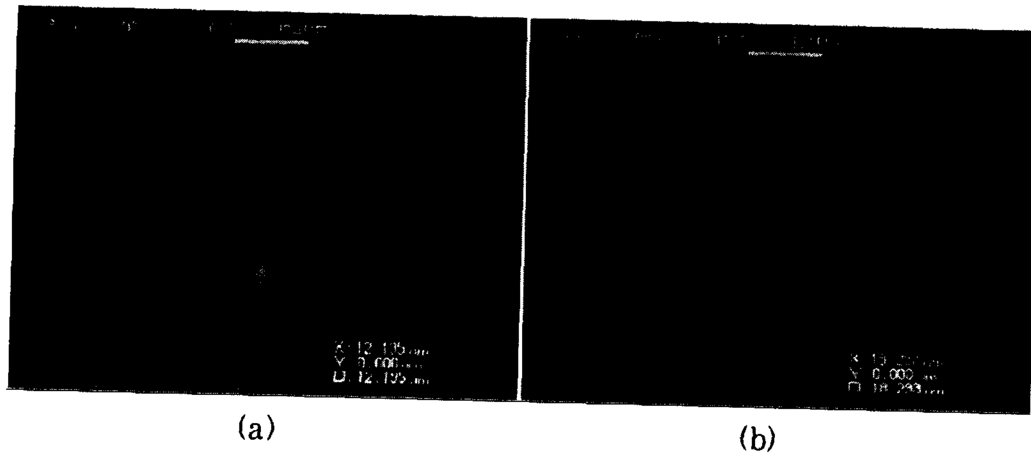

Fig. 1. Optical micrographs of LPs: (a) singular shape without flow pattern and (b) plural shape with flow pattern in as-received wafer (crystal pulling speed: 0.4 mm/min)

commercial DRAM (design rule : 0.38 μm) and ASIC (design rule : 0.50 μm) devices were fabricated on the fast-pulled, slow-pulled and hydrogen annealed wafers. and their device performance/yield were compared.

2. Experimental

Prime Si wafers of p-type (boron-doped, 6-7Ω·cm (100) 200 mm diameter) were taken from the middle position of two Cz crystals grown with a medium oxygen crystal growth program by applying different crystal pulling rates (0.4 mm/min and 0.7 mm/min). Oxygen and carbon concentrations measured using FTIR system were 12.7-13.4 ppma and <0.05 ppma (in new ASTM), respectively. Four kinds of thermal cycles, such as (1) 1100℃, 2 hours, dry oxidation, (2) 1200℃, 2 hours, dry oxidation, (3) 1200℃, 1 hour, wet oxidation, and (4) simulated 4-step based on 16Mbit DRAM process, were used to investigate thermal behavior of FPD and LP. For examination of the changes in radial profiles and morphologies of FPD and LP, non-agitation Secco etching for 30 min (in this case the etched thickness of Si wafer was about 20 μm) was applied to as-received and heat-treated samples. Then, the defect density and morphology were investigated using optical microscope. To understand the effect of LP upon device performance/yield, commercial DRAM (design rule : 0.38 μm) and ASIC (design rule : 0.50 μm) devices were fabricated on the fast-pulled, slow-pulled and commercially available hydrogen annealed wafers. By comparing radial profile of LP on slow-pulled wafers with EDS (Electrical Die Sorting) yield, we tried to figure out the effect of LP upon device yield/performance. In case of device processed wafers, non-agitated Secco-etching is applied after removing the device layer using HF solution (49 mol%).

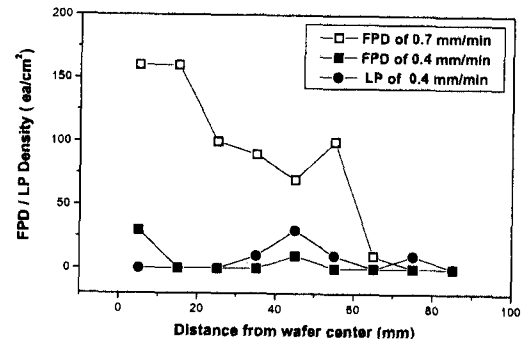

Fig. 2. Radial distribution of FPD and LP in as-received wafers grown with the pulling speed of 0.4 mm/min and 0.7 mm/min (LP was not found in the crystal with the pulling speed of 0.7 mm/min)

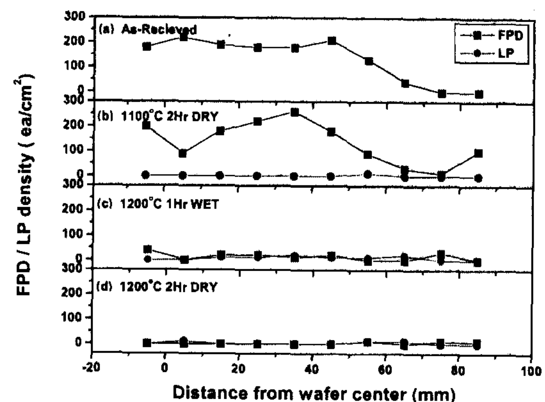

Fig. 3. Dependence of FPD and LP densities on heat treatment condition (a) as-received, (b) 2 hours of dry oxidation at 1100℃, (c) 2 hours of dry oxidation at 1200℃, and (d) 1 hour of wet oxidation at 1200℃) in the crystal grown with the pulling speed of 0.7 mm/min

3. Results and Discussion

3.1 Thermal Behavior of FPD and LP

Fig. 1 shows micrographs of LPs observed in the crystal grown with 0.4 mm/min after non-agitated Secco-etching for 30 min. LPs in thecrystal grown with 0.4 mm/min were composed of either singular or

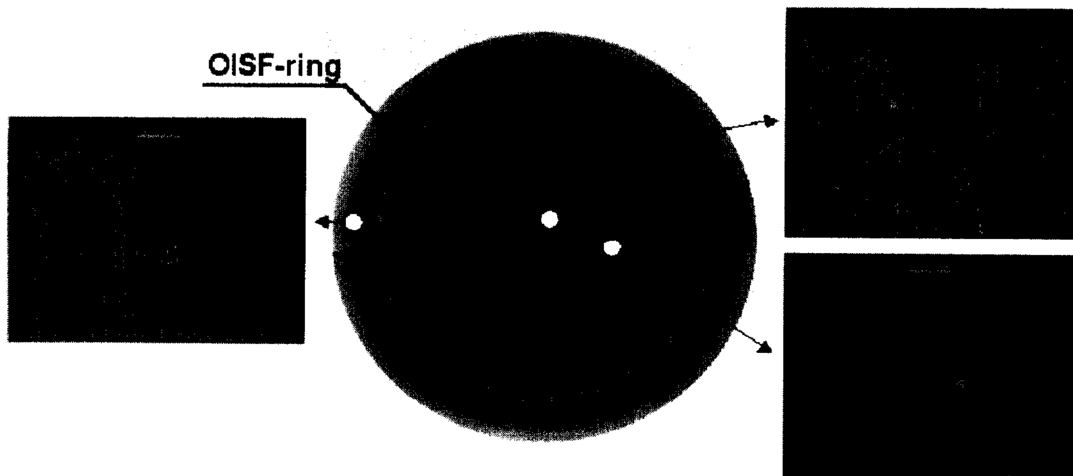

Fig. 4. Optical micrographs of LPs and X-ray Lang topograph with MoKα 1/(440) diffraction in the wafer grown with the pulling speed of 0.7 mm/min after simulated 4-step based on 16Mbit DRAM process.

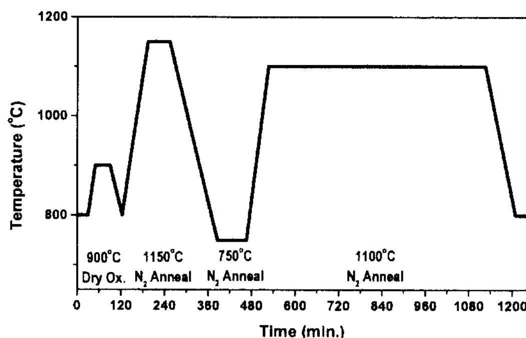

Fig. 5. Schematic showing of the simulated 4-step based on the 16MDRAM process.

plural shapes and with or without flow pattern. The size of LP was 10-30 μm while typical size of the FPD tip was smaller than 1 μm.

The radial distribution of FPD and LP in the crystals grown with 0.7 mm/min and 0.4 mm/min were shown in Fig. 2. It is clear that FPD level lower than 30 ea/cm^2 can be obtained by performing crystal growth with the slow pulling rate of 0.4 mm/min, which is in good agreement with the results of previous studies.[1,5,6] However, as indicated by Sadamitsu et al.[6] this slow crystal growth have a tendency to generate LPs whereas the crystal grown with the pulling speed of 0.7 mm/min showed no LP and higher FPD density. In case of the crystal grown with the pulling speed of 0.7 mm/min, it should be pointed out that there was a boundary at the distance of 70 mm from wafer center where FPD density decreased quickly, which is known as an oxidation induced stacking fault (OISF)-ring. It is said that this OISF-ring divides wafer area into two regions-vacancy-rich region (inside OISF-ring) and interstitial-rich region (outside OISF-ring).[7] According to Sadamitsu et al., the grown-in defects revealed by the non-agitation Secco-etching can be classified into vacancy related defects (FPD ; observed in vacancy rich region) and interstitial related defects (LP ; observed in the interstitial rich region) by their generation locus.

In order to investigate the thermal behavior of FPD and LP, adjacent wafers from each crystal were annealed with four kinds of thermal cycles and then inspected under optical microscope after non-agitation Secco etching for 30 min. Fig. 3 shows the dependence of FPD and LP densities on heat treatment condition in case of the crystal with the pulling speed of 0.7 mm/min. These data clearly indicate that FPD can be annihilated by high temperature ($\geq$1100℃) annealing, and the higher the heat treatment temperature, the faster the reduction rate of FPD density. These results are in general agreement with those of comparatively extended works on the characteristic of FPD.[4,5]

And, it should be noted that LP was generated during high temperature annealing, even though the density of LPs was not so significant and lower than 10 ea/cm^2. It could be a result of the interstitial si atoms that generated by the stress at the si/oxide interface during high temperature annealing. It is also remarkable that LP generation was not confined within a specific region such as inside or outside OISF-ring in wafer and no relationship between the decrease of FPD and LP generation was observed. Judging from these results, even though both FPD and LP were revealed by non-agitated Secco-etching, the origins of FPD and LP seemed to be quite different.

The data in Fig. 4 reconfirm whether LP generation is confined to a specific region in wafer or not. The

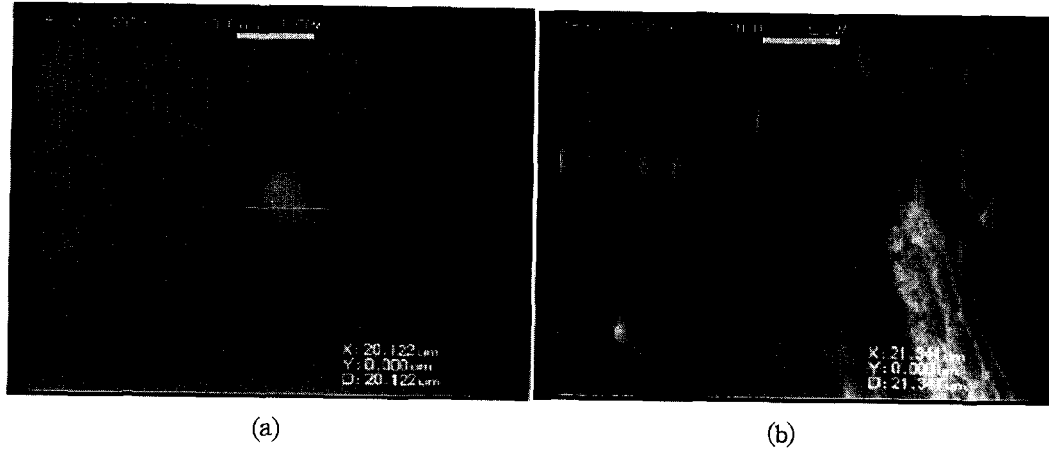

Fig. 6. Optical micrographs of LPs (a) without and (b) with flow pattern in ASIC device-processed wafer grown with crystal pulling speed of 0.7 ㎜/min

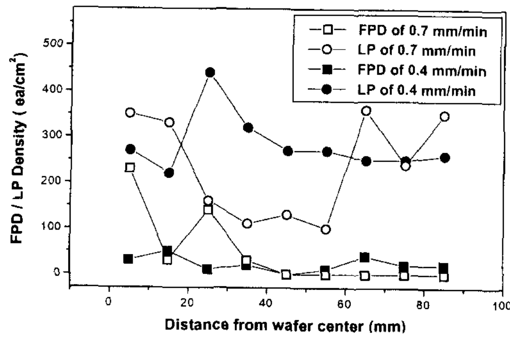

Fig. 7. Radial distribution of FPD and LP in ASIC device-processed wafers grown with crystal pulling speed of 0.4 mm/min and 0.7 mm/min.

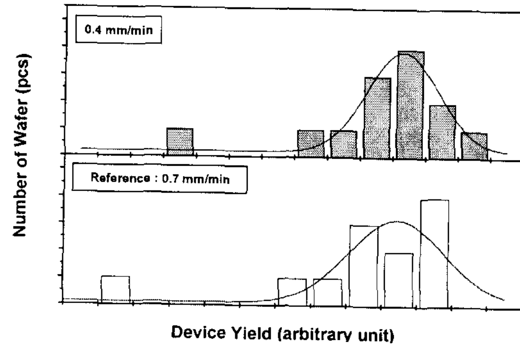

Fig. 8. Device yield comparison between crystals grown with the pulling speed of 0.4 ㎜/min and 0.7 ㎜/min after ASIC device (design rule : 0.5 ㎛) fabrication.

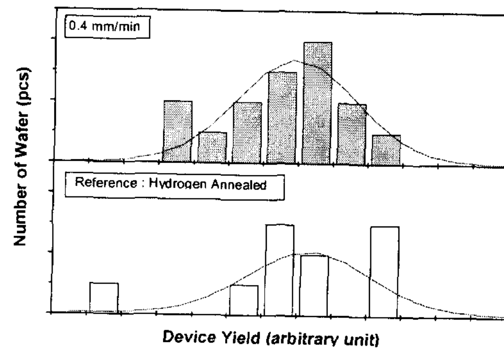

Fig. 9. Device yield comparison between hydrogen-annealed wafer and the crystal grown with the pulling speed of 0.4 ㎜/min after DRAM device (design rule : 0.38 ㎛) fabrication.

samples taken from the crystal prepared with the pulling speed of 0.7 ㎜/min were thermally annealed using simulated 4-step based on 16Mbit DRAM process which illustrated in Fig. 5. For verification of the OISF-ring, X-ray Lang topograph was taken with MoKα1 / (440) diffraction after simulated 4-step. As observed in Fig. 4, LPs were generated both at the inside and at the outside of OISF-ring through simulated 4-step based on 16Mbit DRAM process. Contrast to the case for the model proposed by Sadamitsu et al.[6], which indicated that LP is generated only at the outside of OISF-ring, The results showed that no dependency on the wafer locus which is divided by OISF-ring. Thus the excess interstitial Si atom might not be the origin of the LP generation.

3.2 Effect of LP on Device Yield

In order to investigate the effect of LP on device yield, ASIC (design rule : 0.5 ㎛) and DRAM (design rule : 0.38 ㎛) devices were fabricated and electrical function test was performed. After EDS (electric Die Sorting), samples were taken and non-agitation Secco etching is applied to confirm the effect of LP on the device performance/yield.

Fig. 6 shows the shapes of LPs observed in the samples with the pulling speed of 0.7 ㎜/min after ASIC device processing after removing device layer using HF solution and non-agitated Secco-etching. These shapes are just the same as those in the as-received wafers grown with the pulling speed of 0.4 ㎜/min as shown in

Fig. 1. Therefore, it can be clearly said that LPs were generated in the wafers grown with the pulling speed of 0.7 mm/min through ASIC device processing and the average density is about 240 ea/cm^2 (Fig. 6). It is also noticeable that the average density of LP in the samples grown with the pulling speed of 0.4 mm/min was increased from 6 ea/cm^2 (Fig. 2) to 280 ea/cm^2 (Fig. 7) after ASIC device fabrication. Even though ASIC device-processed wafers contain significant number of LPs, the final device yield on these wafers is kept at a satisfactory level in manufacturing line (Fig. 8). In addition, the wafers (grown with the pulling speed of 0.4 mm/min) which contain LPs in as-received state showed no yield difference compared to hydrogen-annealed wafers which contain no LPs in as-received state after DRAM device fabrication (Fig. 9).

Judging from these results, it seems that LP does not have detrimental effects on the performance/yield of device whose design rule is larger than 0.35 μm, even though the other properties such as reliability test was not considered at this time.

4. Conclusion

The nature of FPD and LP in Cz Si crystals and their effects on device yield/performance were investigated through high temperature (≥1100℃) annealing and ASIC/DRAM device fabrication. The results show that

1) FPD can be annihilated by high temperature annealing and the higher the heat treatment temperature, the faster the reduction rate of FPD density.

2) The origins of FPD and LP seem to be fully different since LP was generated at the temperature higher than 1100℃ and its generation was not confined within a specific region such as inside or outside OISF-ring in wafer.

3) LP revealed by non-agitation Secco etching for 30 min does not have detrimental effects on the performance / yield of device whose design rule is larger than 0.35 μm.

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