Korean J. Crystallography
Vol. 12, No. 3, pp.162~165, 2001

Co-Silicide Device Characteristics in Embedded DRAM

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Abstract

The EDL (Embedded DRAM and Logic) technologies with stack cell capacitors based on NO dielectric and Co-silicided source/drain junctions using a Ti capping material, were successfully implemented. The employed Co-silicided film exhibited junction leakage characteristics comparable to those of non-silicided junctions. Improved device characteristics without degradation of I_{off} was also achieved.

1. Introduction

Titanium silicide ($TiSi_2$) and cobalt silicide ($CoSi_2$) have been employed as gate electrode materials in silicon-based very large-scale integration (VLSI) circuits, as a consequence of their low electrical resistivities and good process compatibilities.[1,2] $TiSi_2$, however, suffers from high electrical resistivity for sub-0.25 micron generations due to the difficulty of phase transition from high resistivity C-49 phase to low resistivity C-54 phase during the second rapid thermal annealing (RTA) of the two-step RTA process.[3] Meanwhile, since $CoSi_2$ could maintain its low resistivity on much narrower lines, it has been employed as gate electrode material by several companies targeting for their sub-0.25 micron technology generations.[4]

Recently, needs for Embedded DRAM and Logic (EDL) technology have been rapidly increasing in an effort to merge DRAM cell arrays and logic circuits in a single chip for the advantages of lower power consumption and higher performance.[5] We have employed cobalt silicide as a source/drain contact material to maintain high-speed logic devices in the EDL technology.[6] In order to establish the process integration for the EDL, the silicide process of the source and drain (S/D) junctions of the MOSFETs should be carefully exploited to endure the high temperature processes for stack cell capacitors.

This study has investigated the thermal stability of Ti capped Co-silicide for additional post heat treatments during capacitor building processes in DRAM part. After the full integration of EDL including DRAM processes, n+/p junction leakage characteristics of Co silicides comparable to those of non-silicide junctions were obtained.

2. Experimental

Figure 1 shows a simple process flow for silicidation and the post heat treatments that were used to evaluate the effect of $CoSi_2$ film. After forming trench isolation and gate patterning, 150 nm thick sidewall spacers were formed in two steps. These thick spacers were used for the protection of the cell array region against silicidation of the S/D of the MOSFETs without additional processes. Arsenic ion implantation was performed for n+/p junction of

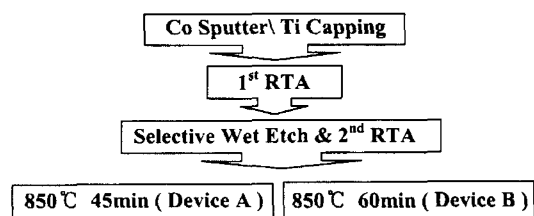

Fig. 1. Co-silicide formation and post heat treatment process flow.

nMOSFETs. After dilute HF acid treatment at the S/D active region, $CoSi_2$ film was formed with a Ti capping material that slows down the agglomeration and prevents the oxygen contamination. In the case of DRAM part, a stack capacitor structure based on NO dielectric was used. Subsequently, BPSG layer was deposited and subjected to a reflow process for planarization for 20 min at 850°C. DRAM cell array with the cell size of 0.56 μm^2 and 0.35 μm logic design rule were used in cell and core/peri regions, respectively.

3. Results and Discussion

Figures 2(a) and (b) show the cumulative probability of n+/p junction leakage currents on area and edge intensive diode patterns. Two devices, to be referred to as device A and B, with respective post heat treatment at 850°C for 45 min and 60 min after the S/D implantation and the subsequent annealing for ion activation were used. Junction leakage current was measured at 4 V and 85°C for both in area and edge intensive diodes. Area components were

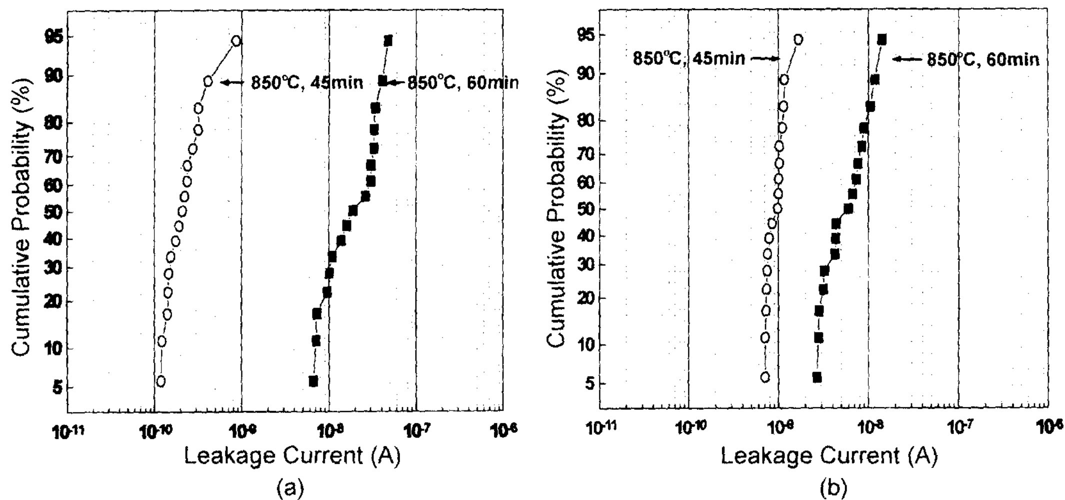

Fig. 2. Cumulative probability of measured n+/p reverse leakage currents in (a) area and (b) edge intensive diodes at 4 V and 85°C after post heat treatments at 850°C for 45 min and 60 min.

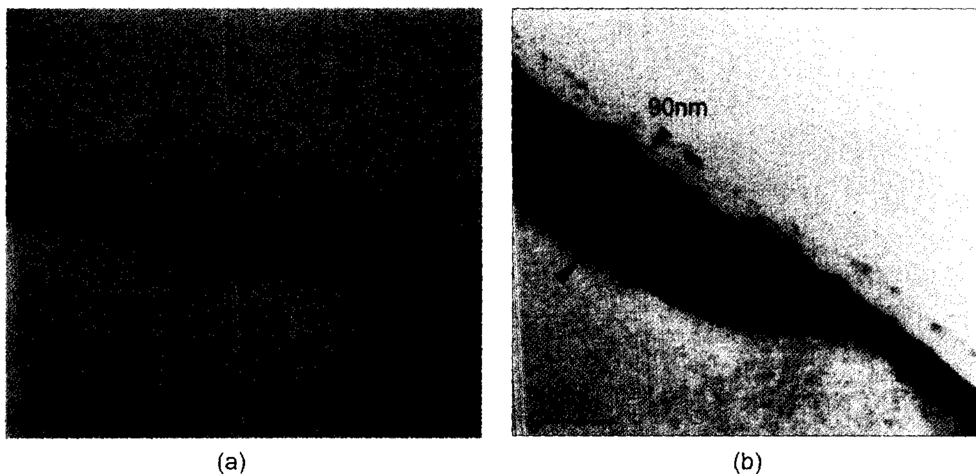

Fig. 3. TEM pictures of $CoSi_2$ after post heat treatment at 850°C for (a) 45 min and (b) 60"Cmin.

calculated by 4 fA/μm^2 for device A and 160 fA/μm^2 for device B. For edge components, 26 fA/μm and 124 fA/μm were obtained, respectively. From these results, it was found that leakage currents were more strongly dependent on the area than the edge component, indicating that the area junction is degraded more severely than the edge junction by the thermal treatment.

In device A, Co-silicide film thickness is in the range of 40 to 50 nm, as shown by the TEM cross-sectional micrograph in Fig. 3(a). However, Fig. 3(b) shows a localized Co-silicide protrusion after the post heat treatment at 850°C for 60 min. The thickness of the Co-silicide protrusions ranged from 85 to 100 nm, which might be enough to increase the leakage current of the area intensive diode.

In order to improve the increased leakage current, we performed an additional phosphorus implantation. In Fig. 4, we compared the results of leakage currents at 4V and 85°C, both with and without additional phosphorus implantation at 30 KeV, 3.0×10^{13} cm^{-2}. A noticeable reduction was observed of the leakage currents in area and edge intensive diodes by 1 and 0.5 orders of magnitude, respectively. These results suggest that the leakage current could be reduced by increasing junction depth and/or doping concentration at the $CoSi_2$/Si interface through an additional phosphorous implantation.

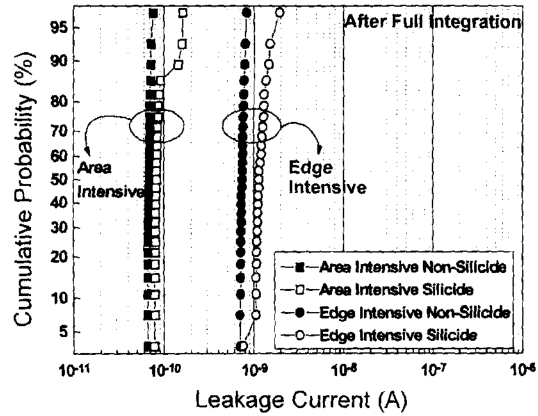

Fig. 5. Cumulative probability of measured n+/p reverse leakage currents with and without Co-silicidation after DRAM integration.

Figure 5, which was measured at 4 V and 85°C, shows the cumulative probability of n+/p junction leakage current. After experiencing the full EDL processes, the leakage current level of silicided devices comparable to that of non-silicided ones was obtained.

V_g-I_d and V_d-I_d characteristics of non-silicided and Co-silicided nMOSFETs are shown in Fig. 6. Compared to the non-silicided nMOSFET, Co-silicided nMOSFET shows improved I_{dsat}, the saturated drain current, without degradation of I_{off}, the off current.

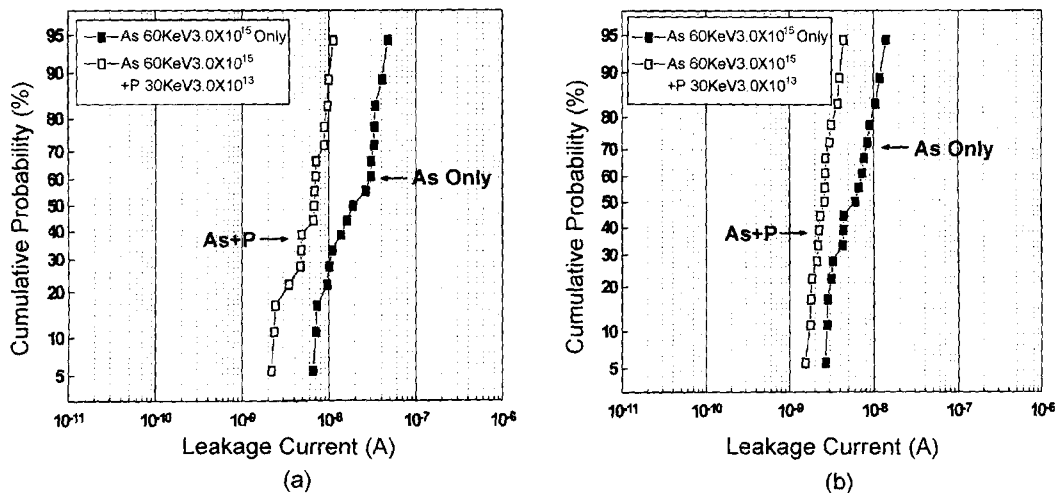

Fig. 4. Cumulative probability of measured n+/p reverse leakage currents in (a) area and (b) edge intensive diodes at 4 V and 85°C both with and without additional Phosphorus ion implantation.

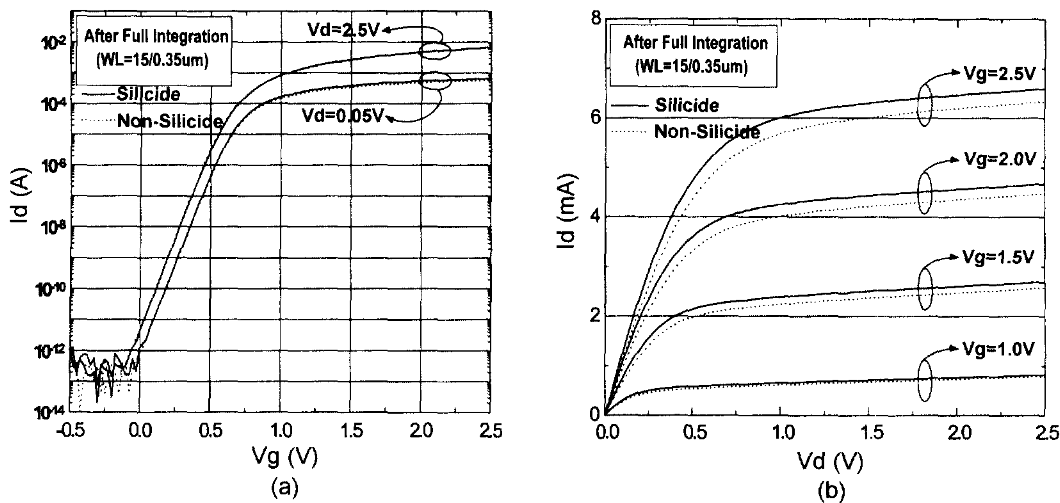

Fig. 6. **(a) V_g-I_d and (b) V_d-I_d characteristics of nMOS with and without Co-silicidation after full integration.**

The improved device characteristics were attributed to the reduction of contact/sheet resistance, which is mainly due to an enlarged diffusion contact area. Measured n+ sheet resistance and contact resistance of 0.38×0.38 μm^2 size are 6 $\Omega/\square$ and 9 Ω/contact, respectively.

4. Conclusion

EDL technologies with stack cell capacitors based on NO dielectric and Co-silicided S/D junctions using a Ti capping material, were successfully implemented. The employed Co-silicided film has a high thermal budget to endure the subsequent DRAM processes and shows excellent electrical properties. Furthermore, we found that the thermal budget could be further extended by introducing additional phosphorus ion implantation after arsenic source/drain ion implantation. The n+/p junction leakage characteristics comparable to those of non-silicided junction were obtained and the improved device characteristics were achieved without degradation of I_{off}.

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