Progress in Superconductivity Vol.3 No.1 pp17-22 31 October 2001

Issues in Building Large RSFQ Circuits

J. H. Kang*
University of Incheon, Incheon, Korea
Received 20 August 2001

대형 RSFQ 회로의 구성

강준희

Abstract

Practical implementation of the SFQ technology in most application requires more than single-chip-level circuit complexity. Multiple chips have to be integrated with a technology that is reliable at cryogenic temperatures and supports an inter-chip data transmission speed of tens of GHz. In this work, we have studied two basic issues in building large RSFQ circuits. The first is the reliable inter-chip SFQ pulse transfer technique using Multi-Chip-Module (MCM) technology. By noting that the energy contained in an SFQ pulse is less than an attojoule, it is not very surprising that the direct transmission of a single SFQ pulse through MCM solder bump connectors can be difficult and an innovative technique is needed. The second is the recycling of the bias currents. Since RSFQ circuits are dc current biased the large RSFQ circuits need serial biasing to reduce the total amount of current input to the circuit.

Keywords : single, flux, quantum, Josephson, logic, circuits, multiple, serial, cloc k

I. Introduction

Superconductive electronics [1-3] is a promising application area of superconductivity. Superconductive digital electronics is a future digital device and uses Josephson junctions as switching elements. Josephson junction is known to be a very fast switching device, and its switching speed can be as small as a fraction of a pico-second. However, early work on Josephson digital devices [4] did not fully utilize the full switching speed of Josephson junction. This was because of the punch-through effect in the hysteretic Josephson junctions. Switching Josephson junctions could be done at very fast speed, but the reset had to be done no faster than a few tenth of a nanosecond. Therefore, the operating speed of this latching logic circuits was limited to a few GHz. Using overdamped Josephson junctions has been suggested to overcome this problem because the overdamped Josephson junction is non-hysteretic and needs no external resets. Due to the lack of maintaining a voltage state with the non-hysteretic Josephson junctions, a new way of building Josephson digital circuits had to be used.

A flux quantum stored in an inductor and controlled by a Josephson junction has been used to build a fast Josephson digital circuit [5]. A counter was built with this Single Flux Quantum (SFQ) logic

*Corresponding author. Fax: +82 32 766-8018
e-mail: jhkang@incheon.ac.kr

and operated at 116 GHz. Due to the high-speed operation of SFQ counter, a high-resolution analog-to-digital converter was built with this technology [6]. A further improvement was made when the resistors in the SFQ logic circuits were removed [7].

There has been a great advancement in the new Rapid Single Flux Quantum (RSFQ) logic circuits development in recent years. A toggle flip-flop (TFF) circuit was built with this technology and operated at 770 GHz. More complicated circuits have been built, which include analog-to-digital (A/D) converters [8], digital-to-analog (D/A) converters [9], time-to-digital converters [10], network switches [11], etc. Performances of these circuits are superior to the circuits made with other technologies because of the ultra-low power consumption and high switching speed of Josephson junctions. Fig. 1 shows the power consumption and the switching speed of the Josephson junctions used in SFQ logic circuits compared to other technologies.

So far, these developments have been primarily restricted to the single chip level because the technique to transfer SFQ pulses between chips has not been well established. By noting that the energy contained in an SFQ pulse is less than an atto-joule, it is not very surprising that a reliable inter-chip SFQ pulse transfer technique is still under development [12-13]. Multi-chip module (MCM) technology has been suggested as a strong candidate to achieve this goal [14-15].

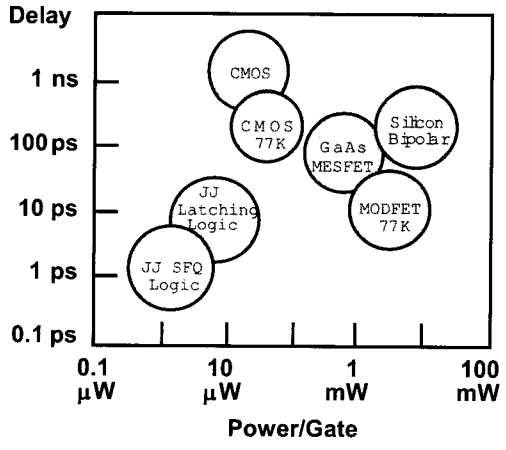

Fig. 1. Power consumption and the switching speed of the various electronic devices.

The main advantage of using SFQ circuits than other superconductive circuits is that SFQ circuits use only dc biases. This greatly simplifies the interference problems caused by ac biasing. However, when the circuit size becomes large the total amount of dc bias current can add up to tens of amperes. To ease this problem we need to recycle the current by biasing the circuits serially. Magnetically coupled JTLs are extremely important when one wants to send SFQ pulses through the circuits that are serially biased. The circuits that are serially biased must have different ground planes so that the SFQ pulses in different ground planes have no galvanic connections. For example, simultaneously biasing twenty four circuits in different ground planes will reduce the required current from roughly 10 A to less than 500 mA, which is a significant reduction in the large scale SFQ circuits.

The need for generation and distribution of a stable, low-jitter on-chip clock is critical in building large circuits. It is extremely challenging to produce a high-speed clock that has both low-jitter and long-term phase stability. Long Josephson junction (LJJ) technology can be an intermediate solution to this problem, but developing an RSFQ clock is an ultimate goal to achieve the hundreds of giga-hertz RSFQ large scale circuits.

II. Multi-chip module

Due to the large impedance mismatch between the Josephson Transmission line (JTL) and the solder bump connectors used in MCM configuration, direct transmission of a single SFQ pulse through MCM solder bump connectors can be difficult. Sending a dc voltage signal, instead of sending a single SFQ pulse, is much more effective to overcome the impedance mismatch problem. To achieve this goal we need to develop two high-speed circuits, a transmitter circuit that converts a single SFQ pulse to dc voltage signal and a receiver circuit that converts a dc voltage signal to a single SFQ pulse.

The overall scheme of this strategy is shown in Fig. 2. As shown in Fig. 2, the SFQ pulses to be sent to other chips are converted into the toggled dc voltage signal by a transmitter in a chip. This toggled dc voltage signal is sent to another chip through MCM interconnects. Finally, the SFQ pulses

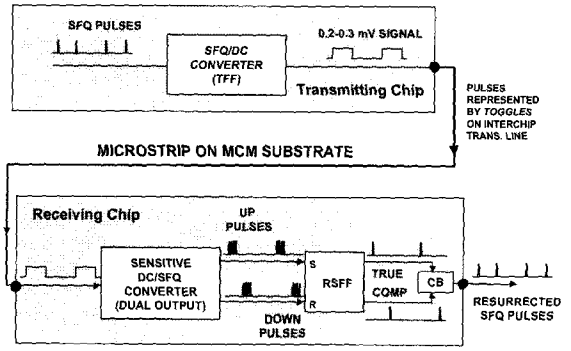

Fig. 2. Schematic diagram showing the flow diagram of SFQ pulse transmission through MCM interconnects. MCM substrate is used only for the passive signal transmission.

duplicating the original SFQ pulse pattern are extracted from the toggled dc voltage signal with a receiver.

MCM substrate in Fig. 2 was a carrier chip where only passive microstrip transmission lines and DC bias lines were present. MCM interconnects were composed of microstrip transmission lines and InSn bump bonds [14]. We used 5 ohm microstrip lines for passive interconnects. The usual lengths of microstrip lines used in this work were several millimeters.

Transmitter was an SFQ/DC converter, a toggle flip-flop (TFF) with dc read out. In this circuit each SFQ pulse toggles the output voltage between the two voltage levels. The usual output voltage levels were 0 mV and 0.2 – 0.3 mV.

In receiver, a sensitive DC/SFQ converter was used to convert the toggled voltage signal to short SFQ pulse trains. A SQUID based DC/SFQ converter had a dual output, an up pulse branch and a down pulse branch. The rising edge of the input voltage caused a short pulse train on the up pulse branch, and the falling edge caused a short pulse train on the down pulse branch. By using an RS flip-flop (RSFF) we converted each train of SFQ pulses to a single pulse. This could be done because only the first SFQ pulse sets RSFF to either set state or reset state depending on the input branch where the pulses enter.

The subsequent pulses in the short pulse train were rejected from the RSFF by floating junctions. By combining the two outputs from RSFF by using a confluence buffer (CB), complete recovery of the original signal was accomplished. The mask layout

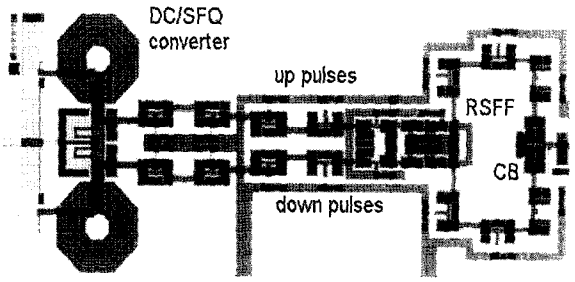

Fig. 3. Mask layout of the receiver circuit. Voltage signal is input from the left. Each voltage toggle in input signal is converted to an SFQ pulse leaving at the right.

of the receiver is shown in Fig. 3, where the main circuit components were labeled.

The transmitter circuit is a well-known TFF and confluence buffer is a common circuit. Therefore, combination of dual output DC/SFQ converter and RSFF, used to convert toggled dc voltage signal to SFQ pulses, are the key components to achieve the present scheme of MCM transmission.

Various circuits to test this scheme were constructed by using standard Hypres Nb process[16] with junction critical current density of 2.5 kA/cm^2. MCM chips were flip chip mounted on the carrier chips using InSn solder bumps [14]. The size of each solder bump was about 100μm in diameter.

Circuits built to test the receiver showed that it worked at 20 GHz. The tested circuit had receiver functions of generating streams of up pulses and down pulses from toggled dc voltage signal and of converting a short pulse train to a single SFQ pulse.

To perform a high frequency test with low bandwidth scope an asynchronous beat frequency test is often used [17]. We constructed a flash A/D converter and operated it in beat frequency mode. The difference between input signal frequency and clock frequency becomes the beat frequency in the output of flash A/D converter. Test results at 5 GHz are shown in Fig. 4. The 3rd scope trace shown in Fig. 4 is 10 kHz reference signal. Data "0"s are represented as either "0" or "1" states and data "1"s an average of "0" and "1" states. This is because we used TFF type DC/SFQ converter for data monitor output, considering the data flow was a single stream. In TFF type DC/SFQ converter there is no voltage toggle in "0" states and voltage toggles in "1" states. The 1st traces in Fig. 4 are from the data monitor

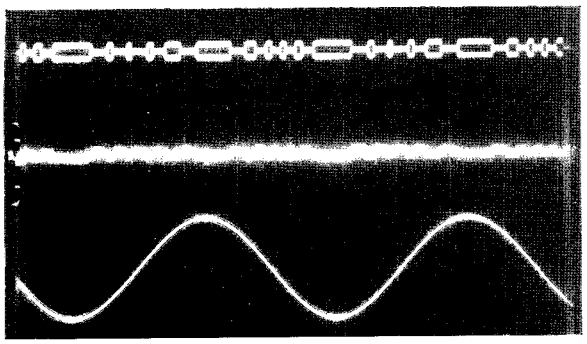

Fig. 4. Test results of one bit MCM digitizer chip at 5 GHz. Data monitor outputs, shown in the first traces, are from TFF type SFQ/DC converter, and the outputs from memory buffer, shown in the second traces, are from RSFF type SFQ/DC converter. 10 kHz reference signals are also shown in the third traces.

outputs and the 2nd traces are after the signal transfer through MCM. The circuit was proved to work at 10 GHz. Either the comparator or the probe limited the test speed. Further work is needed to test at the higher speeds.

III. Bias current recycling

Reduction of the bias currents can be achieved by serial biasing. The circuits in serial bias must have different ground planes, and SFQ pulses in different ground planes will have no galvanic connections. To transfer SFQ pulses between the circuits on different ground planes we need a magnetically coupled Josephson transmission lines. The circuit that we designed is shown in Fig. 5. To test the actual operation of SFQ pulse transfer through magnetic coupling, we designed a circuit whose block diagram is as shown in Fig. 6. First we separated a region by ground plane moats. In this way we created a region with ground plane 2, while the other area had ground plane 1 as their ground. We used DC/SFQ converter that was a SQUID to generate the SFQ pulses from an analog input signal. Each of these SFQ pulses induced an SFQ pulse in the magnetically coupled JTL laid on ground plane 2. Each of the output pulses from this magnetically coupled JTL was split to two pulses. One was sent to Output 1 to monitor the correct pulse transfer and the other was sent to another magnetically coupled circuits to transfer to the SFQ circuit on the ground plane 1. Toggle

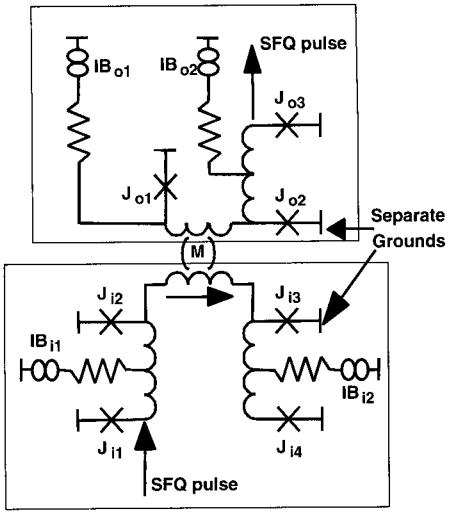

Fig. 5. Circuit schematics for the magnetically coupled SFQ pulse transfer circuit. An SFQ pulse enters from the bottom and travels through JTLs in the bottom circuit. Magnetic coupling induces an SFQ pulse on the top circuit that uses a different ground plane.

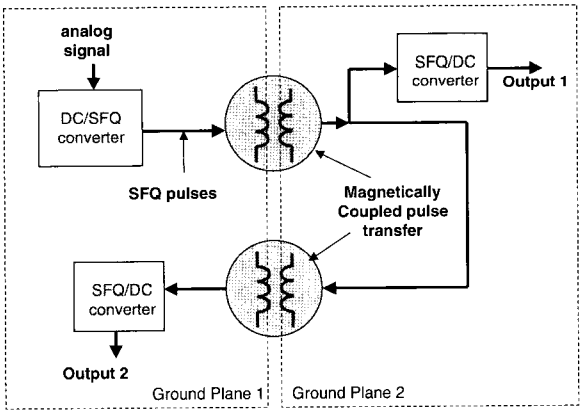

Fig. 6. Block diagram of the circuit designed to test the magnetically coupled SFQ pulse transfer circuit. Complete transmission of SFQ pulses through the circuits on separate ground planes can be tested with this circuit.

flip-flop (TFF) type SFQ/DC converters were used to monitor Output 1 and Output 2. The circuits were fabricated by using the ten-level Nb process with junction critical current density of 2.5 kA/cm^2.

The test results are shown in Fig. 7. At each positive slope of the input signal, an SFQ pulse was generated and transmitted to the magnetically coupled pulse transfer circuit. The first trace shows

the voltage output from Output 1. In TFF type DC/SFQ converter, there is a voltage toggle whenever an SFQ pulse enters. Output 1 showed the correct voltage toggle for each positive slope of the input signal. Correct outputs from Output 2 showed that the second magnetically coupled pulse transfer circuit also operated correctly. Due to the low bandwidth of the scope used in this experiment the test speed was limited to 2 MHz.

The same circuit was successfully applied to operate an 8-stage shift register built on the floating ground plane.

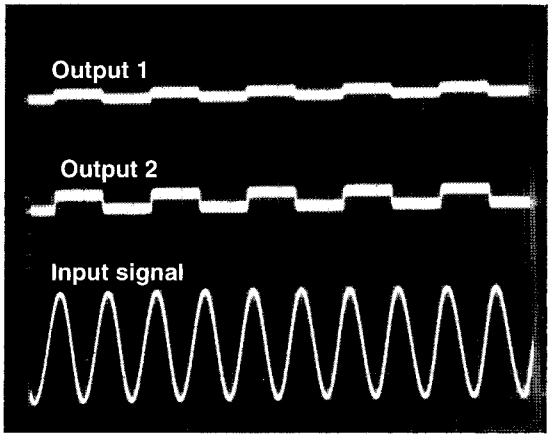

Fig. 7. Test results of the magnetically coupled SFQ pulse transfer. At each positive slope of the input signal an SFQ pulse is generated and is sent to output 1 and output 2. Each SFQ pulse toggles the output voltage of output 1 and output 2, showing the correct operation of the circuit. This scope picture was taken at 100 kHz

IV. Conclusion

Rapid Single Flux Quantum (RSFQ) logic circuit development has advanced a lot in recent years. However, most of these developments were limited to the single chip level efforts. In most practical applications, we need to integrate the multiple chips. The important issues in achieving this are reliable inter-chip SFQ pulse transfer technique, current recycling, and reliable clock distribution. We found that the reliable inter-chip SFQ pulse transfer technique can be achieved by using a Multi-Chip-Module (MCM) technology, where a conversion process between the SFQ pulse signal and the dc voltage signal was used. We also found that the current recycling can be achieved by using magnetically coupled Josephson transmission lines.

Acknowledgments

This work was supported in part by the Korea Ministry of Science and Technology. The work at University of Inchon was partly supported by the Korea Science and Engineering Foundation through the Multimedia Research Center at University of Inchon.

References

[1] Y. H. Kim, C. H. Kim, T. S. Hahn and S. S. Choi, J. H. Kang, S. J. Park, "Building SFQ Circuits with High-Tc Superconductors," J. of Korean Physical Society, 31, 76-79 (1997).

[2] Sang Young Lee and V. B. Fedorov, "A Study of the TE_{011} Mode Resonant Frequency of a Dielectric Loaded Resonator with HTS Films Having Finite Thicknesses," J. of Korean Physical Society, 36, 316-322 (2000).

[3] J. H. Kang and S. E. Choi, "Thermal Noise Induced Bit Error Rates of Josephson Devices," J. of Korean Physical Society, 30, 306-309 (1997).

[4] S. Hasuo, IEEE Trans. on Magnetics, "High-Speed Josephson Integrated Circuit Technology," 25, 740-749 (1989).

[5] C. A. Hamilton and Frances L. Lioyd, "100 GHz Binary Counter Based on DC SQUID," IEEE Electron Devices Letters, vol. EDL-3, 335-338 (1982).

[6] D. L. Miller, J. X. Przybysz, J. H. Kang, C. A. Hamilton, and D. M. Burnell, "Josephson Counting A/D Converter," IEEE Trans. on Magnetics, 27, 2761-2764 (1991).

[7] K. Likharev and V. Semenov, "RSFQ Logic/Memory Family: A New Josephson-Junction Technology for Sub- Terahertz Clock-Frequency Digital Systems," IEEE Trans. on Applied Superconductivity, 1, 3-28 (1991).

[8] O. A. Mukhanov, V. K. Semenov, W. Li, T. V. Filippov, D. Gupta, A. M. Kadin, D. K. Brock, A. F. Kirichenko, Y. A. Polyakov, and I. V. Vernik, "A Superconductor High-Resolution ADC," IEEE Trans. on Applied Superconductivity, 11, 601-606 (2001).

[9] S. P. Benz, C. A. Hamilton, C. J. Burroughs, T. E.

Harvey, L. A. Christian, and J. X. Przybysz, "Pulse-Driven Josephson D/A converter," IEEE Trans. on Applied Superconductivity, 8, 42-47 (1998).

[10] A. F. Kirichenko, S. Sarwana, O. A. Mukhanov, I. V. Vernik, Y. Zhang, J. H. Kang, and J. M. Vogt, "RSFQ Time Digitizing System," IEEE Trans. on Applied Superconductivity, 11, 978-981 (1998).

[11] S. Tahara, S. Yorozu, Y. Kameda, Y. Hashimoto, H. Numata, T. Satoh, W. Hattori, and M. Hidaka, "Superconducting Digital Electronics," IEEE Trans. on Applied Superconductivity, 11, 463-468 (2001).

[12] J. X. Przybysz, D. L. Miller, S. S. Martinet, J. H. Kang, A. H. Worsham, and M. L. Farish, "Interface Circuits for chip-to-chip data transfer at GHz rate," IEEE Trans. on Applied superconductivity, 7, 2657-2660 (1997).

[13] M. Maezawa, H. Yamamori, and A. Shoji, "Chip-to-chip communication using a single flux quantum pulse," IEEE Trans. on Applied superconductivity, 10, 1603-1605 (2000).

[14] K. E. Yokoyama, G. Akerling, A. D. Smith, and M. Wire, "Robust superconducting die attach process," IEEE Trans. on Applied superconductivity, 7, 2631-2634 (1997).

[15] S. Tanabashi, T. Kubo, K. Kawabata, R. Jikuhara, G. Kaji, M. Terasawa, H. Nakagawa, M. Aoyagi, I. Kurosawa, and S. Takada, "Superconductive wiring in multichip module for josephson lsi circuits," Japanese J. of Applied Physics, 32, 898-900 (1993).

[16] HYPRES design rules can be found at Hypres web site at www.hypres.com.

[17] P. D. Bradley, "A 6-bit Josephson Flash A/D converter with GHz input band width," IEEE Trans. on Applied superconductivity, 3, 2550-2557 (1993).