JPE 1-2-3

A High-Power Step-up Converter with High Efficiency and Fast Control-to-Output Dynamics

Jeong-il Kang[1], Chung-Wook Roh[2], Gun-Woo Moon[1], and Myung-Joong Youn*[1]

[1]Korea Advanced Institute of Science and Technology, Taejon 305-701, Korea

[2]Samsung Electronics Co., LTD, Suwon City 442-742, Korea

ABSTRACT

A new high-power step-up based on the two-module parallel-input/series-output (PISO) modular dual inductor-fed push-pull converter is proposed. The proposed converter is operated at a constant duty cycle and employs an auxiliary circuit to control the output voltage with a phase-shift between two modules. It shows a high efficiency due to the greatly reduced switch turn-off stress. It also shows a high and linear voltage conversion ratio, low current stress in the output capacitor, and fast control-to-output dynamics. The operation principles and the mathematical models of the proposed converter are presented. Features of the proposed converter are discussed in comparison with the two-module PISO modular dual inductor-fed push-pull converter. Also, experimental results from a 50kHz, 800W, 350Vdc prototype with an input voltage range of 20 – 32Vdc are provided to confirm the validity of the proposed converter. The new converter compares favorably with the conventional counterpart, and is considered well suited to high-power step-up applications.

Key Words : high-power step-up converter, high efficiency, fast dynamics

1. Introduction

The step-up power conversion technique finds increasing necessities and power capability demands in applications such as electric vehicles, uninterrupted power supplies (UPS), servo-drive systems, and photovoltaic systems. The fuel cell power system [1,2], which is recently gaining a lot of attention as a new alternative power source, also makes a good application of a step-up converter since the voltage generated by each cell is relatively low about 0.75V. However, the high input current of the step-up converter makes it difficult to develop a high-performance converter in view of step-up ratio, power capability, efficiency, and dynamic response. The high input current is a problem especially in high-power and high-output voltage applications since it causes a serious degradation in the power conversion efficiency and step-up ratio, or sometimes results in a unfeasibly high switch current stress. Among various remedies for this problem, the parallel-input/series-output (PISO) modularisation[3] approach has many desirable features for high-power step-up applications. Moreover, the dual inductor-fed push-pull converter, or in short, the dual converter [4,5] appears to be a good candidate for a base module of the PISO modular step-up converter. However, the output voltage sensitivity is high in the PISO modular step-up converter, and the switch turn-off voltage stress which results in considerably large losses in switching devices is overlooked. In the mean time, compared to a step-down converter with a second order *LC* filter, a step-up converter generally requires a larger output capacitance to effectively remove the switching ripples. This, however, results in a decrease

Manuscript received May 3, 2001; revised August 21, 2001.
Corresponding Author: mmyoun@ee.kaist.ac.kr, Tel: +82-42-869-3498, Fax: +82-42-869-3410

in the control-to-output bandwidth [6]. Therefore, the step-up converter with a large-valued output capacitor for a low output voltage ripple is short of an ability to respond quickly to disturbances. Furthermore, the right half-plane (RHP) zero [7] in the control-to-output transfer function of a step-up converter is another problem limiting the closed-loop dynamic performance [8].

In this paper, a new phase-shifted PISO dual inductor-fed push-pull converter based on the conventional two-module PISO modular dual inductor-fed push-pull converter is proposed. The new converter features a high step-up ratio, small root-mean-square (RMS) current in the output capacitor, and a greatly reduced switch turn-off stress so that the converter efficiency can be significantly improved. It also shows a linear voltage conversion characteristic to changes in the control input and a fast control-to-output transient response under low influence of the RHP zero.

The steady-state operation of the proposed converter is analyzed and the mathematical models are presented. Features of the proposed converter are discussed through a comparative analysis with the conventional two-module PISO dual inductor-fed push-pull converter. Also, experimental results from a 50kHz, 800W, 350Vdc prototype with an input voltage range of 20 – 32Vdc are presented to validate the proposed converter.

2. Operation Principle

Fig. 1 shows a circuit diagram of the phase-shifted PISO dual inductor-fed push-pull converter, where a resistive load R_o is assumed. It consists of two identical dual inductor-fed push-pull converters [4], which is named hereafter as dual converter, with a common voltage source V_i, and an auxiliary circuit. The auxiliary circuit is composed of tertiary windings, a full-wave rectifier, and LC filter components. Both modules are operated with a constant duty cycle D and a phase-shift ϕ between the modules. The bottom module denoted by module 2 is assumed to have a lagging phase. The switching period is defined as T_s. To simplify the steady-state analysis all the circuit components are assumed ideal. All the inductors and the capacitors are assumed large enough to be approximated by constant current and voltage sources within one switching cycle.

The turns ratio of the primary and secondary windings is

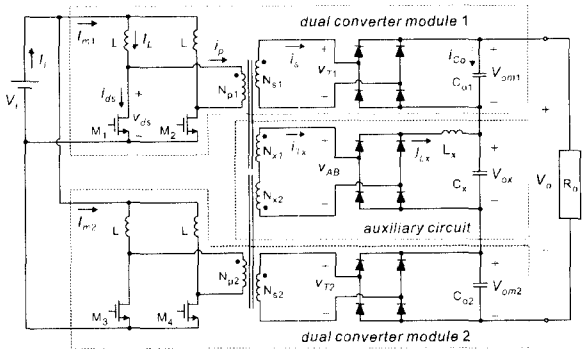
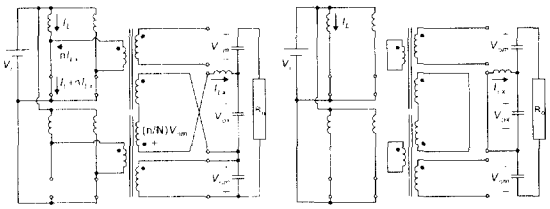
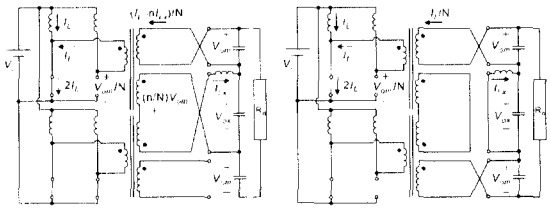


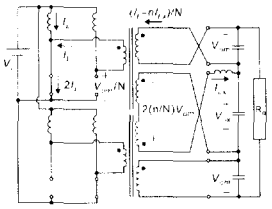
Fig. 1. Circuit diagram of proposed converter



(a) Sub-topology 1 (b) Sub-topology 2



(c) Sub-topology 3 (d) Sub-topology 4



(e) Sub-topology 5

Fig. 2. Sub-topologies of proposed converter

defined as $N = N_s/N_p$, and that of the primary and tertiary windings is defined as $n = N_x/N_p$. The undotted ends of the tertiary windings are connected together so that the voltage between the dotted ends, denoted by v_{AB}, becomes $(n/N)(v_{T1} - v_{T2})$, where v_{T1} and v_{T2} are the instantaneous secondary voltages. The voltage v_{AB} is rectified in the auxiliary circuit, and the LC filter produces an averaged dc voltage V_{ox}. By imposing the constant volt-second relationship on the boost inductor L, it is easily shown that the output voltage of each module is independent of ϕ, and

is the same as that of a stand-alone dual converter, that is, $V_{om1} = V_{om2} = V_{om} = NV_i/(1-D)$.

Under steady-state conditions, one switching cycle of the proposed converter is divided into eight operational modes according to the switching states. Four modes in a half of the switching cycle are equivalent to those in another half of the switching cycle, except that the switching states of left and right legs are interchanged. Thus the analysis is concentrated on the first half of the switching cycle, where one switching cycle is assumed to begin with conduction of M_1.

In the first half of the switching cycle, the proposed converter takes one of the five sub-topologies shown in Fig. 2 at each operational mode. The sequences of sub-topologies for various operating conditions and the resultant waveforms are shown in Table 1 and Fig. 3, respectively. Waveforms of other switches and windings omitted in Fig. 3 can be obtained by shifting or mirroring their counterparts shown in each figure.

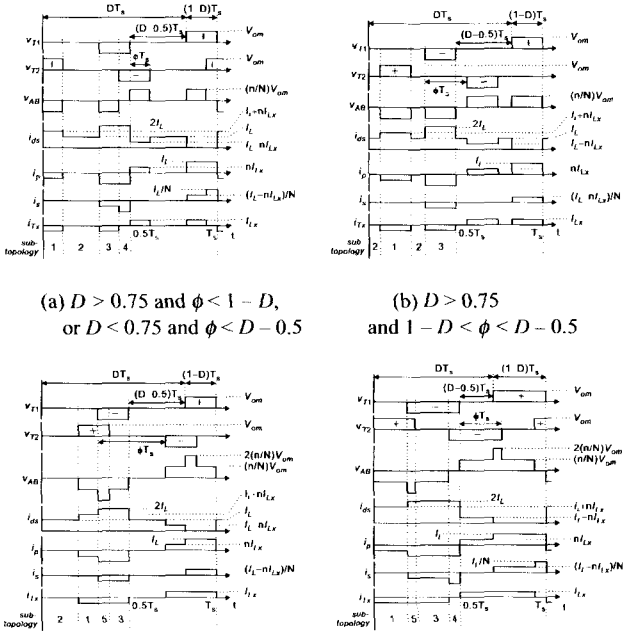
2.1 Operation Principle: $D > 0.75$

If $\phi = 0$, the waveforms of v_{T1} and v_{T2} completely overlap with each other. In this case, the voltage v_{AB} and the auxiliary output voltage V_{ox} become zero. The proposed converter at this condition is equivalent to the conventional two-module PISO dual converter without the auxiliary circuit. If $\phi \neq 0$, the rectangular waves of v_{T1} and v_{T2} are out of phase with each other to the amount of ϕT_s, and they cannot be completely cancelled in the auxiliary circuit. The non-overlapped portions of the waves of v_{T1} and v_{T2} are reflected to the waveform of v_{AB} with an amplitude of $(n/N)V_{om}$. Fig. 3(a) shows typical operating waveforms of the proposed converter when ϕ is slightly larger than zero. Four operational modes in the first half of the switching cycle are analyzed below.

Mode 1 ($t_0 - t_1$): Module 1 is in a boost phase and module 2 is in a powering phase. The sub-topology for this mode is shown in Fig. 2 (a). During this mode, the voltage across N_{x1} is 0 and the voltage across N_{x2} is $(n/N)V_{om}$, resulting in $v_{AB} = -(n/N)V_{om}$. The tertiary windings N_{x1} and N_{x2} carry a current $i_{Tx} = -I_{Lx}$, where I_{Lx} denotes the current flowing in the LC filter inductor L_x. In module 2, the primary current is divided into the secondary current and the tertiary current i_{Tx}. On the other hand, in module 1, the current i_{Tx} is reflected to the primary side and circulates through M_1 and M_2.

Table 1 Sequence of sub-topologies in the first half switching cycle

D	ϕ	sub-topological sequence
$D > 0.75$	$0 < \phi < 1-D$	$1 \rightarrow 2 \rightarrow 3 \rightarrow 4$
$D > 0.75$	$1-D < \phi < D-0.5$	$2 \rightarrow 1 \rightarrow 2 \rightarrow 3$
$D > 0.75$	$D-0.5 < \phi < 0.5$	$2 \rightarrow 1 \rightarrow 5 \rightarrow 3$
$D < 0.75$	$0 < \phi < D-0.5$	$1 \rightarrow 2 \rightarrow 3 \rightarrow 4$
$D < 0.75$	$D-0.5 < \phi < 1-D$	$1 \rightarrow 5 \rightarrow 3 \rightarrow 4$
$D < 0.75$	$1-D < \phi < 0.5$	$2 \rightarrow 1 \rightarrow 5 \rightarrow 3$



(a) $D > 0.75$ and $\phi < 1-D$, or $D < 0.75$ and $\phi < D-0.5$

(b) $D > 0.75$ and $1-D < \phi < D-0.5$

(c) $D > 0.75$ and $D-0.5 < \phi < 0.5$, or $D < 0.75$ and $1-D < \phi < 0.5$

(d) $D < 0.75$ and $D-0.5 < \phi < 1-D$

Fig. 3. Waveforms of proposed converter for various operating conditions

The switch M_1 therefore carries a current $i_{ds} = I_L + nI_{Lx}$. This mode continues for ϕT_s until the switch M_3 is turned on and module 2 enters a boost phase at $t = t_1$.

Mode 2 ($t_1 - t_2$): All the switches are turned on and both modules are in boost phases. The transformer primaries are short-circuited by the switches, while the secondaries are open-circuited by the rectifier diodes. Due to the short-circuited primaries, the voltages v_{T1} and v_{T2} become zero, therefore making v_{AB} also zero. The current I_{Lx} forces all the rectifier diodes in the auxiliary circuit to turn on and freewheels through them while being equally divided in both diode legs. The sub-topology for this mode is shown in Fig. 2 (b). The duration of this mode is $(D-0.5-\phi)T_s$.

Mode 3 (t_2– t_3): This mode is similar to mode 1 except that the roles of module 1 and 2 are interchanged as shown in Fig. 2 (c). The output voltage of module 1 is reflected to N_{x1}, and the voltage v_{AB} becomes $-(n/N)V_{om}$ again. The primary current i_p of module 1 is divided into the secondary current $i_x = -(I_L - nI_{Lx})/N$ and the tertiary current $i_{Tx} = -I_{Lx}$, as shown in Fig. 3 (a). The current i_{Tx} reflected to the primary side of module 2 circulates through M_3 and M_4. This mode continues for ϕT_s until the switch M_4 is turned off and module 2 enters a powering phase at $t = t_3$.

Mode 4 (t_3– t_4): As shown in Fig. 2 (d), the switches M_1 and M_3 are turned on, and M_2 and M_4 are turned off, making both modules be in powering phases. Both of the transformers have voltages of the same polarity. The voltages reflected to N_{x1} and N_{x2} are exactly cancelled so that the voltage v_{AB} becomes zero. As in mode 2, all the rectifier diodes in the auxiliary circuit are turned on and carry the freewheeling current of I_{Lx}. This completes one half of the switching cycle and another half begins with conduction of the switch M_2. The duration of this mode is $(1 - D - \phi)T_s$.

By imposing the constant volt-second relationship on the LC filter inductor L_x for the first half of the switching cycle described above, the steady-state output voltage of the auxiliary circuit is obtained as

$$V_{ox} = 4\frac{n}{N}V_{om}\phi \tag{1}$$

Equation (1) can also be obtained by geometrically averaging the area of the waveform of v_{AB} shown in Fig. 3 (a).

If $1 - D < \phi < D - 0.5$, the rectangular wave of v_{T2} entirely deviates from the equally signed wave of v_{T1}. Therefore, those waveforms of v_{T1} and v_{T2} cannot be cancelled any more. Instead, all the waves of v_{T1} and v_{T2} are individually reflected to the auxiliary circuit side, as shown in Fig. 3 (b). As ϕ is increased, the rectangular wave of v_{T2} approaches the oppositely signed wave of v_{T1} without affecting V_{ox}.

If $\phi = D - 0.5$, the rectangular wave of v_{T2} meets the oppositely signed wave of v_{T1} on the time axis, while the equally signed waves of v_{AB} come together to match each other. If ϕ is further increased. overlapped portions of the oppositely signed waves of v_{T1} and v_{T2} begin to appear, resulting in a stepwise waveform of v_{AB} as shown in Fig. 3 (c). Although the waveshape of v_{AB} is modified as ϕ is increased, the total area of the waveform of v_{AB}, which is equivalent to V_{ox}, still remains independent of ϕ. The sub-topology for this instance is shown in Fig. 2 (e). During this stage, both modules are in powering phases with opposite polarities in the transformers. The voltages on N_{x1} and N_{x2} also have opposite signs, and the auxiliary circuit delivers power to the output with $v_{AB} = -2(n/N)V_{om}$.

3. Modeling of proposed converter

The state-space averaging method [6] is employed to model the proposed converter. It is assumed that all the elements except for the switching devices are ideal, and currents and voltages are uniformly distributed under a balanced condition.

Since all the boost inductor currents as well as the output voltages of both modules have no differences in an averaged sense, they can be treated with one state variable. Thus the state variables are defined by i_L, v_{om}, i_{Lx}, and v_{ox}. Referring to the sub-topologies shown in Fig. 2 with considerations on R_{ds}, the large-signal model of the proposed converter is obtained as follows:

$$\dot{i}_L = \frac{V_i}{L} - \frac{v_{om}}{NL}(1-D) - \frac{(3-2D)i_L}{L}R_{ds} \tag{2}$$

$$\dot{v}_{om} = \frac{2i_L}{NC_o}(1-D) - \frac{2n\phi}{NC_o}i_{Lx} - \frac{2v_{om}}{R_oC_o} - \frac{v_{ox}}{R_oC_o} \tag{3}$$

$$\dot{i}_{Lx} = \frac{4nv_{om}}{NL_x}\phi - \frac{v_{ox}}{L_x} - \frac{8n^2R_{ds}i_{Lx}}{L_x}\bar{\phi} \tag{4}$$

$$\dot{v}_{ox} = \frac{i_{Lx}}{C_x} - \frac{2v_{om}}{R_oC_x} - \frac{v_{ox}}{R_oC_x} \tag{5}$$

where $0 < \phi < 1 - D$ and $\bar{\phi} = \min\{\phi, D - 0.5\}$. Although the steady-state analysis of the proposed converter has shown that the sequence of the sub-topologies varies depending on operating conditions, the model is found to be independent of the conditions. Substituting all the

derivative terms on the left hand sides of (2) ~ (5) with zeros yields steady-state solutions of the proposed converter as

$$V_{om} = \frac{NV_i}{1-D}\left[1+\frac{(3-2D)\left(\frac{N+2n\phi}{1-D}\right)^2\frac{R_{ds}}{R_o}}{1+8n^2\frac{R_{ds}}{R_o}\bar{\phi}}\right]^{-1} \tag{6}$$

$$V_{ox} = \frac{4n\phi}{N}V_{om}\frac{1-4nN\frac{R_{ds}}{R_o}}{1+8n^2\frac{R_{ds}}{R_o}\bar{\phi}} \tag{7}$$

$$I_{Lx} = \frac{2V_{om}+V_{ox}}{R_o} \tag{8}$$

$$I_L = \frac{1}{2}\frac{N+2n\phi}{1-D}I_{Lx} \tag{9}$$

The small-signal model of the proposed converter is obtained by linearizing the equations of the large-signal model given by (2) ~ (5) as follows:

$$\begin{bmatrix}\hat{i}_L\\ \hat{v}_{om}\\ \hat{i}_{Lx}\\ \hat{v}_{ox}\end{bmatrix} = \mathbf{A}\begin{bmatrix}\hat{i}_L\\ \hat{v}_{om}\\ \hat{i}_{Lx}\\ \hat{v}_{ox}\end{bmatrix} + \mathbf{B}\begin{bmatrix}\hat{v}_i\\ \hat{\phi}\end{bmatrix} \tag{10}$$

where

$$\mathbf{A} = \begin{bmatrix} -\frac{(3-2D)R_{ds}}{L} & -\frac{1-D}{NL} & 0 & 0\\ \frac{2(1-D)}{NC_o} & -\frac{2}{R_oC_o} & -\frac{2n\phi}{NC_o} & -\frac{1}{R_oC_o}\\ 0 & \frac{4n\phi}{NL_x} & -\frac{8n^2R_{ds}\bar{\phi}}{L_x} & -\frac{1}{L_x}\\ 0 & -\frac{2}{R_oC_x} & \frac{1}{C_x} & -\frac{1}{R_oC_x}\end{bmatrix},$$

and

$$\mathbf{B} = \begin{bmatrix}\frac{1}{L} & 0\\ 0 & -\frac{2nI_{Lx}}{NC_o}\\ 0 & \frac{4nV_{om}}{NL_x}-\frac{8n^2R_{ds}I_{Lx}}{L_x}\alpha\\ 0 & 0\end{bmatrix}.$$

where $\alpha = 0$ when $\phi > D - 0.5$ and $\alpha = 1$ when $\phi < D - 0.5$. The input vector consists of the small-signal input voltage and phase-shift. By defining an appropriate output equation, (11) can be solved to obtain a transfer function from any variable in the input vector to an output of interest. Note that all the mathematical expressions of the proposed converter are reduced to those of the conventional two-module PISO dual converter by removing all dependencies on i_{Lx}, v_{ox}, and ϕ.

4. Feature and comparative analysis

4.1 Voltage conversion characteristic

A duty cycle controlled step-up converter is generally considered to have an asymptotic voltage conversion characteristic, while a step-down converter has a linear one. The rapidly changing output voltage of the step-up converter makes a design of the feedback loop critical. Since the auxiliary circuit behaves like a step-down converter, the proposed converter shows a voltage conversion ratio which is linear to ϕ. The step-up ratio of the proposed converter, including R_{ds}, can be obtained from (6), (7) and the relationship $V_o = V_{ox} + 2V_{om}$ as (11) shown below. The step-up ratio of the conventional PISO dual converter can be obtained by replacing ϕ in (11) with zero as follows:

$$\frac{V_o}{V_i} = \frac{2N}{1-D}\left[1+\left\{(3-2D)\left(\frac{N}{1-D}\right)^2\right\}\frac{R_{ds}}{R_o}\right]^{-1} \tag{12}$$

$$\frac{V_o}{V_i} = \frac{2N+4n\phi}{1-D}\left[1+\left\{8n^2\bar{\phi}+(3-2D)\left(\frac{N+2n\phi}{1-D}\right)^2\right\}\frac{R_{ds}}{R_o}\right]^{-1} \tag{11}$$

The step-up ratios of the proposed converter for different ϕ's are shown in Fig. 4. The transformer is designed as N =1.7 and n = 2, and R_{ds} is assumed $0.0015R_o$. The bottom curve with upright triangles represents the step-up ratio of the proposed converter when ϕ = 0. This coincides with that of the conventional PISO dual converter given by (12). The other four curves show that, at the same duty cycle, the proposed converter gives a higher step-up ratio than the conventional PISO dual converter. To attain the same step-up ratio, the conventional PISO dual converter should be operated at a larger duty cycle than the proposed converter.

4.2 Device stress

Table 2 shows several important design equations of both converters. In the equations of the proposed converter, the phase-shift ϕ is assumed to have a value between 0 and 1 − D. By matching the ampere-second balance of the output capacitor, the steady-state relation between I_o and I_L is obtained as follows:

$$I_L = \frac{N + 2n\phi}{2(1-D)} I_o \tag{13}$$

which is similar to the relation between V_o and V_i. Each equation of the RMS current can be normalized with respect to either I_L or I_o using (13). It is noted that the equations of the proposed converter are reduced to those of the conventional PISO dual converter by replacing ϕ with zero.

The equations in Table 2 are graphically shown in Fig. 5 as a function of step-up ratio, where all the RMS currents are normalized with respect to the load current I_o. The dashed line in each graph represents the stress in the conventional PISO dual converter obtained by varying D from 0.7 to 0.82. On the other hand, the solid line represents the stress in the proposed converter obtained by varying ϕ from 0 to 0.3 at D = 0.7. The transformer parameters are N = 1.7 and n = 2 as previously designed and the input voltage is V_i = 24Vdc.

Since the proposed converter is operated at a smaller duty cycle than the conventional PISO dual converter, it shows a somewhat larger switch RMS current than the conventional PISO dual converter. However, the switch turn-off voltage V_{ds} of the proposed converter is maintained constant and lower than that of the conventional PISO dual converter. It should be noted that a switching device with a lower voltage rating generally shows a lower conduction loss. The low switch turn-off voltage of the proposed converter therefore reduces not only the switching loss but also the conduction loss by using a switching device with a smaller R_{ds}. It is shown in Fig. 5 (a) and (b) that the proposed converter shows a maximum 40% lower switch turn-off voltage than the conventional PISO dual converter at the expense of only 10% increase in the switch RMS current. Since the conventional PISO dual converter shows a maximum V_{ds}

Table 2. Design equations of two converters

	Proposed converter	Conventional PISO dual converter
Switch RMS current, $I_{dS,RMS}$	$\sqrt{2(nI_o)^2\bar{\phi} + (3-2D)I_L^2}$	$I_L\sqrt{(3-2D)}$
Switch turn-off voltage, V_{ds}	$\frac{V_i}{1-D}\left[1+(3-2D)\left(\frac{N+2n\phi}{1-D}\right)^2\left(1+8n^2\frac{R_{ds}}{R_o}\bar{\phi}\right)^{-1}\frac{R_{ds}}{R_o}\right]^{-1}$	$\frac{V_i}{1-D}\left[1+\frac{N^2(3-2D)}{(1-D)^2}\frac{R_{ds}}{R_o}\right]^{-1}$
Output capacitor RMS current, $I_{Co,RMS}$	$\sqrt{(2D-1)I_o^2 + 2\phi\left(\frac{I_L-nI_o}{N}-I_o\right)^2 + 2(1-D-\phi)\left(\frac{I_L}{N}-I_o\right)^2}$	$\sqrt{(2D-1)I_o^2 + 2(1-D)\left(\frac{I_L}{N}-I_o\right)^2}$
Primary RMS current, $I_{p,RMS}$	$\sqrt{2(nI_o)^2\bar{\phi} + 2(1-D)I_L^2}$	$I_L\sqrt{2(1-D)}$
Secondary RMS current, $I_{s,RMS}$	$\frac{1}{N}\sqrt{2\phi(I_L-nI_o)^2 + 2(1-D-\phi)I_L^2}$	$\frac{I_L}{N}\sqrt{2(1-D)}$
Tertiary RMS current, $I_{TS,RMS}$	$I_o\sqrt{2(\phi+\bar{\phi})}$	*NON*

* Each expression can be normalized with I_o or I_L using (14).

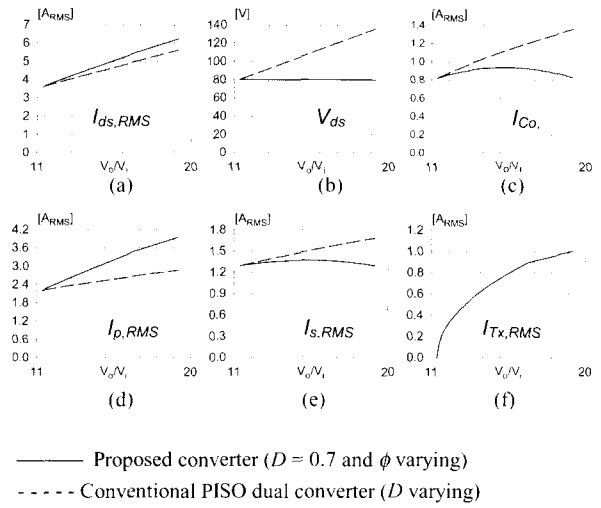


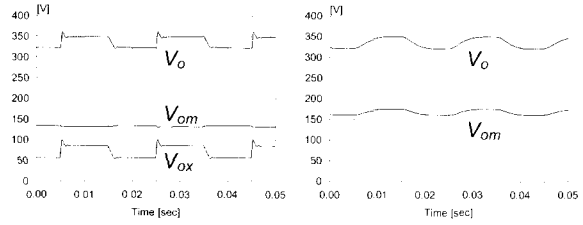
Fig. 5. Theoretical device stress in both converters (RMS currents are normalized with I_o): (a) Switch RMS current, (b) Switch turn-off voltage, (c) Capacitor RMS current, (d) Primary RMS current, (e) Secondary RMS current, (f) Tertiary RMS current

of 135V, IRFP250 with the voltage rating BV_{dss} of 200V and R_{ds} of 0.085Ω would be a good choice provided that a properly designed snubber circuit is employed. On the other hand, the proposed converter shows a constant V_{ds} of 80V over the entire operation range, so that IRFP150 with BV_{dss} of 100V and R_{ds} of 0.055Ω can be used to improve the efficiency.

Fig. 5 (c) shows that the output capacitor RMS current is small in the proposed converter. This advantage facilitates the selection of the high voltage output capacitor of the proposed converter. Fig. 5 (d), (e), and (f) show the RMS currents in the transformer windings of both converters. The secondary current is somewhat larger in the conventional PISO dual converter, while the primary RMS current is somewhat larger in the proposed converter.

4.3 Control-to-output dynamics

The trade-off between the fast transient response and the low output voltage ripple in determining the value of the output capacitor is significantly relieved in the proposed converter. This is because both modules are operated at a constant duty cycle and the auxiliary circuit regulates the overall output voltage. If the auxiliary circuit has a fast response speed dominating the overall converter dynamics, the transient response of the proposed converter can be greatly improved.



(a) Proposed converter: $D = 0.7$, $\phi = 0.1 \leftrightarrow 0.15$ (b) Conventional PISO converter: $D = 0.76 \leftrightarrow 0.78$

Fig. 6. Theoretical control-to-output responses of both converters

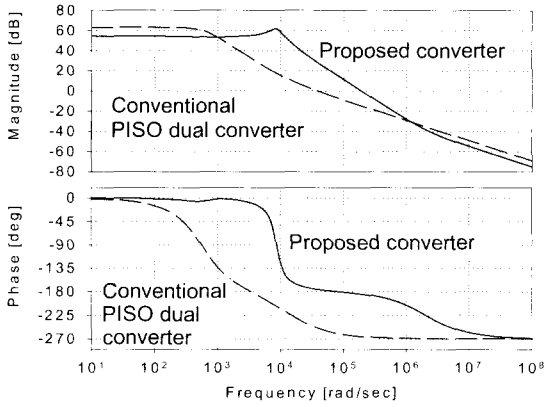


Fig. 7. Bode plots of control-to-output transfer functions of both converters

To investigate the control-to-output dynamics of both converters, the large-signal model simulations are made with the converter parameters given in the previous section. The operating condition of the proposed converter is D = 0.7. Relevant control inputs are applied to alternate the output voltages between 320Vdc and 350Vdc. Fig. 6 (a) shows the output voltage waveforms of the proposed converter obtained by alternating ϕ between 0.1 and 0.15. The corresponding waveforms of the conventional PISO dual converter are shown in Fig. 6 (b), where the duty cycle D is alternating between 0.76 and 0.78 to achieve the same output voltage swings. Due to the fast dynamics of the auxiliary circuit, the proposed converter shows a faster transient response than the conventional PISO dual converter.

Fig. 7 shows the Bode plots of the control-to-output transfer functions of both converters. The wide bandwidth of the proposed converter agrees with its fast response shown in Fig. 6 (a). The low frequency gain of the conventional PISO dual converter is 8.85dB, or 2.77 times

as large as that of the proposed converter. This verifies that the voltage conversion characteristic of the proposed converter is less sensitive to changes in the control input than that of the conventional PISO dual converter.

Another interesting feature common to most of step-up converters is the RHP zero in the small-signal control-to-output transfer function. Several techniques dedicated to eliminating the RHP zero in a step-up converter have been proposed. The suggestions are made that the converter parameters be properly designed to minimize the influence of the RHP zero by shifting this zero toward the positive infinity [9,10]. The RHP zero of the proposed converter is found to be located at 2.1×10^6 when $D = 0.7$ and $\phi = 0.15$, whereas the conventional PISO dual converter has this zero at 1.3×10^4 when $D = 0.78$. Since the RHP zero of the proposed converter is located over 150 times farther from the origin, this converter is much less affected by the unwanted RHP zero than the conventional PISO dual converter.

5. Experimental Results

A 50kHz, 800W, 350Vdc prototype with an input voltage range of 20 – 32Vdc has been constructed with circuit parameters shown in Table 3.

The rated input is 24Vdc and the rated operating conditions are $D = 0.7$ and $\phi = 0.15$. The conventional PISO dual converter is realized with the same components to those of the proposed converter except that the switching devices are IRFP250 due to the higher switch turn-off stress. The rated operating condition of the conventional PISO dual converter is $D = 0.78$.

Table 3. Circuit parameters of proposed converter

Switching frequency (f_s)	50 (kHz)
Switching devices (M_1, M_2, M_3, and M_4)	IRFP150
Boost inductor (L)	180 (μH)
Dual converter output capacitor (C_o)	600 (μF)
Auxiliary circuit inductor (L_x)	140 (μH)
Auxiliary circuit capacitor (C_x)	100 (μF)
Turn ratio of secondary : primary (N)	1.7
Turn ratio of tertiary : primary (n)	2

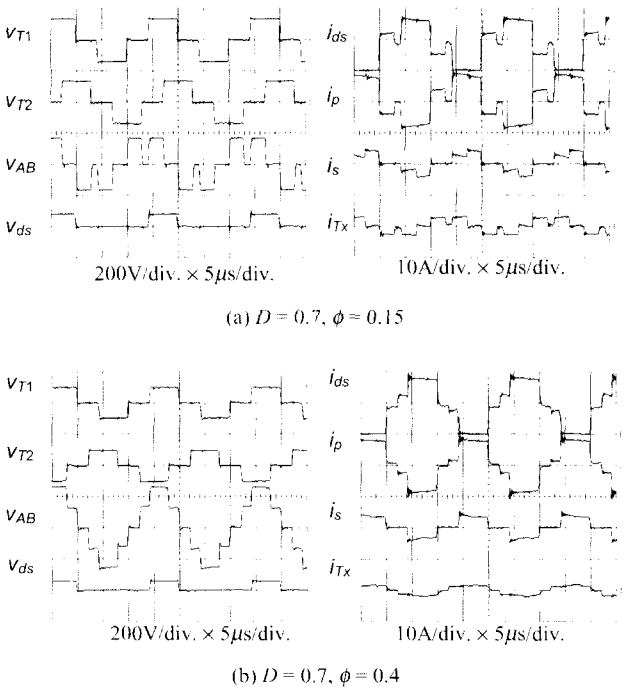


Fig. 8. Experimental operating waveforms of proposed converter

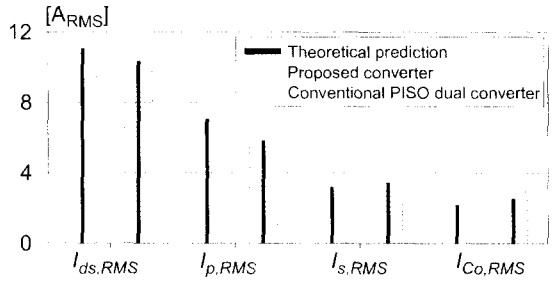
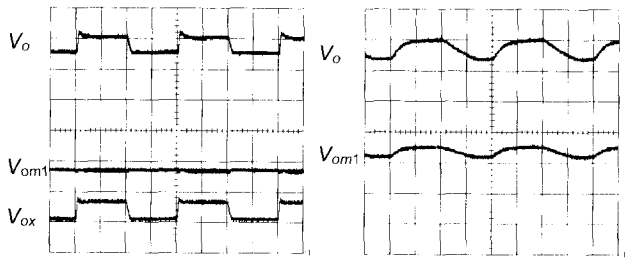


Fig. 9. Experimentally measured RMS currents in both converters

Fig. 8 (a) shows the measured operating waveforms of the proposed converter at the rated condition, where *RCD* snubbers are employed to protect the switches from high voltage surges. The waveforms clearly verify the theoretical waveforms shown in Fig. 3 (a). Fig. 8 (b) shows another results for $\phi = 0.4$ with a reduced input voltage. In this case, the phase-shift is so large that the overlap of oppositely signed waves of v_{T1} and v_{T2} takes place. These waveforms correspond to Fig. 3 (c).

The RMS currents of both the proposed converter and the conventional PISO dual converter are measured at their rated conditions. Fig. 9 shows the results in comparison with their theoretically predicted values. The measurements well agree with the theoretical predictions.



50V/div. × 5ms/div.
(a) Proposed converter
$D = 0.7$, $\phi = 0.1 \leftrightarrow 0.15$

50V/div. × 5ms/div.
(b) Conventional PISO dual converter
$D = 0.76 \leftrightarrow 0.78$

Fig. 10. Experimental waveforms of control-to-output transient responses of both converters

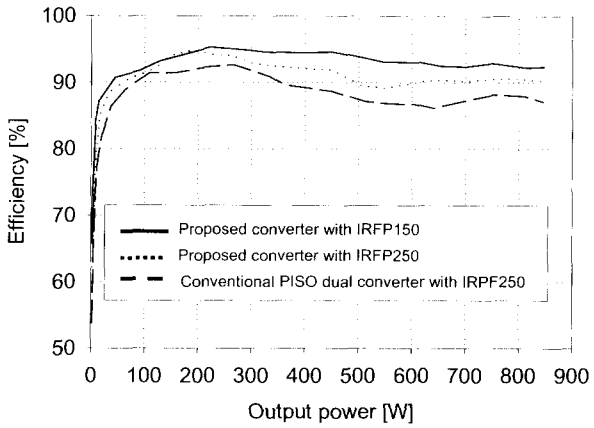


Fig. 11. Experimentally measured efficiencies of both converters

The control-to-output transient responses of both converters are shown in Fig. 10. The phase-shift of the proposed converter is changed between 0.1 and 0.15 to alternate the output voltage between 320Vdc and 350Vdc. The duty cycle of the conventional PISO dual converter is changed between 0.76 and 0.78 to achieve the same output voltage swing. The experimental waveforms confirm the results shown in Fig. 6 and also verify the validity of the large-signal model.

Fig. 11 shows the measured efficiencies of both converters. The solid line shows the efficiency of the proposed converter with IRFP150 and the dashed line shows the efficiency of the conventional PISO dual converter with IRFP250. The dotted line shows another result obtained from the proposed converter with IRFP250. As IRFP150 has a smaller turn-on resistance than IFRP250, the proposed converter, of course, shows a higher efficiency. Furthermore, the proposed converter still shows a higher efficiency than the conventional PISO dual converter although both converters make use of the same switching devices. This is because the low switch turn-off voltage of the proposed converter results in a low switching loss developed during switching transients.

6. Conclusion

A new phase-shifted parallel-input/series-output dual converter based on a conventional two-module PISO modular dual inductor-fed push-pull converter is proposed. Both modules are operated at a constant duty cycle and the output voltage is controlled with a phase-shift between two modules. The operation principles are analyzed and the mathematical models are presented. Features of this converter are discussed in comparison with the conventional two-module PISO dual inductor-fed push-pull converter. Also, experimental results from a 50kHz, 800W, 350Vdc prototype with an input voltage range of 20 – 32Vdc are presented to validate the proposed converter. This converter compares favorably with the conventional counterpart in many aspects as described below.

The proposed converter shows a high step-up ratio with a greatly reduced switch turn-off stress, so that it is possible to use a switching device with a low conduction loss. The low switch turn-off voltage also reduces the switching loss developed during switching transients. These compromise the slightly increased switch RMS current and result in a significant improvement in the power conversion efficiency.

The proposed converter also shows a small RMS current in the output capacitor, facilitating the selection of the high-voltage output capacitor. Due to the voltage conversion characteristic which is linear to control input variations and the fast control-to-output dynamics with a reduced influence of the RHP zero, the proposed converter can be easily stabilized without a loss in the closed-loop dynamic performance. Therefore, the proposed converter is considered well suited to high-power step-up applications.

References

[1] S. Rahman and K-S. Tam, "A feasibility study of photovoltaic-fuel cell hybrid energy system", *IEEE Transactions on Energy Conversion*, vol. 3, no. 1, pp. 50~55, 1988.

[2] J. H. Hirschenhofer, "Fuel cell status: 1996", *IEEE Aerospace and Electronics Systems Magazine*, vol. 12, no. 3, pp. 23~28, 1997.

[3] S. N. Manias and G. Kostakis, "Modular dc-dc converter for high-output voltage applications", *IEE Proceeding B*, vol. 140, no. 2, pp. 97~102, 1993.

[4] P. J. Wolfs, "A current-sourced dc-dc converter derived via the duality principle from the half-bridge converter", *IEEE Transactions on Industrial Electronics*, vol. 40, no. 1, pp. 139~144, 1993.

[5] W. C. P. De Aragao Filho and I. Barbi, "A comparison between two current-fed push-pull dc-dc converters - analysis, design and experimentation", *IEEE International Telecommunications Energy Conference Records*, pp. 313~320, 1996.

[6] R. D. Middlebrook and S. Cuk, "A general unified approach to modeling switching-converter power stages", *IEEE Power Electronics Specialists Conference Records*, pp. 18~34, 1976.

[7] G. W. Wester and R. D. Middlebrook, "Low-frequency characterization of switched dc-to-dc converters", *IEEE Transactions on Aerospace and Electronics Systems*, vol. AES-9, no. 3, pp. 376~385, 1973.

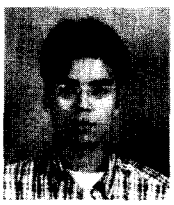
[8] K. H. Billings, *Switchmode Power Supply Handbook*, Mc Graw-Hill, pp. 3.136~3.141, 1999.

[9] D. M. Sable, B. H. Cho, and R. B. Ridley, "Elimination of the positive zero in fixed frequency boost and flyback converters", *IEEE Applied Power Electronics Conference Records*, pp. 205~211, 1990.

[10] W-C. Wu, R. M. Bass, and J. R. Yeargan, "Eliminating the effects of the right-half plane zero in fixed frequency boost converters", *IEEE Power Electronics Specialists Conference Records*, pp. 362~366, 1998.

Jeong-il Kang was born in Seoul, Korea, in 1973. He received the B.S. and M.S. degrees in electrical engineering in 1995 and 1997, respectively, from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, where he is currently working towards the Ph.D degree.

His research interests are in the areas of power electronics and control, including analysis, modeling, design and control of power converter, distributed power systems, and step-up power conversion techniques. He is a member of KIPE.



Chung-Wook Roh was born in Pusan, Korea, in 1971. He received the B.S. degree in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, in 1993 and the M.S. degree in electrical engineering and Ph.D. degree in electrical engineering and computer science, both from KAIST, Daejeon, in 1995 and 2000, respectively.

He joined the research and development group of Digital Television (DTV) Enabling Operations in Samsung Electronics Co. LTD., Suwon, in 2000 as a Senior Electrical Engineer. His research interests include the analysis and design of power conversion circuit in modern display system such as plasma display panel (PDP) driver, cathode ray tube (CRT) television, and wireless RF amplifier, and the innovative circuit techniques in various mixed analogue/digital system. Dr. Roh is a member of KIEE.

Gun-Woo Moon received the B.S. degree from Han-Yang University, Seoul, Korea, in 1990, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1992 and 1996, respectively.

He is currently an assistant professor in the department of electrical engineering and computer science, KAIST. His research interests include modeling, design and control of power converter, soft switching power converter, resonant inverters, distributed power systems, power factor correction, electric drive systems, driver circuit of PDP and flexible AC transmission systems (FACTS). Dr. Moon is a member of KIEE, KIPE, KITE, KIIEIE and IEEE.

Myung-Joong Youn was born in Seoul, Korea, on November 26, 1946. He received the B.S. degree from Seoul National University, Seoul, Korea, in 1970 and the M.S. and Ph.D. degrees in electrical engineering from the University of Missouri, Columbia, in 1974 and 1978, respectively. He was with the Air-Craft Equipment Division of General Electric Company, Erie, PA, where he was an Individual Contributor on aerospace electrical system engineering. Since1983, he has been a Professor at the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea. His research activities are in the areas of power electronics and control, which include the drive systems, rotating electrical machine design, and high-performance switching regulators. Dr. Youn is a senior member of IEEE, a member of IEE, KIEE, KIPE, and KITE.