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Improved Zero-Current-Switching (ZCS) PWM Switch Cell with Minimum Additional Conduction Losses

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ABSTRACT

This paper proposes a new zero-current switching (ZCS) pulse-width modulation (PWM) switch cell that has no additional conduction loss of the main switch. In this cell, the main switch and the auxiliary switch turn on and turn off under zero current condition. The diodes commutate softly and the reverse recovery problems are alleviated. The conduction loss and the current stress of the main switch are minimized, since the resonating current for the soft switching does not flow through the main switch. Based on the proposed ZCS PWM switch cell, a new family of DC to DC PWM converters is derived. The new family of ZCS PWM converters is suitable for the high power applications employing IGBTs. Among the new family of DC to DC PWM converters, a boost converter was taken as an example and has been analyzed. Design guidelines with a design example are described and verified by experimental results from the 2.5 kW prototype boost converter operating at 40kHz.

Key Words : zero current switching (ZCS), pulse width modulation (PWM)

1. Introduction

Recently, various kinds of soft switching techniques for the switching power converters have been proposed in order to satisfy the ever-increasing requirements for smaller size, lighter weight and higher efficiency. These techniques reduce the switching losses enabling high frequency operation and consequently reduce the overall system size. In general, the soft switching approaches can be classified into two groups; zero voltage switching (ZVS) approaches [1-3] and zero current switching (ZCS) approaches [4-11].

The ZVS approaches are more desirable for the majority carrier semiconductor devices such as MOSFET's, since the turn-on loss caused by the output capacitance is more dominant. While, the ZCS approaches are suitable for the minority carrier semiconductor devices such as IGBT's, since the turn-off loss is dominant due to the tail current.

These days, IGBT's are replacing MOSFET's for high voltage, high power applications, since IGBT's have higher voltage rating, higher power density, and lower cost compared to MOSFET's. In an effort to increase the switching frequency of IGBT's by reducing switching losses, several kinds of ZCS soft switching techniques have been proposed since the ZCS PWM switch cell was first proposed in[4]. In the approaches proposed in [4] and [5], ZCS of the active switches is achieved by using a resonant inductor in series with the main switch and a resonant capacitor in series with the auxiliary switch. The main drawbacks of the ZCS approaches are high current stress on the active switches and high voltage stress on the diodes. In the approaches proposed in [6, 7] and [8], the resonating current for ZCS flows only through the auxiliary circuit, thus the current stress of the main switch

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is eliminated. However, it presents two power diodes in the power transfer path, which increases conduction losses of the diodes. In the approach proposed in [9], the peak current through the main switch is substantially reduced by using an additional inductor. Unfortunately, this approach is not effective in reducing conduction loss of IGBT, since the on-voltage of IGBTs is almost independent of the current.

This paper proposes a novel ZCS PWM switch cell that improves the drawbacks of the previously proposed ZCS PWM converters. The proposed cell provides ZCS condition for both the main switches and the auxiliary switch. Since the circulating current for the soft switching flows only through the auxiliary circuit, the conduction loss and current stress of the main switch are minimized. A new family of DC to DC PWM converters based on the proposed ZCS PWM switch cell is proposed. These converters are suitable for the high power applications employing IGBT's. Among the new family of DC to DC PWM converters, a boost converter was taken as an example and has been analyzed. Design guidelines with a design example are described and verified by experimental results from the 2.5 kW prototype converter operating at 40kHz.

2. The Proposed ZCS PWM Switch Cell

Fig. 1 shows the proposed ZCS PWM switch cell. It consists of two switches S1 and S2, two diodes D_1 and D_2, one resonant inductor L_r , and one resonant capacitor C_r . S1 is the main switch through which the input current flows while, S2 is the auxiliary switch that handles only a small portion of the output power and is rated at a lower average current.

Fig. 2 shows the previous ZCS PWM switch cell proposed in [4, 5] and Fig. 3 compares the additional conduction losses of the previous ZCS switch cell and the proposed ZCS switch cell, with respect to a hard switching counterpart. As can be seen in Fig. 3, the proposed approach has about 30% reduction in the conduction losses compared to the previous approach. Fig. 4 shows the new family of ZCS PWM converters derived using the proposed cell.

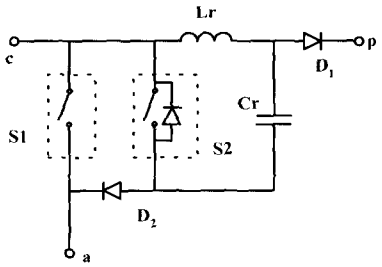

Fig. 1. The proposed ZCS PWM switch cell

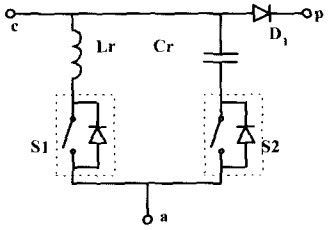

Fig. 2. The previous ZCS PWM switch cell [4,5]

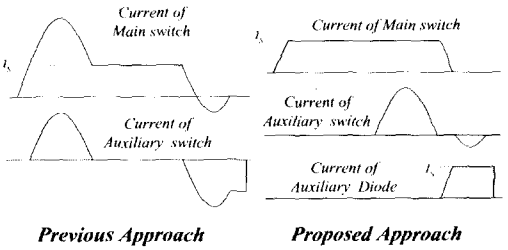

Fig. 3. Comparison of the additional conduction losses for ZCS

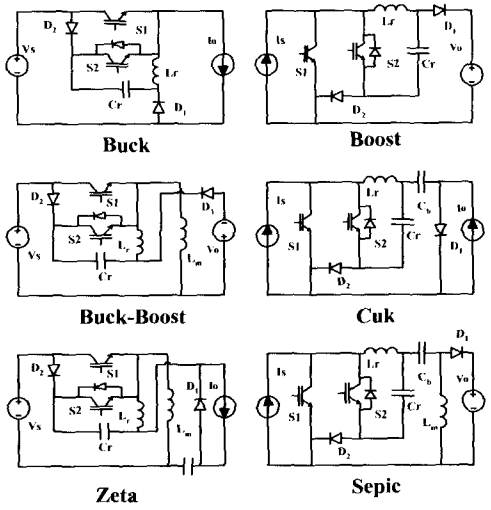

Fig. 4. New family of ZCS DC-to-DC PWM converters

3. Operation Principle

To explain the operation principle of the proposed cell, a boost converter was taken as an example. To analyze the steady state operation, it is assumed that all components and devices are ideal and the input inductor is large enough to be regarded as a constant current source during one operating cycle. The proposed converter has seven operation modes during one switching cycle. The key waveforms and the equivalent circuit of each operation mode are shown in Fig. 5 and 6, respectively.

Mode 1 (T_0-T_1): Prior to T_0, the input current I_s flows to the output through the ouput rectifier diode D1. At T_0, the main switch S1 turns on and the output voltage Vo is applied to the resonant inductor L_r. The current through S1 and L_r increases linearly until it reaches the input current I_s at T_1.

$$I_{S1}(t) = I_{Lr}(t) = \frac{Vo}{L_r}(t - T_0) \tag{1}$$

Mode 2 (T_1-T_2) : The input current flows through S1 and L_r. During this mode the ouput diode remains in the OFF state and the voltage of the resonant capacitor C_r is clamped at the output voltage Vo.

Mode 3 (T_2-T_3) : At T_2, the auxiliary swith turns on and C_r is discharged through the auxiliary switch S2 resonating with auxiliary resonant inductor L_r. This mode continues until V_{cr} reaches -Vo at T_3. The voltage of C_r and the current through the auxiliary switch are obtained as:

$$V_{cr}(t) = V_o \cos(w_r(t - T_2)) \tag{2}$$

$$I_{S2}(t) = \frac{V_o}{Z_r}\sin(w_r(t - T_2)) \tag{3}$$

where, $w_r = \frac{1}{\sqrt{L_r C_r}}$ and $Z_r = \sqrt{\frac{L_r}{C_r}}$

Mode 4 (T_3-T_4) : At T_3, the current through Lr change its direction and diode D2 begins to conduct. C_r is charged through D2 and S1 by the resoance with L_r. Even though there exists another charging path through the antiparallel diode of S2, Cr is charged only through D2, since the voltage drop of S1 counterbalances the voltage drop of D2 . The currents through the main switch and the auxiliary switch decrease, and this mode ends when the current through the main switch reaches zero. The voltage of Cr and the current of the main switch are obtained as:

$$V_{cr}(t) = -V_o \cos(w_r(t - T_3)) \tag{4}$$

$$I_{S1}(t) = I_s - \frac{V_o}{Z_r}\sin(w_r(t - T_3)) \tag{5}$$

Mode 5 (T_4-T_6) : At T_4, the current through S1 reaches zero and the anti-parallel diode of S2 begins to conduct. When the current through the antiparallel diode of S2 goes back to zero at T_6, this mode ends. When the current S2 reaches its negative peak value at T_5, the gate-drive signals for S1 and S2 are disabled at the same time and both the two switches are turned off with zero currents.

Mode 6 (T_6-T_7) : The input current flows through D2 charging Cr, and the voltage of Cr linearly increases until it reaches Vo at T_7.

Mode 7 (T_7-T_8) : When the voltage of Cr reaches Vo, D2 turns off and D1 begins to conduct at T_7. During this mode, the entire input current flows to the output through D1 and L_r. Since the voltage of Cr is clamped at Vo, D2 turns off with zero voltage.

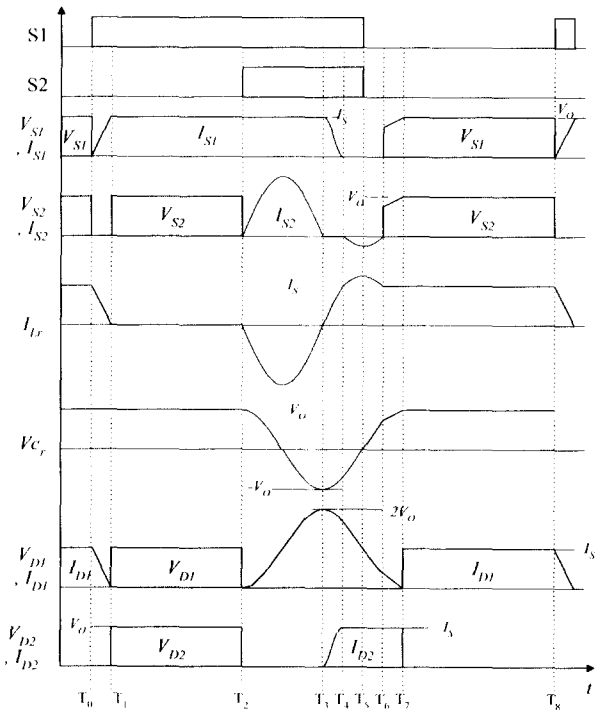

Fig. 5. Key waveforms of the new ZCS PWM Boost converter

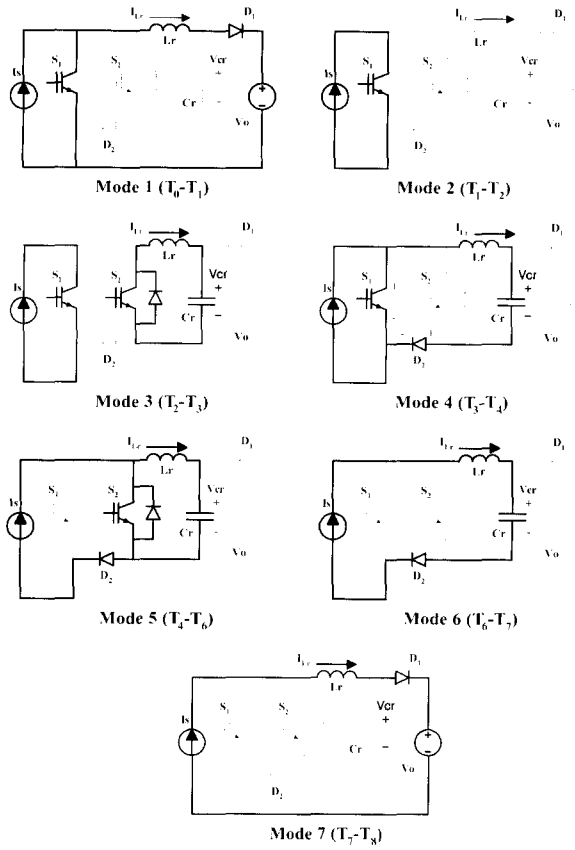

Fig. 6. Operation modes

4. Design Procedure and Example

In order to achieve zero current switching for the two switches, the following equations should be satisfied.

$$I_{Lf.peak}^{\max} < \frac{V_o}{Z_r} \tag{6}$$

$$D_{\max} T_s > \frac{T_r}{2} \tag{7}$$

where $T_r = 2\pi\sqrt{L_r C_r}$, $I_{Lf.peak} = \frac{P_o}{\eta V_s} + \frac{V_s}{L_f} DT_s$, η is the expected efficiency and Po is the output power.

As a rule of thumb, selection of the resonant period Tr as about five times of the fall time of the switching device, is known to be adequate. However, by increasing resonant inductor, the reverse recovery of the diode can be reduced. Lr and Cr should be determined by trade-off, therefore.

The additional conduction loss caused by the circulating current is obtained as:

$$Loss_{add} = \int_0^{Ts} |i_{cr}| dt \cdot fs \cdot V_{conduct} \cong 2V_o \cdot C_r \cdot fs \cdot (V_{CE.S2} + V_{F.D2}) \tag{8}$$

where i_{cr} is current of Cr, $V_{conduct}$ is the voltage drop of the semiconductor involved in the circulating current path, $V_{CE.S2}$ is the on state collector-emitter voltage of the auxiliary switch and $V_{F.D2}$ is the forward voltage of the diode D2. To make the ZCS effective in respect of efficiency, the additional conduction loss should be less than the reduced switching loss by soft-switching.

From (9), the reduction of the additional conduction loss compared to the previous approach of [4,5] can be approximated as:

$$Loss_{reduced} \cong 2V_o \cdot C_r \cdot fs \cdot V_{CE.S1} \tag{9}$$

The specifications of the boost example are as follows:

Vs=220V, Vo=400V, Po=2.5kW, fs=40kHz

From (6), $I_{LF.peak}^{\max}$ is 13A and V_o/Z_r is chosen as 20A considering safe ZCS operation.

The values of the resonant inductor and the resonant capacitor are determined as:

Lr=20μH, Cr=50nF

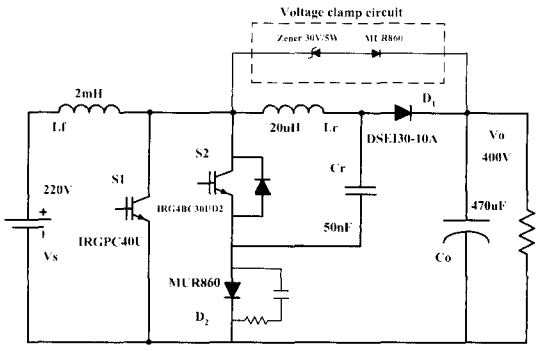

Fig. 7. Implemented circuit of the new ZCS PWM Boost converter

The power stage circuit is shown in Fig. 7 and the main parameters are summarized in Table I. To prevent ringing of the voltages of the main switches, a simple clamp circuit is used as shown by the dashed line in Fig. 7. The clamp circuit consists of a low voltage zener diode in series with the clamp diode. The voltages of the switches are clamped to a voltage slightly higher than the output voltage. As also shown in Fig. 7, an RC snubber is used to suppress the parasitic oscillation between the resonant inductor and the parasitic capacitance during the main switch turn-on transition.

5. Experimental Results

Fig. 8 and Fig. 9 show the current and voltage waveforms of the main switch and the auxiliary switch at full load, respectively. The main switch and the auxiliary switch turn on and turn off with zero currents.

Fig. 10 shows the current and voltage waveforms of the output diode at full load. The output diode turns off softly by the resonance inductor L_r and the reverse recovery is reduced.

Fig. 11 shows the efficiency curves versus output power with different approaches. The efficiencies were measured using Voltech power analyzer (PM3300). For a proper comparison, the resonant components of the previous ZCS approach are set at the same value with those of the proposed approach. The proposed approach shows better efficiency than the previous ZCS approach and the maximum efficiency is 97.6%. As the load level decreases, the efficiencies of the ZCS schemes drop, which is the common characteristic of the ZCS approaches. The reason is that the commutation energy is designed to meet the worst case requirement, i.e. heavy load condition, and it keeps constant, regardless of the load variation. In case of the previous ZCS scheme, the efficiency is lower than that of the hard switching scheme below 45% load. However, the proposed scheme has higher efficiency than the hard switching scheme down to the 30% load, since the additional conduction loss is minimized. Compared to the previous ZCS approach, the efficiency is improved by 0.3%, which amounts to about 7W. The calculated efficiency improvement is about 5W from (9).

Table 1. Utilized components and parameters

Compon	Parameters
Lf	PE22EC90-Z , 2mH
Lr	PQ2620, 20μH
Cr	50 nF ,polypropylene capacitor (600V)
Co	450V/ 470 μF, electrolytic capacitor
S1	IRGPC40U (600V, 20A)
S2	IRG4BC30UD2 (600V, 12A)
D1	DSEI30-10A(1000V, 30A)
D2	MUR860(600V, 8A)

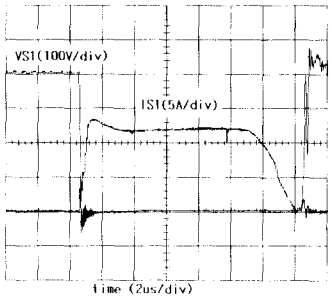

Fig. 8. Current and voltage waveforms of S1

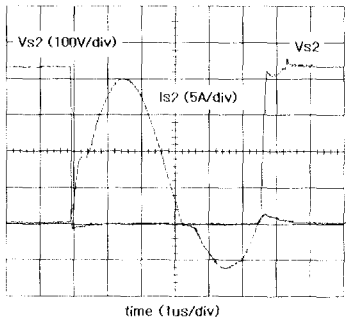

Fig. 9. Current and voltage waveforms of S2

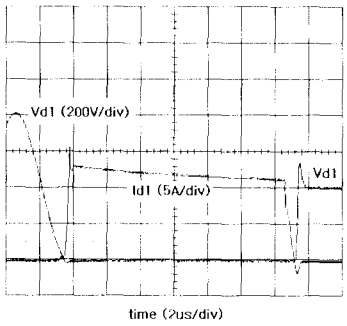

Fig. 10. Current and voltage waveform of D1

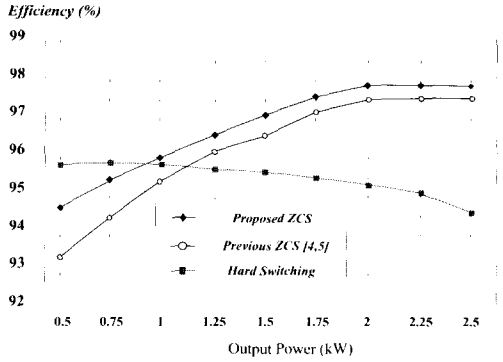

Fig. 11. Measured efficiency

6. Conclusion

This paper has presented a novel zero-current switching (ZCS) pulse-width modulation (PWM) switch cell minimizing the additional conduction loss for ZCS. The proposed cell provides zero current switching conditions for the main switch and the auxiliary switch. The diodes are softly commutated and the reverse recovery problems are alleviated. The conduction loss and current stress of the main switch are minimized since the resonating current flows only through the auxiliary circuit. Based on the proposed soft commutation cell, a new family of DC to DC PWM converters was derived. The new family of ZCS PWM converters is suitable for the high power applications employing IGBT's. A boost converter was taken as an example and has been analyzed. Design guidelines with a design example were illustrated. Experimental results from the 2.5 kW, 40kHz prototype ZCS boost converter employing IGBT's were presented and compared with that of hard-switching and previous ZCS schemes.

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