측면 전계 방출 소자를 위한 화학적-기계적 연마를 이용한 새로운 미소 간격 제작 기술

論 文
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A Novel Sub-Micron Gap Fabrication Technology using Chemical-Mechanical Polishing (CMP) for Lateral Field Emission Device (FED)

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(Choon-Sup Lee · Chul-Hi Han)

Abstract - We have developed a sub-micron gap fabrication technology using chemical-mechanical polishing (CMP) without /the sub-micron lithography equipments (0.18~0.25 μm). And it has been applied to a lateral field emission device (FED), in which narrow gap distance is very important for reducing turn-on voltage. As a result, the turn-on voltage (at which the current level is 1 nA) of the fabricated device with the gap distance of 256 nm is as low as 4.0 V, which is the lowest turn-on voltage among lateral FEDs ever reported.

Key Words : small gap, chemical-mechanical polishing (CMP), lateral FED, turn-on voltage

1. Introduction

Recently, a fabrication technology of narrow gap distance has been given many attentions in wide areas, for example, MEMS devices for increasing electrostatic force and sensitivity in a capacitive sensing method, and FEDs for reducing turn-on voltage [1-4]. However, it is difficult to deposit uniformly at the high aspect ratio layer. Thus, it suffers from the nonuniformity of the gap spacing along the side wall [1-2]. Also, it is very difficult to precisely align the sub-micron gap with electrostatic actuators. And it has nonlinear operation property [3-4]. In this paper, we have proposed a uniform sub-micron gap fabrication technology using chemical-mechanical polishing (CMP). Since dry or wet oxidation process determines the gap distance, it is relatively simple and easy to form uniform gaps with dimensions less than 1 μm compared with the sub-micron lithography (0.18~0.25 μm). And it does not require the sub-micron lithography equipments. Also, the distance of a few nanometer gaps can be fabricated. This process generates excellent uniformity and reproducibility in controlling the gap distance owing to the nature of oxidation.

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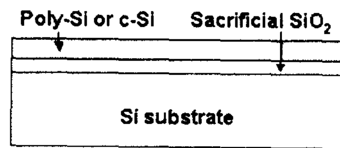
2. Sub-micron gap

The fabrication procedures of narrow gap are shown in Figure 1. Figure 1 (a) shows sacrificial oxide and poly-Si deposition. And lithography (#1 mask), RIE, and wet oxidation for defining a narrow gap are performed as shown in Figure 1 (b). Next, second poly-Si layer is deposited as shown in Figure 1 (c). For reducing dishing effect in CMP, the thickness of second poly-Si is about 2.5 times larger than that of first poly-Si. Then, CMP process and poly-Si patterning are performed as shown in Figure 1 (d). The CMP rate of poly-Si is about 50 nm/min. The CMP selectivity between poly-Si and the oxide is larger than 100:1. Thus, the polishing is self-stopped at the gap oxide. The dishing effect at the second poly-Si is reduced by the fill factor of about 90 % in mask layout. And the lift-off process is used for metallization as shown in Figure 1 (e) and (f). It protects the metal contamination on poly-Si tunneling tips. When gap and sacrificial oxide are etched, the narrow gap is formed as shown in Figure 1(f).

Figure 2 shows the fabrication results of the narrow gap using SOI wafer. The thickness of top c-Si is 3 μm. It replaces the first poly-Si with the single crystalline silicon. Thus, one side is c-Si, and the other side is poly-Si. The gap distance is about 200 nm and the length is the 300 μm. The uniformity of gap oxide thickness is about ±4 %. Figure 3 shows the gap distance versus oxidation time at a fixed temperature of 950°C in a steam ambient. The gap distance is measured with SEM view.

The oxidation time can control the gap distance. The oxidation temperature can also control the gap distance. Owing to the nature of oxidation, this process generates excellent uniformity and reproducibility in controlling the gap distance. If the oxidation is performed in the dry ambient, the gap distance of a few nanometer gaps can be obtained.



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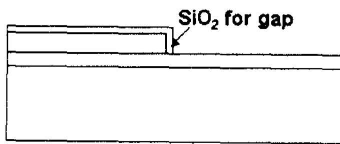

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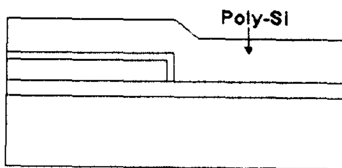

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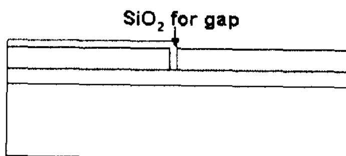

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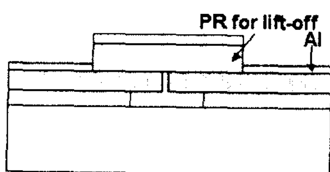

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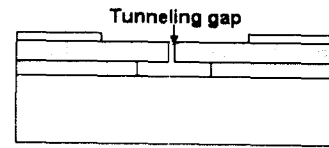
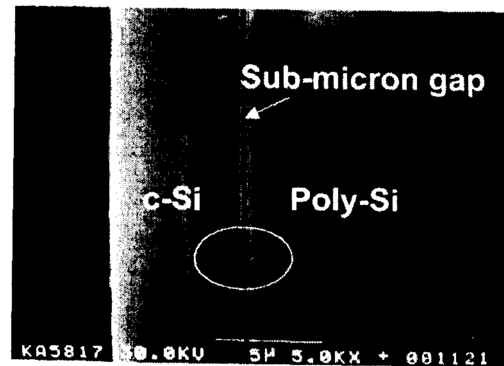


(f)

Figure 1. Fabrication procedures (a) Sacrificial oxide deposition, poly-Si deposition, and phosphorus diffusion (b) photolithography (#1 Mask), RIE, ando xidation for defining a narrow gap. (c) Second poly-Si deposition. (d) CMP process, phosphorus diffusion, and poly-Si patterning (#2 Mask) (e) PR patterning for lift-off process and Al sputtering (f) PR strip and sacrificial and gap oxides etching.



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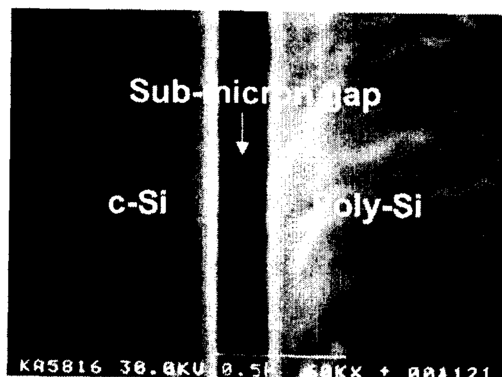


(b)

Figure 2. Fabrication results of narrow gap. (a) It shows the part of total length 300 μm. (b) Enlarged view. The gap distance of 200 nm is very uniform.

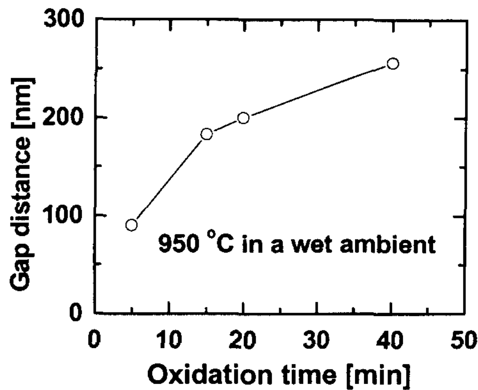
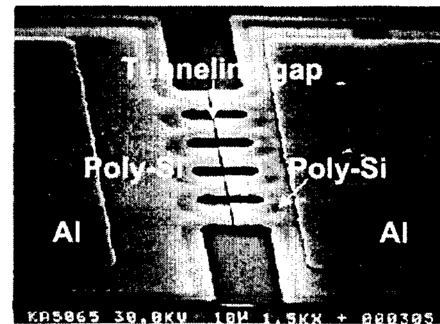


Figure 3. Gap distances versus oxidation time. The gap distance can be easily controlled by oxidation process.

3. Application to lateral FED

The sub-micron gap fabrication technology has been applied to the lateral field emission device (FED) [5]. In the FEDs, the narrow gap distance is very important for reducing the turn-on voltage [6]. For reducing the turn-on voltage, lateral FED are typically made by tensile stress induced at the initially connected slim poly-Si pattern or electrical stress at the PdO film for surface-conduction electron emitters (SCEs) [7-8]. However, these methods suffer from the nonuniformity of the gap due to the uses of thermal or electrical stress. But the sub-micron gap, which is formed by oxidation and CMP process, is very uniform. And it can be also controlled. Figure 4 shows the SEM view of the fabricated lateral FED. The width and length of the emitters are 10 μm and 10 μm, respectively. The gap distance is about 256 nm. As shown in Figure 4 (b), the grain size of poly-Si is about 50 nm. Owing to the nature of the poly-Si, the edge of the gap is rough. Thus, tunneling may be occurrd at the sharp point of poly-Si.

Electrical measurements are performed in a vacuum probing station at the pressure of $1x10^{-5}$ Torr. For the desorption of the contaminant, constant current annealing is performed before electrical measurements. And then, I-V characteristics are measured as shown in Figure 5. The turn-on voltage is as low as 4.0 V. Turn-on voltage is defined as the voltage at which the current level is 1 nA. And the emission current is measured very high about 1.5 μA at the voltage of 15 V. I-V characteristics of both forward and reverse bias voltages are similar behavior because of the symmetrical geometry. The combined effects of narrow tunneling gap and surface roughness of poly-Si grain are responsible for the low turn-on voltage and high emission current. Figure 6 shows the Fowler-Nordheim (F-N) plots of both forward and reverse bias voltage. In the F-N plot, the good linearity clearly shows the confirmation of the field emission. We assume the work function of the poly-Si emitter is 4.05 eV. The field enhancement factor (β) for the tips is first obtained by the slope of the FN plot. And effective emitting area (α) is obtained by the field enhancement factor and the intersection between the extrapolated line and y-axis [6]. The field enhancement factors (β) and the emission areas (α) are estimated from the F-N plot. The field enhancement factor is large because of the poly-Si grain. As shown in Figure 7, the turn-on voltage varies with respect to the gap distance. As the gap distance decreases, the turn-on voltage reduces. And Figure 8 shows the SEM view of the poly-Si emitter after multiple failure events. Because it has five wedge-shaped combs, it has multiple emission sites. And because the electric field at the corner is larger than that at the edge, failure events often occur at the corner. This failure event may be due to the tip melting or local arcing [6].



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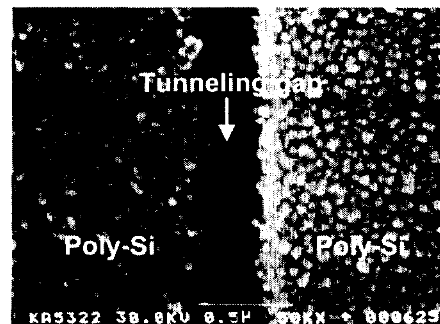


(b)

Figure 4. Fabrication results of lateral FED (a) It has five comb fingers. (b) The gap distance is about 256 nm.

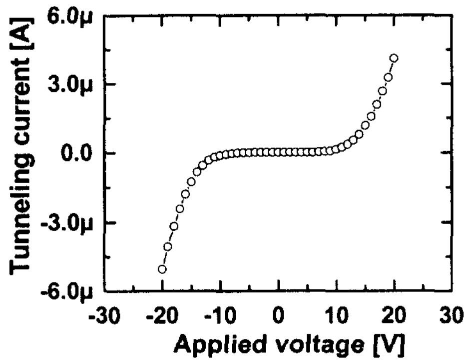
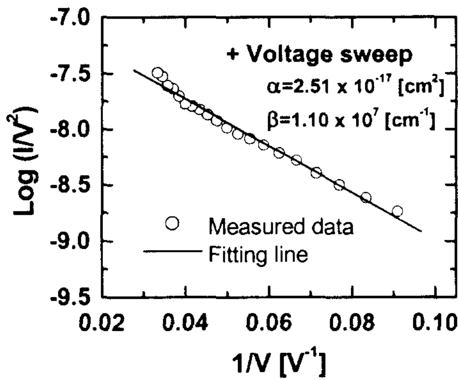


Figure 5. I-V characteristic of FED with 256 nm distance. The turn-on voltage (@ 1nA) is about 4.0 V.



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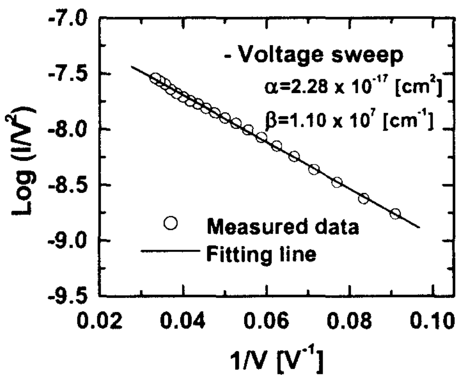

(b)

Figure 6. Fowler-Nordheim plot of above results. (a) Positive voltage sweep. (b) Negative voltage sweep.

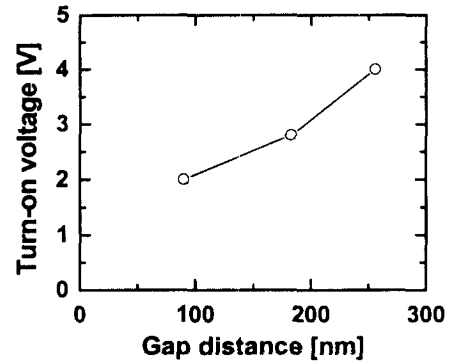

Figure 7. Turn-on voltage versus gap distance.

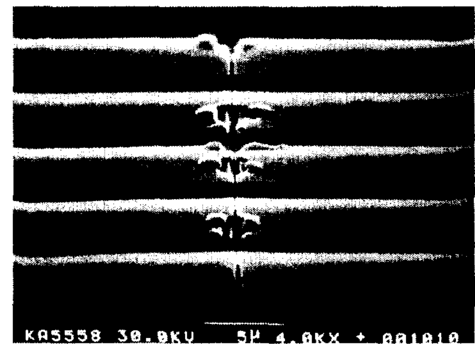

Figure 8. SEM microphotograph of polysilicon emitter tips after multiple failure events.

4. Conclusions

In conclusion, we have developed a sub-micron gap fabrication technology using CMP. And it has been applied to lateral FED. As a result, the low turn-on voltage of 4 V and high emission current of 1.5 μA at the voltage of 15 V have been obtained. The sub-micron gap fabrication technology, which does not required the sub-micron lithography equipments, may be applicable to many MEMS devices.

감사의 글

FED 측정에 많은 도움을 주신 서울대학교 이종덕 교수님, 오창우, 진성훈, 양기동에게 감사를 드립니다.

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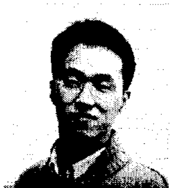
저 자 소 개



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