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탭-인덕터와 스너버-커패시터를 적용한 3 Level 영전압·영전류 스위칭 DC/DC 컨버터

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A Three Level ZVZCS Phase-Shifted DC/DC Converter Using A Tapped Inductor And A Snubber Capacitor

Eun-Soo Kim, Yoon-Ho Kim

요 약

종래의 위상전이 영전압 스위칭 풀-브리지 DC/DC 컨버터와 비슷하게 영전압 스위칭 3레벨 DC/DC 컨버터의 동작 모드 및 파형에서도 순환모드 구간동안 흐르는 순환전류에 따라 스위칭소자 및 변압기에서의 도통손실이 증가하는 단점을 갖고 있다. 따라서, 본 논문에서는 스위칭전원의 효율개선 및 스위칭 주파수를 증가시키기 위한 보다 개선되고, 진보된 탭인덕터와 스너버 캐패시터/다이오드로 구성된 2차 측 보조회로 적용 영전압·영전류 스위칭 3 레벨(Level) DC/DC 컨버터에 대한 주 회로특성분석 및 7kW, 30kHz DC/DC 컨버터의 시제품을 제작하여 실험한 결과에 대해 서술하고자 한다.

ABSTRACT

The conventional three-level high frequency phase-shifted dc/dc converter has a disadvantage that a circulating current flows through transformer and switching devices during the freewheeling interval. Due to this circulating current and RMS current stress, conduction losses of transformer and switching devices increases. To alleviate these problems, we propose an improved three-level Zero Voltage and Zero Current Switching (ZVZCS) dc/dc converter using a tapped inductor, a snubber capacitor and two snubber diodes attached at the secondary side of transformer. The proposed ZVZCS converter is verified on a 7kW, 30kHz experimental prototype.

Key Words : ZVZCS DC/DC Converter, Phase-shifted ZVS FB DC/DC Converter, Snubber Circuit

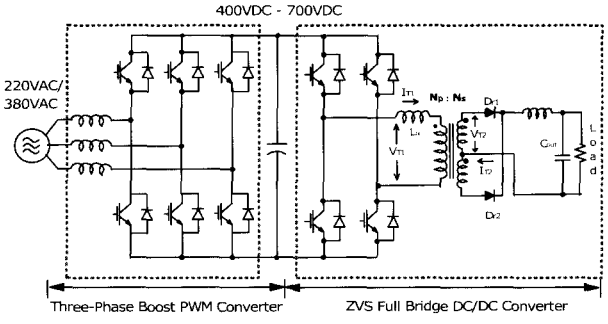
1. Introduction

Recently, to improve the input power factor in the utility side, a three-phase ac/dc boost converter has been used. However, in that scheme, the output voltage of the three-phase ac/dc boost converter increases with respect to the input voltage in the utility side. In turn this increment of output voltage in ac/dc boost converter raises the voltage stress across the primary switching devices of ZVS full bridge (FB) dc/dc converter as shown in Fig. 1(a).

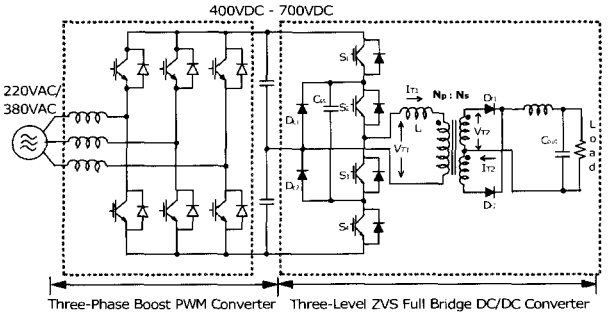
Therefore, to cope with the increased output voltage of ac/dc boost converter, the three-level ZVS phase-shifted dc/dc converters were presented in reference[1][2]. By using the three-level ZVS phase-shifted dc/dc converter, voltage stress across the primary switching devices is reduced to the half of input voltage as shown in Fig. 1(b). However, the conventional three-level ZVS phase-shifted dc/dc converter has a disadvantage that the primary circulating current that is the reflected output current nI_o flows through the transformer and

switching devices during the freewheeling interval.

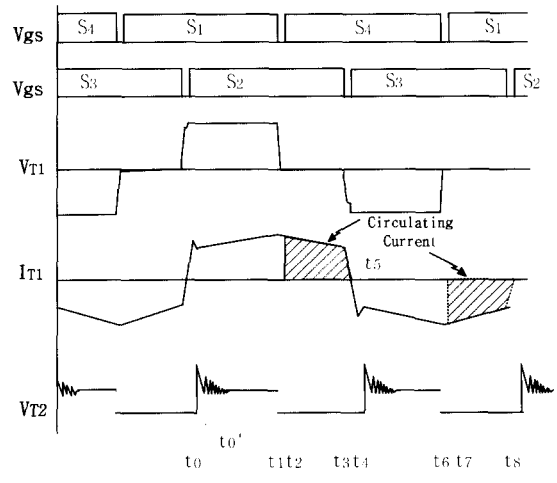
To alleviate this problem, ZVZCS dc/dc converters using a simple auxiliary circuit have been presented [2][3][4][5]. But, the use of the simple auxiliary circuit to reduce the circulating current has disadvantages such as the use of active switches, an over-voltage and severe parasitic ringing in the secondary side of the ZVZCS dc/dc converter.



(a) ZVS FB dc/dc converter



(b) Three-level ZVS dc/dc converter



(c) Operation waveforms

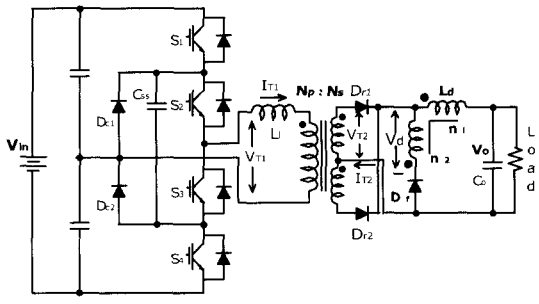
Fig. 1 The ZVS dc/dc converter and its waveforms

This paper proposes an improved three-level ZVZCS phase shifted dc/dc converter using a tapped inductor, a snubber capacitor and two snubber diodes attached at the secondary side of the transformer. By using a tapped inductor and a snubber capacitor, the proposed converter can reduce the primary circulating current flowing through switching devices during the freewheeling interval.

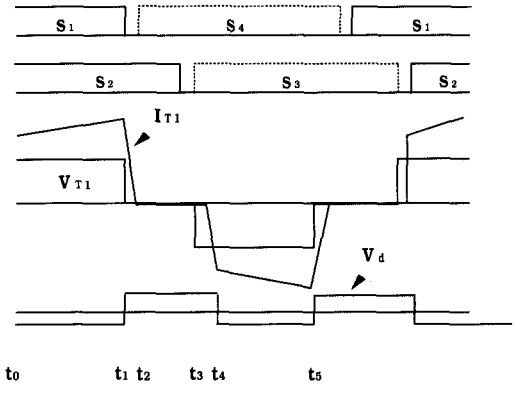
The converter also can reduce the reverse recovery loss, a parasitic ringing and voltage stress in the secondary rectification diodes.

2. Review of ZVZCS DC/DC Converters with Simple Auxiliary Circuits

2.1 The ZVZCS dc/dc converter with a tapped inductor[3]



(a) ZVZCS converter using the tapped inductor



(b) Operation waveforms

Fig. 2 Three-level ZVZCS dc/dc converter with a tapped inductor and its waveforms

To reset the circulating current during the freewheeling interval as shown in Fig. 2, the three-level ZVZCS phase-shifted dc/dc converter with a tapped inductor can be used. During the

conduction interval (t_0-t_1), switching devices S_1, S_2 are turn-on and the input energy is transferred from the input source to the output load.

And then, when the switching device S_1 is turn-off and S_4 is turn-on, the freewheeling interval is started and the secondary current of transformer continues flowing through the rectifier diode D_{f1} and the output filter inductor L_o. Also, the primary current I_{T1} flows through S_2, transformer and D_{c1}.

At this time, unlike the use of the untapped inductor, the freewheeling diode D_f conducts in this interval and the freewheeling current is flowing through the n_2, n_1 of the tapped inductor and output filter capacitor C_o.

Due to the reverse blocking voltage (V_d) of a tapped inductor during the freewheeling interval (t_1-t_3), the secondary rectifier diodes D_{f1}, D_{f2} are biased in reverse and the secondary windings of transformer are opened. Therefore, both transformer primary and secondary currents become zero during the freewheeling interval (t_1-t_3). However, in order to decrease the primary current to zero rapidly, this topology requires increasing the turns-ratio of the tapped inductor.

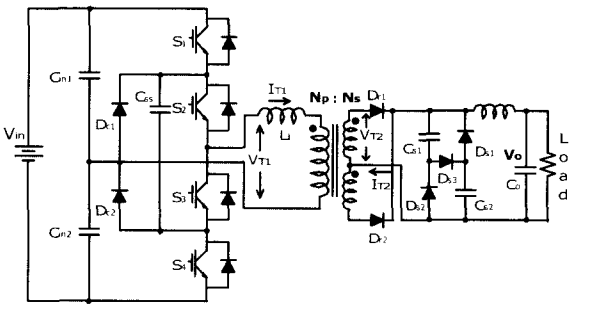
In this case, this circuit has disadvantages such as the increase of the voltage stress and parasitic ringing at the freewheeling and rectification diodes.

Therefore, the saturable reactors connected in series with the secondary windings have to be used to reduce the parasitic ringing. The use of the saturable reactor produces an additional loss and heat in the saturable core. For these reasons, it is suited only for medium power applications.

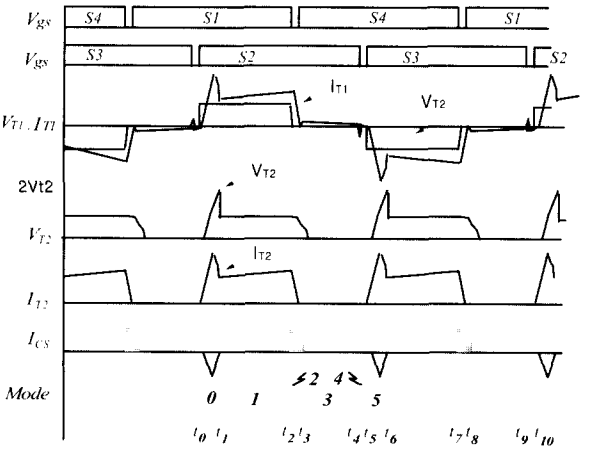
2.2 The ZVZCS dc/dc converter with an energy recovery snubber (ERS)[4]

By using an energy recovery snubber instead of adding a tapped inductor to reduce RMS current stress such as described in reference[4][5], the converter can reduce the circulating current flowing through the transformer and switching devices during the freewheeling interval (t_2-t_4, t_7-t_9). As shown in Fig. 3, the energy stored in the snubber capacitors C_{s1}, C_{s2} during the conduction interval (t_0-t_2, t_5-t_7) starts discharging when the transformer secondary voltage in the freewheeling interval becomes zero. Due to the discharging of the snubber capacitors C_{s1}, C_{s2}, the rectification diodes D_{f1} and D_{f2} are biased in reverse and the secondary windings of the transformer are opened. Therefore, both primary and secondary currents of the transformer become zero.

Thus, the RMS currents for the transformer and switches are considerably reduced in the freewheeling interval (t_2-t_4, t_7-t_9). However, in this case, during the transition from off stage to active stage, the serial resonance circuit is formed with the leakage inductance of the transformer and the snubber capacitors (C_{s1}, C_{s2}), and the secondary current I_{T1}/n begins to flow to C_{s1}, D_{s3} and C_{s2} through the transformer and the secondary rectification diodes. During the charging process, snubber capacitors (C_{s1}, C_{s2}) are charged up to the secondary voltage (V_{T2}) of the transformer, respectively.



(a) ZVZCS dc/dc converter using an energy recovery snubber(ERS)



(b) Operation waveforms

Fig. 3 Three-level ZVZCS dc/dc converter using an energy recovery snubber and its waveforms

As a result, over-voltage ($2V_{T2}$) on the secondary occurs. Due to the relatively high impedance of the

resonance tank, the snubbing or clamping effect for the secondary transient voltage are also lost. Also, the energy to reset the primary leakage current of the transformer is dependent on the charging energy of the snubber capacitors C_{s1}, C_{s2}. At the light and medium load, the ZVZCS characteristics easily can be achieved. However, the ZVZCS characteristics can be lost at the heavy load.

3. The Proposed ZVZCS DC/DC Converters Using a Tapped Inductor and a Snubber Capacitor

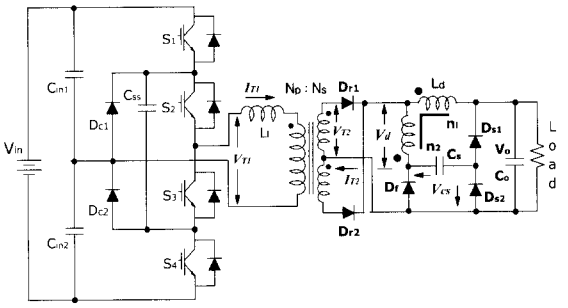
Fig. 4 (a) and Fig. 6 show the proposed ZVZCS phase-shifted dc/dc converters that employs a tapped inductor and a snubber capacitor to minimize the circulating current and the secondary transient over-voltage. The operating mechanism and circuit configuration of the proposed converter are similar to the ZVZCS dc/dc converter using a tapped inductor except that the snubber capacitor C_s and snubber diodes D_{s1}, D_{s2} are inserted.

The proposed converter operation with respect to switching transitions is briefly described as follows. During the conduction interval (t_0-t_3), the switches S_1, S_2 are turned-on and the converter is transferring the input power to the transformer secondary. When the secondary current reaches the output current, the voltage polarity of the tapped inductor is changed. Therefore, during the time interval (t_1-t_2), the serial resonance circuit is formed with the leakage inductance of the transformer and the tapped inductor and the capacitance of the snubber capacitor, and the small charging current begins to flow to Ld_n2, C_s, D_{s1} and load through the transformer and the rectification diode D_{r1}. During the charging process interval (t_1-t_2), the snubber capacitor voltage V_{cs} is charged up to the double tapped inductor voltage ($V_{cs}(t) = 2V_d$, $n_1 = n_2$).

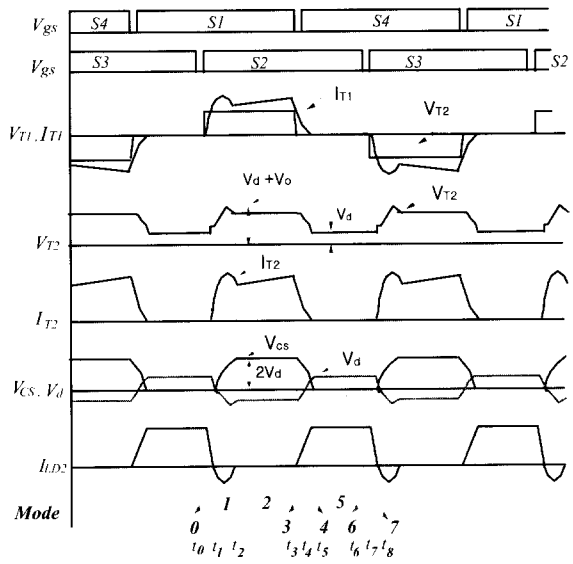
At this time, the secondary voltage V_{t2} of the transformer is the sum of the reverse blocking voltage (V_d) of the tapped inductor, the snubber capacitor voltage ($V_{cs}(t) = 2V_d$) and the output voltage (V_o).

Therefore, the proposed ZVZCS dc/dc converter can clamp the secondary transient over-voltage to the voltage of ($V_d + V_o$). Also, in the proposed converter, the available voltage sources to reset the primary leakage current of the transformer during the freewheeling interval (t_3-t_6) are the tapped inductor voltage ($V_d(t) = V_o/2$, $n_1 = n_2$) and the snubber capacitor Voltage (V_{cs}).

Therefore, the ZVZCS concept can be implemented easily in the proposed ZVZCS three-level dc/dc converter than others. Also, by increasing the turns-ratio of the tapped inductor, the ZVZCS condition can be expanded into the heavy load without voltage stresses and ringing. The proposed snubber adopted in this study recovers the switching losses to the load.



(a) The proposed ZVZCS DC/DC converter using the clamp circuit 1



(b) Operation waveforms

Fig. 4 The proposed three-level ZVZCS DC/DC converter using the clamp circuit 1 and its waveforms

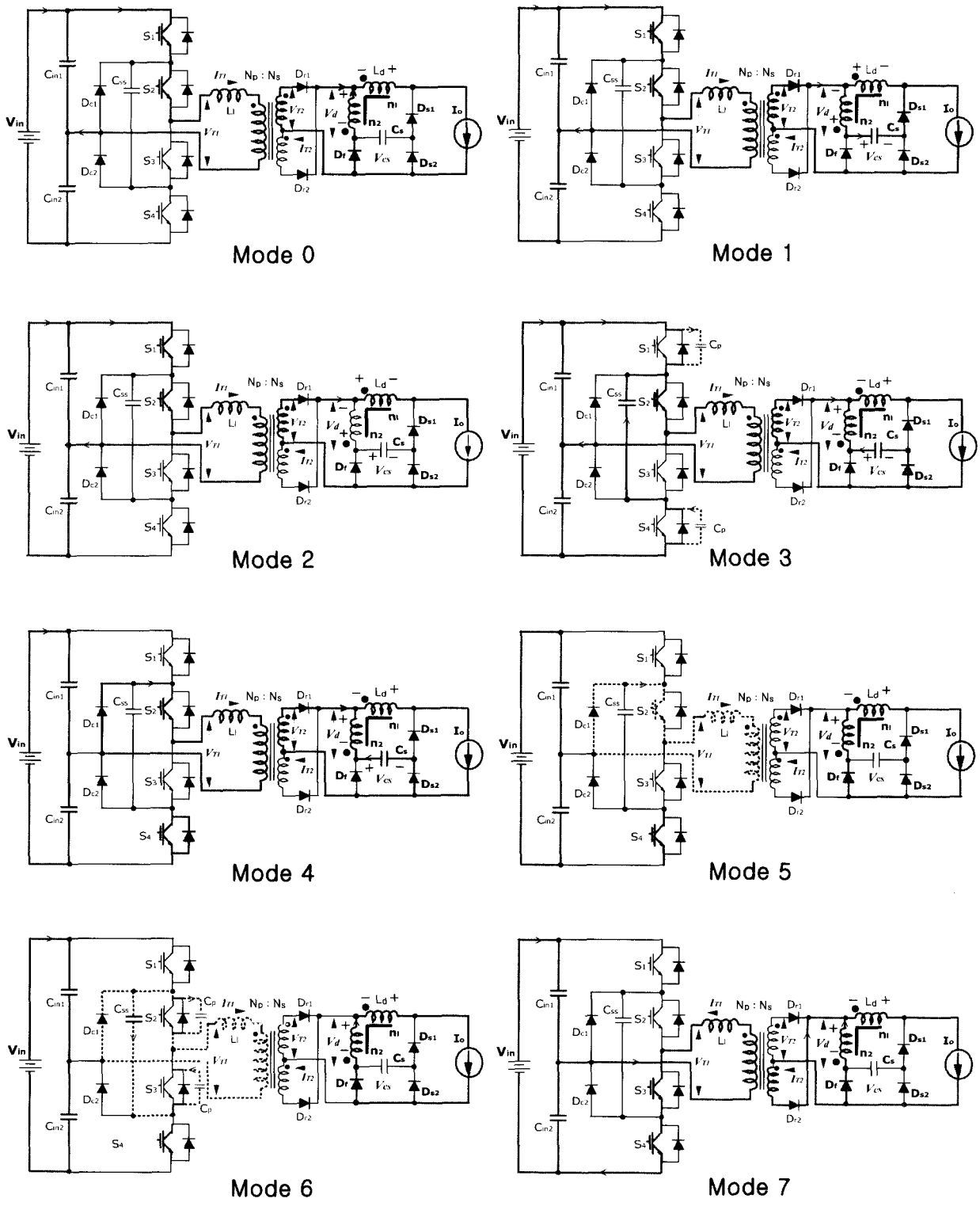


Fig. 5 Circuit configuration for operating mode in ZVZCS dc/dc converter using the clamp circuit 1

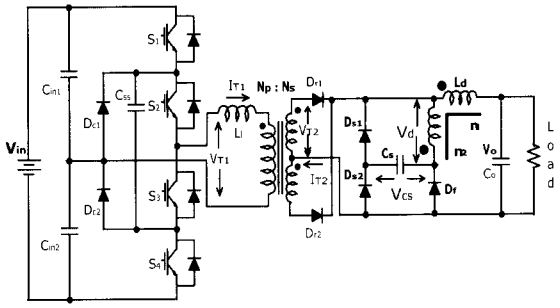


Fig. 6 The proposed three-level ZVZCS DC/DC converter using the clamp circuit 2

4. Experimental Results

A 7kW(110VDC, 65A), 30kHz IGBT based experimental circuit has been implemented to verify the operation of the proposed ZVZCS three-level dc/dc converter.

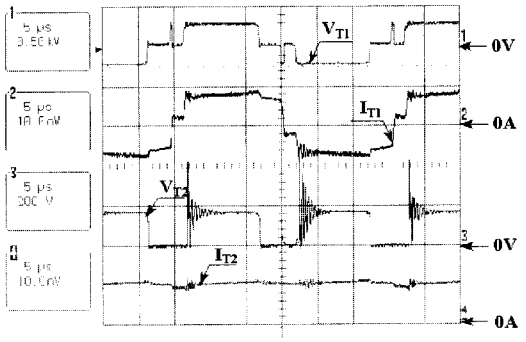
The specifications of the experimental circuit are as follows:

* DC Input voltage: 540VDC
* Output voltage and current: 110VDC, 65A,
* Switching frequency: 30kHz

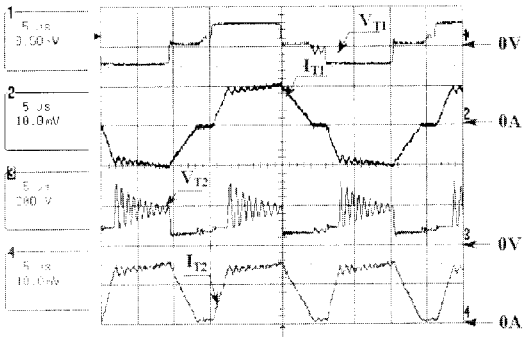
The parameters of the circuit are as follows.

* S_1 - S_4 : IGBT(2MBI120L060, 600V, 200A)
* D_{c1}, D_{c2} : Circulating diodes
* L_m : 286uH (Magnetizing inductance)
* L_l : 3.5uH (Leakage inductance of transformer)
* n : Transformer turns ratio (n=Ns/Np=6/8=0.75)
* C_s : 0.1uF (Snubber capacitor)
* C_p : 14nF (Stray capacitance of IGBT)
* D_{s1}, D_{s2} : Snubber diode
* D_{r1}, D_{r2}, D_f : Secondary diodes and freewheeling diode, 600V, 100A, trr:150ns
* L_d:500uH (n_1=n_2)
* Co:4,700uF
* t:1.3us (Dead time)

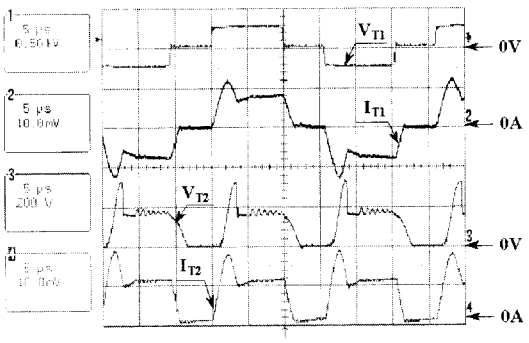
Fig. 7 (a), (b) and (c) show the voltage and current waveforms of the primary and secondary side of the transformer in the three-level phase-shifted ZVS dc/dc converter and ZVZCS dc/dc converters with an auxiliary circuit, respectively. Comparing Fig. 7(a) with Fig. 7(b) and Fig. 7(c), it can be seen that by using the tapped inductor and the energy recovery snubber in



(a) Voltage and current waveforms of the primary and secondary of the transformer in the three-level ZVS dc/dc converter



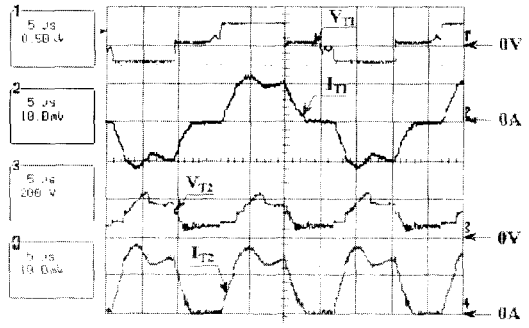
(b) Voltage and current waveforms of the primary and secondary of the transformer in the three-level ZVZCS dc/dc converter using the tapped inductor [n_1=n_2]



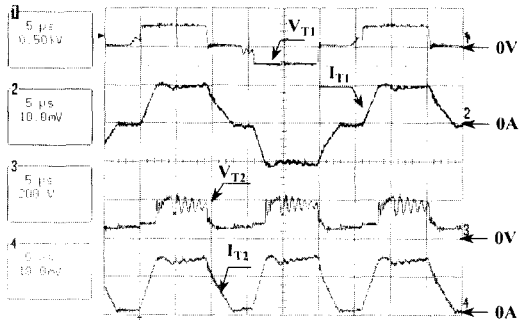
(c) Voltage and current waveforms of the primary and secondary of the transformer in the three-level ZVZCS dc/dc converter using an energy recovery snubber (ERS) [C_{s1} = C_{s2} = 0.3uF]

Fig. 7 Experimental waveforms of three-level dc/dc converters Input voltage : 540VDC, the output: 110V, 56A]
(500V/div, 50A/div, 200V/div, 50A/div, 5us/div)

three-level dc/dc converter, the primary circulating current decreases nearly to zero during the freewheeling interval. However, it can be seen that the parasitic ringing and the transient over-voltage are produced in the secondary rectification diodes of the converter.



(a) Voltage and current waveforms of the proposed ZVZCS dc/dc converter using the clamp circuit 1 [n_1=n_2, C_s=0.1uF]



(b) Voltage and current waveforms of the proposed ZVZCS dc/dc converter using the clamp circuit 2 [n_1=n_2, C_s=0.1uF]

Fig. 8 Experimental waveforms of the proposed ZVZCS three-level dc/dc converters
[Input voltage: 540VDC, the output: 110V, 56A]
(500V/div, 50A/div, 200V/div, 50A/div, 5us/div)

By using the clamp circuit, which is consisted of a tapped inductor, a snubber capacitor and two snubber diodes as shown in Fig. 4(a) and Fig. 6, we can see that the proposed converters can reduce the circulating current flowing through switching devices during the freewheeling interval, and also the voltage stress and ringing are reduced in the secondary rectification diodes according to the reverse voltage of the tapped inductor and the charging voltage of the snubber capacitor.

Fig. 9 shows the measured efficiency of the proposed three-level ZVZCS dc/dc converters in comparison with the other ZVZCS dc/dc converters using an auxiliary circuit, respectively. The efficiency of ZVZCS dc/dc converter using the tapped inductor shown in Fig. 2 is similar to the efficiency characteristics of the proposed ZVZCS dc/dc converter shown in Fig. 4(a) and Fig. 6.

However, ZVZCS dc/dc converter using the tapped inductor produces the voltage stress and ringing in the secondary rectification diodes due to the resonance of the transformer leakage inductance and the stray capacitance of the freewheeling diode (D_f).

The efficiency of the ZVZCS dc/dc converter using an energy recovery snubber shows especially the low efficiency characteristics in the light load (below 20A) even though the circulating current is reduced during the freewheeling interval. It shows the reduced efficiency characteristics in the light load according to the charging current flowing through the snubber capacitors (0.3uF) and snubber diodes.

The efficiency of the proposed ZVZCS dc/dc converters shows the high efficiency characteristics from the light load to the heavy load, and shows some improvement (2% - 4%) over the conventional ZVS dc/dc converter due to the reduced charging current and circulating current. The highest efficiency is 96.5% at 15A and the efficiency at the full load (58A) is 94%. Also, by increasing the turns-ratio of the tapped inductor, the proposed ZVZCS condition can be extended to the heavy load without voltage stresses and ringing.

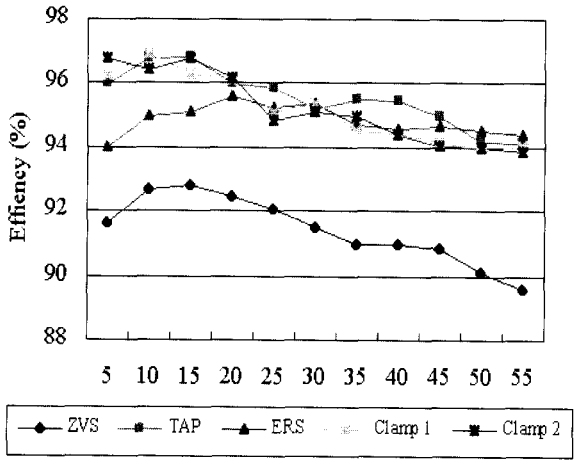


Fig. 9 The efficiency characteristics

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