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Effect of Dopants on Cobalt Silicidation Behavior at Metal-oxide-semiconductor Field-effect Transistor Sidewall Spacer Edge

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ABSTRACT

Cobalt silicidation at sidewall spacer edge of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) with post annealing treatment for capacitor forming process has been investigated as a function of dopant species. Cobalt silicidation of nMOSFET with n-type Lightly Doped Drain (LDD) and pMOSFET with p-type LDD produces a well-developed cobalt silicide with its lateral growth underneath the sidewall spacer. In case of pMOSFET with n-type LDD, however, a void is formed at the sidewall spacer edge with no lateral growth of cobalt silicide. The void formation seems to be due to a retarded silicidation process at the LDD region during the first Rapid Thermal Annealing (RTA) for the reaction of Co with Si, resulting in cobalt monosilicide at the LDD region. The subsequent second RTA converts the cobalt monosilicide into cobalt disilicide with the consumption of Si atoms from the Si substrate, producing the void at the sidewall spacer edge in the Si region. The void formed at the sidewall spacer edge serves as a resistance in the current-voltage characteristics of the pMOSFET device.

Key words : Cobalt silicidation, Void, Lightly doped drain (LDD), Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

1. Introduction

Titanium silicide ($TiSi_2$) and cobalt silicide ($CoSi_2$) have been employed as gate electrode materials in silicon-based very large-scale integration (VLSI) circuits, as a consequence of their low electrical resistivities and good process compatibilities.[1,2] $TiSi_2$, however, suffers from high electrical resistivity for sub-0.25 micron generations due to the difficulty of phase transition from high resistivity C-49 phase to low resistivity C-54 phase during the second Rapid Thermal Annealing (RTA) of the two-step RTA process.[3] Meanwhile, since $CoSi_2$ could maintain its low resistivity on much narrower lines, it has been employed as gate electrode material by several companies targeting for their sub-0.25 micron technology generations.[4]

The merge of DRAM (Dynamic Random Access Memory) and logic also requires application of cobalt silicidation on the source/drain region to implement lower power consumption and higher performance in a single chip, and its thermal stability to endure the subsequent high temperature capacitor forming process. However, it has been reported that cobalt silicidation induced a void formation at the edge of the oxide pattern causing a serious junction leakage.[5] We also reported cobalt silicidation-induced void defect formation at the sidewall spacer edge of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs).[6] Recent study indicated that the cobalt silicidation through reaction between Co and Si substrate was affected by the dopant species implanted into the Si substrate. Literature survey also indicated that n-type dopant species retarded the cobalt silicidation process.[7] Typical MOSFET structure employs Lightly Doped Drain (LDD) that forms a lightly doped region under sidewall spacer so that channel region is connected to drain region with a reduced electric field intensity to improve hot carrier effect. Pocket structure, on the other hand, forms an opposite-type dopant region under the sidewall spacer to reduce short channel effect. Since MOSFET devices use these different LDD structures in a single chip, it is very important to understand the effect of dopant species on the cobalt silicidation behavior at the MOSFET sidewall spacer edge. In this study, various combinations of dopant species were employed to fabricate several different dopant distributions in Si substrate, and to investigate the effect of dopant species on the cobalt silicidation behavior at the sidewall spacer edge of MOSFETs.

2. Experimental

The substrates used in this study were p-type Si (001) wafers with electrical resistivity of 9-12 ohmcm. Phospho-

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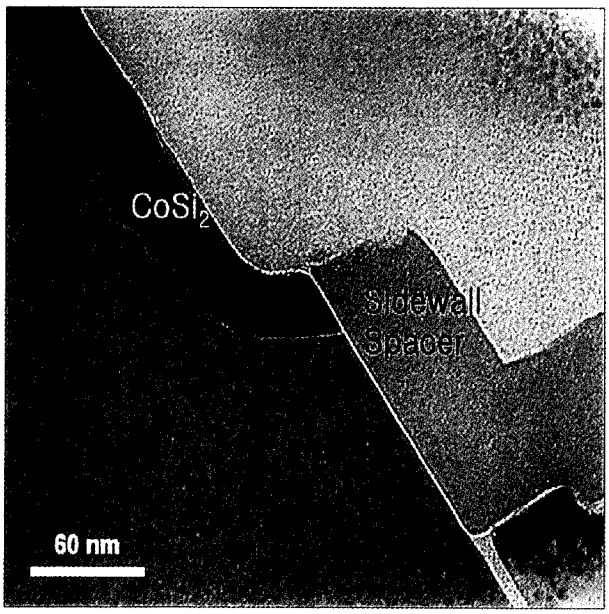
Table 1. Ion-implantation Conditions for Fabrications of MOSFET Devices

Process Condition \ Sample	1	2	3	4
n-well				
p-well				
p V_T Ion Implantation				
n V_T Ion Implantation				
Gate Formation				
P (10^{13}) Blank Ion Implantation				
As (10^{14}) LDD Ion Implantation				
B LDD Ion Implantation		10^{13}		10^{14}
Oxide/Nitride Deposition				
As (10^{15}) S/D Ion Implantation				
B (10^{15}) S/D Ion Implantation				

rus (P) and boron (B) were ion-implanted to form n and p-well in the substrate after Shallow Trench Isolation (STI). Appropriate n and p-type dopant ion implantations for threshold voltage control of MOSFET devices were conducted in n and p-channel regions, respectively. After gate etch process, reoxidation and LDD ion implantation were performed. LDD ion-implantation conditions were split to prepare four different samples, as shown in Table 1. P blank ion implantation was conducted on samples 1, 3 and 4 with dose of 10^{13} /cm^2. Sample 1 was arsenic (As) ion-implanted on the wafer for n-type LDD and n-type source/drain with doses of 10^{14} /cm^2 and 10^{15} /cm^2, respectively, resulting in nMOSFET with n-type LDD. Sample 2 was B ion-implanted on the wafer for p-type LDD and p-type source/drain with doses of 10^{13} /cm^2 and 10^{15} /cm^2, respectively, resulting in pMOSFET with p-type LDD. Sample 3 was prepared as pMOSFET, but with n-type LDD and p-type source/drain with doses of 10^{13} /cm^2 and 10^{15} /cm^2, while sample 4 as pMOSFET with counter-doped LDD and p-type source/drain with doses of 10^{14} /cm^2 and 10^{15} /cm^2. The counter-doped LDD was achieved by counter-doping the n-type LDD of sample 3 (P 10^{13}/cm^2) with p-type dopant (B 10^{14}/cm^2).

RTA process was performed to activate the implanted dopants. The samples were dipped in a diluted HF solution prior to cobalt (Co) film deposition to remove native oxide. Co film with titanium capping layer was sputter deposited without breaking vacuum in a DC magnetron sputtering system.[8] Subsequent RTA was carried out at 600°C for 60 sec in an N_2 ambient (first RTA). Unreacted metals were then removed in metal etchant solutions. Additional annealing was performed at 750°C for 30 sec to form low resistivity $CoSi_2$ (second RTA). Post annealing was conducted for capacitor fabrication process. The fabricated samples were analyzed by employing transmission electron microscope (TEM: Philips CM200 with field emission gun) and focused ion beam (FIB: Micrion 2500).



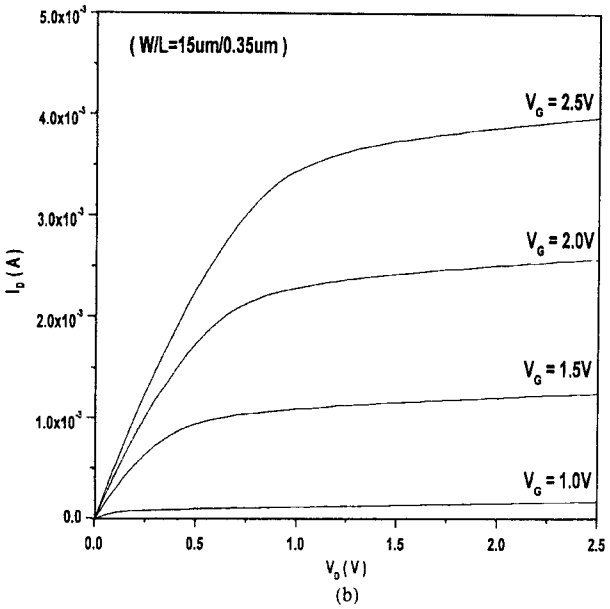


Fig. 1. Cobalt silicide of nMOSFET with n-type LDD (sample 1): (a) cross-sectional TEM of gate spacer edge region and (b) its I_D-V_D characteristics.

3. Results and Discussion

Fig. 1(a) shows a cross-sectional TEM picture of nMOSFET sidewall spacer region with n-type LDD (sample 1) exhibiting a well-formed cobalt silicide layer in the source/drain region. This sample shows no void defect under the sidewall spacer edge, and instead the silicide is encroached into the underneath region of sidewall spacer. The I_D-V_D characteristics of the nMOSFET is exhibited in Fig. 1(b), showing no current penetration through the pn junction between source/drain and channel, and no low dielectric breakdown at V_{GS} = 0 V. I_D, V_D and V_{GS} are drain current,

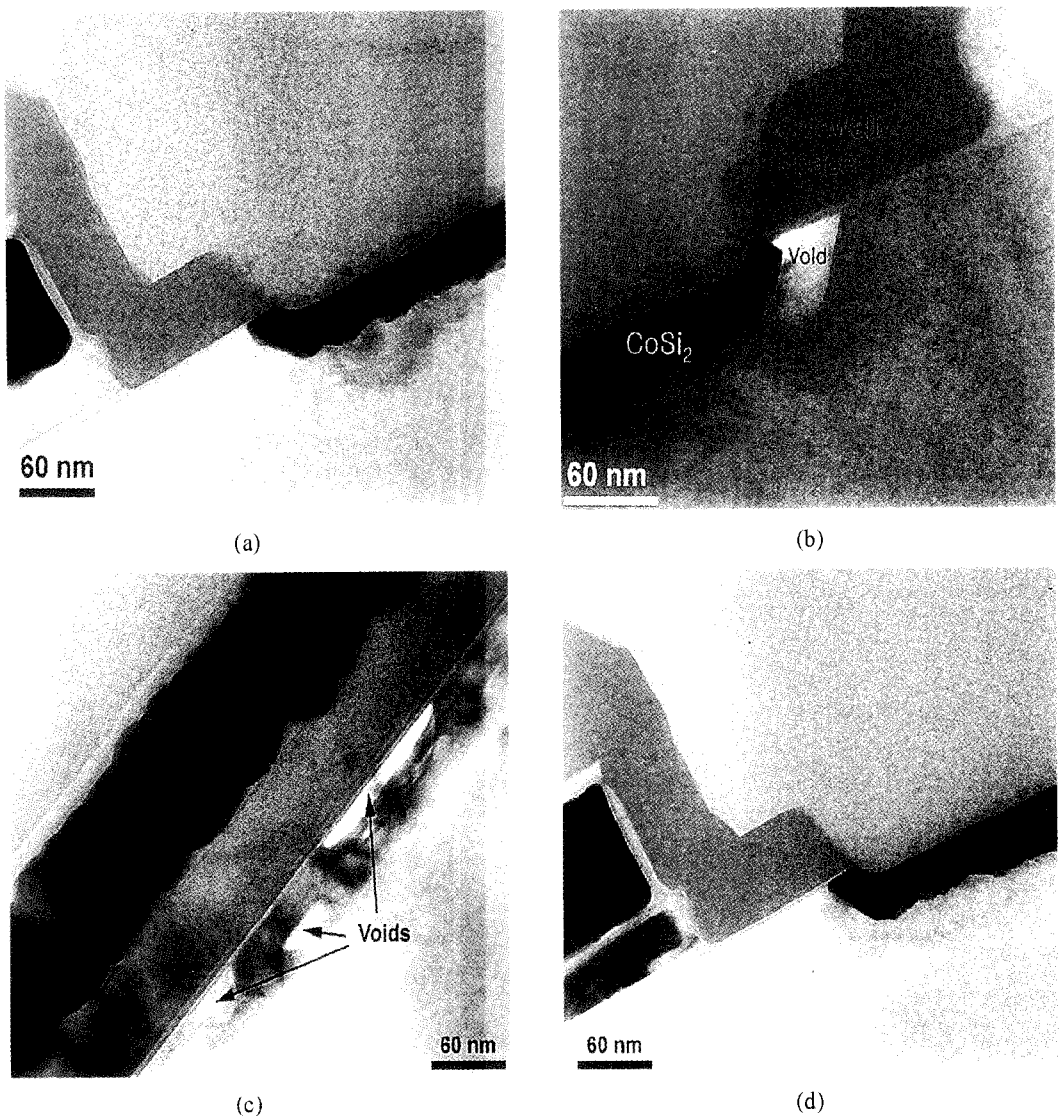


Fig. 2. Cobalt silicides of pMOSFET (a) with p-type LDD (sample 2), (b) with n-type LDD (sample 3), (c) along the gate direction of sample 3 and (d) with counter-doped p-type LDD (sample 4).

drain voltage and voltage between gate and source, respectively.

Three pMOSFET devices with different LDD structures were fabricated to evaluate the effect of dopants on the cobalt silicidation behavior. Fig. 2 shows cross-sectional TEM pictures of the three pMOSFETs. Fig. 2(a) shows pMOSFET sidewall spacer region with p-type LDD (sample 2) exhibiting similar cobalt silicide morphology as that of sample 1. pMOSFET with n-type LDD (sample 3) shown in Fig. 2(b), however, contains a void defect at the sidewall spacer edge. Byun *et al.*[5] reported that the void formation was due to lateral formation of cobalt monosilicide during the first RTA and the following formation of cobalt disilicide with the consumption of silicon from the substrate during the second RTA. While their void was formed in the Si substrate with lateral growth of cobalt silicide, our result showed little lateral growth of cobalt silicide and a void formed in the region instead. The void formed between channel and source/drain region reduced an appreciable amount of drain current,[9] and its mechanism was reported as agglomeration of Si vacancies generated during the cobalt silicidation.[6,10] Present experimental results, however, indicate that the dopant species affects the formation of void defects at the sidewall spacer edge during the cobalt silicidation process. During the first RTA of cobalt silicidation, cobalt on source/drain region reacts with Si to form cobalt disilicide while that on sidewall space edge seems to form some amount of cobalt monosilicide due to a retarded cobalt silicidation process by the n-type dopant. The unreacted metals were removed before the second RTA. Therefore, the void formation at sidewall spacer edge is believed to occur by the Si consumption from the Si substrate during the second RTA where cobalt mono-

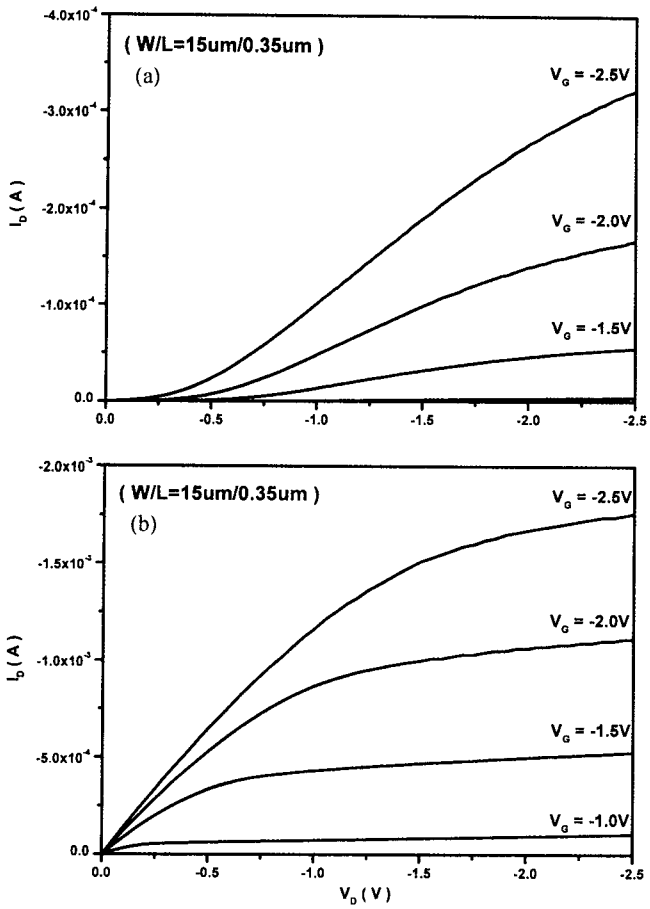


Fig. 3. I_D-V_D characteristics of pMOSFETs (a) with a void at the gate spacer edge and (b) without a void.

silicide transforms into cobalt disilicide at the cobalt monosilicide/Si (001) interface. Suppressed lateral growth of cobalt silicide at the sidewall edge supports this silicidation model. Fig. 2(c) shows the voids formed along the sidewall spacer edge by preparing TEM sample parallel to the gate direction. FIB technique is essential in preparing this TEM sample, due to its unique capability of probing a specific area for thinning.

When the n-type LDD of sample 3 is neutralized and changed to p-type LDD by counter-doping the LDD with p-type dopant, B (sample 4), the cobalt silicide layer is again well-formed as shown in Fig. 2(d). The lateral formation of cobalt silicide is observed with no void formation. This result indicates that the cobalt silicidation process is affected by the dopant species, requiring further investigation.

Fig. 3(a) shows the I_D-V_D characteristics of the pMOSFET with a void at the sidewall spacer edge (sample 3). The void serves as a resistance in the current-voltage characteristics of the pMOSFET device. The result is quite different compared with the pMOSFET with no void (sample 2), showing a typical current voltage characteristics as in Fig. 3(b).

4. Conclusion

Dopant species of LDD ion implantation affects the defect formation at the MOSFET sidewall spacer edge. Cobalt silicidation of nMOSFET with n-type LDD structure and pMOSFET with p-type LDD produces well-developed cobalt silicides with its lateral growth underneath the sidewall spacer.

Void is formed at the sidewall spacer edge of pMOSFET with P-doped n-type LDD structure. The void formation seems to be due to a retarded silicidation process at the LDD region during the first RTA for the reaction of Co with Si, resulting in some amount of cobalt monosilicide at the LDD region. The subsequent second RTA converts the cobalt monosilicide into cobalt disilicide with the consumption of Si atoms from the Si substrate, producing void in the Si region. pMOSFET with a counter-doped LDD is prepared by counter-doping the P-doped n-type LDD with B dopant. Cobalt silicidation of this pMOSFET produces a well-developed cobalt silicide with its lateral growth underneath the sidewall spacer. Therefore, we believe that the cobalt silicidation process is affected by the dopant species. The void formed at the sidewall spacer edge serves as a resistance in the current-voltage characteristics of the pMOSFET device.

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