Dynamic Power Supply Current Testing for Open Defects in CMOS SRAMs

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The detection of open defects in CMOS SRAM has been a time consuming process. This paper proposes a new dynamic power supply current testing method to detect open defects in CMOS SRAM cells. By monitoring a dynamic current pulse during a transition write operation or a read operation, open defects can be detected. In order to measure the dynamic power supply current pulse, a current monitoring circuit with low hardware overhead is developed. Using the sensor, the new testing method does not require any additional test sequence. The results show that the new test method is very efficient compared with other testing methods. Therefore, the new testing method is very attractive.

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I. INTRODUCTION

In an SRAM testing, various fault models such as stuck-at, transition, coupling faults are used unlike random logic testing [1], [2]. In order to detect these faults, March test [3] has been widely used. However, some open defects on SRAM cells may not be detected by the conventional March tests. These open defects can be modeled as data retention faults and destructive read out faults. To detect these faults is very time consuming.

In a six-transistor CMOS SRAM cell, if the pull-up p-devices are too weak due to a fabrication defect such as a missing connection of the p-devices, a memory cell can write and memorize the input data but fails to retain its logic value after some time [1], [4]. The resulting fault in a defective cell is referred to as a data retention fault. The retention time depends on the leakage current and on the node capacitance. For the opens in the pull-down n-devices, data can be written into the defective cell, but the data stored in the defective cell can be affected by a destructive read out [5].

Traditionally, data retention faults are tested writing '0' or '1' in each address and after an allowed waiting time a read operation is made [2]. In [6], a soft-defect detection technique is proposed to test data retention faults. However, the implementation of this technique implies the inconvenience of modifications to the design of the basic six-transistor memory cell. Therefore, Iddq (Quiescent Supply Current) testing for data retention faults is proposed. However, the technique proposed in [7] requires modifications on the address decoder to access the whole memory cells. Furthermore, large currents may flow when the cells are accessed simultaneously. This current flow may cause reliability problems. In [8], an Iddq data retention test made in the lower power supply voltage corner, is proposed. However, this technique requires a long test time. In [9],

Iddq testing is used to detect data retention faults and destructive read out faults. But the Iddq testing has a substantial problem of taking too much time to measure the Iddq. Therefore, it requires long test time and high test cost.

Nowadays, a dynamic power supply current (Iddt) testing is proposed as an alternative or a supplement to Iddq testing for CMOS circuits. In [10], an SRAM testing by monitoring a dynamic power supply current is proposed. This method uses a special power distribution tree and a simple current sensor. With these circuits, the cell coupling faults can be easily detected and an efficiency of the dynamic power supply current testing for CMOS SRAM coupling faults is presented. In [11], Iddt testing is proposed to perform functional test, but it cannot handle open defects.

In order to perform efficient testing of data retention faults and destructive read out faults, a dynamic power supply current testing is proposed in this paper. Section II describes the basic concept of a dynamic power supply current testing. In section III and IV, how data retention faults and destructive read out faults affect the dynamic power supply current is presented. Section V presents the advantages and the cost of this method. Also, a comparison with other testing methods is described. In section VI, the current sensing technique is proposed and finally a conclusion is given in section VII.

II. DYNAMIC POWER SUPPLY CURRENT TESTING CONCEPT

In a CMOS six-transistor SRAM cell shown in Fig. 1, no current flows at a steady state. Whenever a cell switches its state, a measurable dynamic current pulse is established. Thus, the peak value of the dynamic current pulse gives useful information about the switching behavior of an SRAM cell [10]. Considering these current characteristics, a memory write operation can be classified into two kinds. One is a 'transition write' operation that changes the data in the cell. And the other is a 'non-transition write' operation that does not change the data in the cell [1].

In a fault free SRAM cell, only a transition write can establish the dynamic current pulse but a non-transition write or a read can't. Thus, if a dynamic current pulse is not sensed during a transition write or if it is sensed during a non-transition write or a read, we can conclude that this cell is faulty. Furthermore, if the peak value of the established dynamic current pulse during a transition write is prominently different from that of a fault free cell, there must be some defects in the accessed cell.

The dynamic current test can be implemented as shown in Fig. 2. The embedded Iddt current sensor measures the peak value of a dynamic current pulse when a read operation or a write operation is performed. The measured peak value of the dynamic current pulse is compared with the predetermined fault free value and if the measured value is prominently different from that of a fault free cell, the accessed cell is faulty.

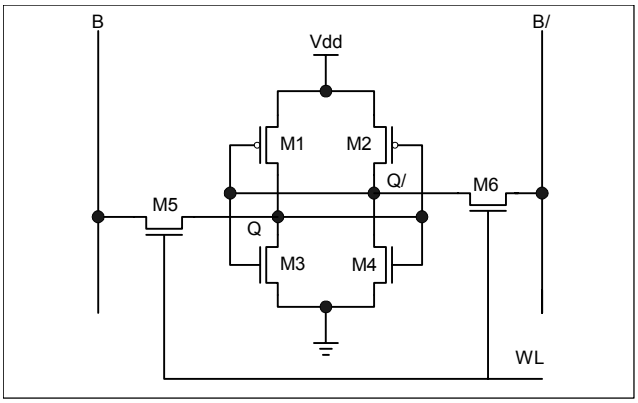

Fig. 1. A CMOS six-transistor SRAM cell.

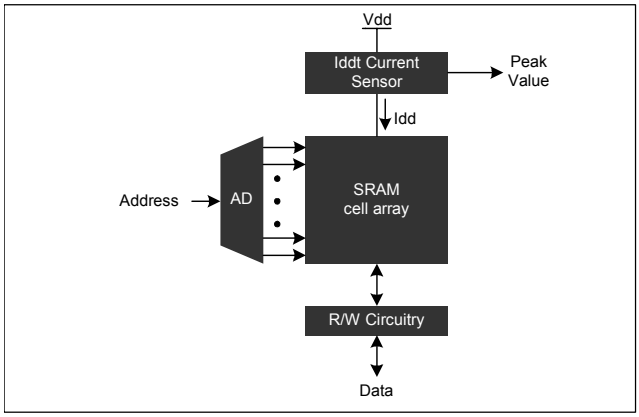

Fig. 2. Conceptual diagram of dynamic current test.

III. TESTING DATA RETENTION FAULTS

Data retention faults are due to a defective pull-up device. There are two types of pull-up defects, which are symmetric and asymmetric [4]. A symmetric defect is a defect affecting the conduction or the connection of both p-devices in the SRAM cell to Vdd, while an asymmetric defect affects only the connection or the conduction of one device. These defects are modeled in a circuit level as shown in Fig. 3. To model open defects, the value of an inserted resistor was selected to 100MΩ.

All circuit simulations were performed for a temperature of 25°C and Vdd of 5.0V. Following procedure was performed on a good cell, a cell with a symmetric pull-up defect, and a cell with an asymmetric pull-up defect.

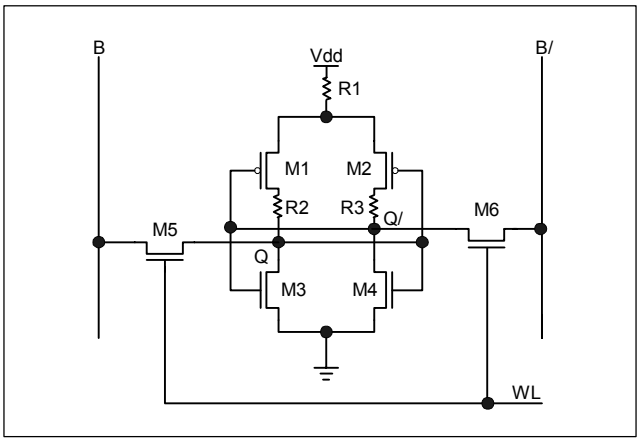

Fig. 3. Symmetric (R1) and asymmetric (R2, R3) defects.

(1) Initialize a cell to '1' using DC node voltages
(2) Pre-charge both bit lines
(3) Write '0' on the cell
(4) Pre-charge both bit lines
(5) Write '1' on the cell

The following subsections describe how the above procedure affects a dynamic power supply current of a good cell and defective cells.

1. A Good Cell

Because two write operations in the procedure write the opposite value of the data stored in the cell, both write operations are transition write operations. Thus, every write operation generates the dynamic current pulse. Figure 4 shows the current waveform of a good cell. The cell's initial value was '1', and transition write operations '0' and '1' are performed sequentially. The established dynamic current pulse has the peak value of 120uA.

2. A Cell with a Symmetric Pull-Up Defect

The same write sequence performed on a good cell was executed on a cell with a symmetric pull-up defect. Due to the pull-up defect, however, the current waveform shown in Fig. 5 is different from that of Fig. 4.

In Fig. 5, the peak value of dynamic current pulse when a transition write operation is 28nA, which is prominently different from that of a good cell.

3. A Cell with an Asymmetric Pull-Up Defect

Figures 6 and 7 are the current waveforms of a cell with an asymmetric defect due to R2 and R3, respectively.

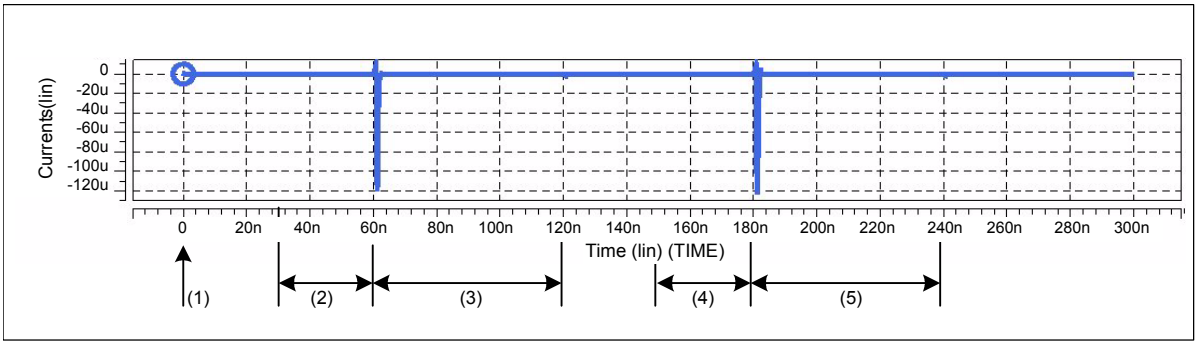

Fig. 4. A good cell.

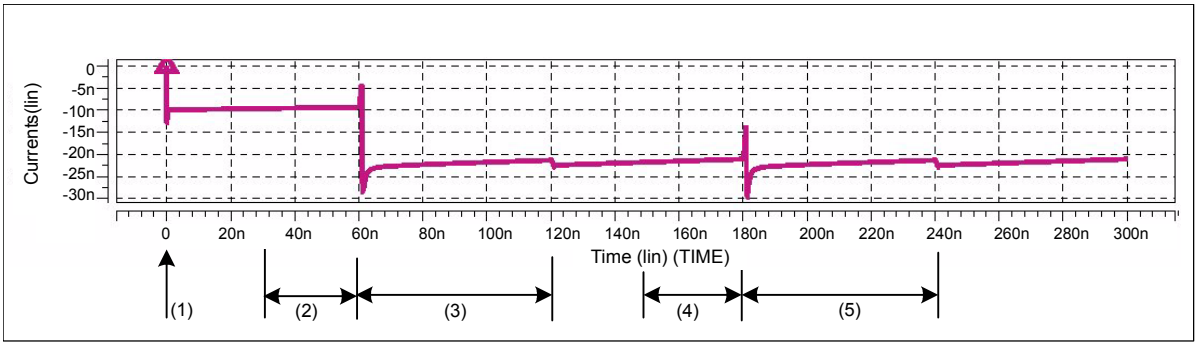

Fig. 5. A cell with a symmetric defect.

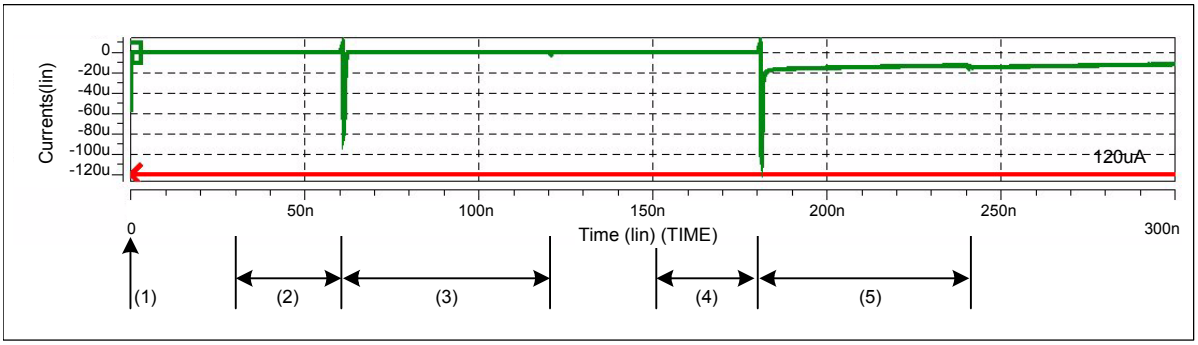

Fig. 6. A cell with an asymmetric defect R2.

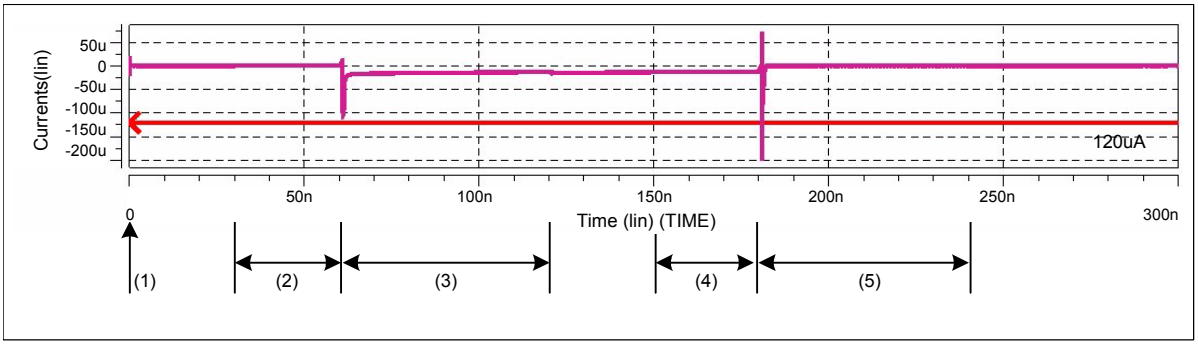

Fig. 7. A cell with an asymmetric defect R3.

The peak value of the first transition write in Fig. 6 is below 100uA and that of the second transition write in Fig. 7 is above 150uA. Thus, at least one of two transition write operations on a defective cell, establishes the dynamic current pulse whose peak value is prominently different from that of a fault free cell.

IV. TESTING DESTRUCTIVE READOUT FAULTS

Destructive read out faults are due to a defective pull-down device. For opens in the pull-down devices, it has been found that both states can be written, but one state can be affected by a destructive read-out. These faults can be modeled as shown in Fig. 8. The value of an inserted resistor is 100MΩ.

To show how an open defect in a pull-down n-device affects the dynamic power supply current, the following procedure was performed on each good cell and a cell with a defective pull-down transistor:

(1) Initialize a cell to '1' using DC node voltages
(2) Pre-charge both bit lines
(3) Write '0' on the cell
(4) Pre-charge both bit lines
(5) Read '0' on the cell

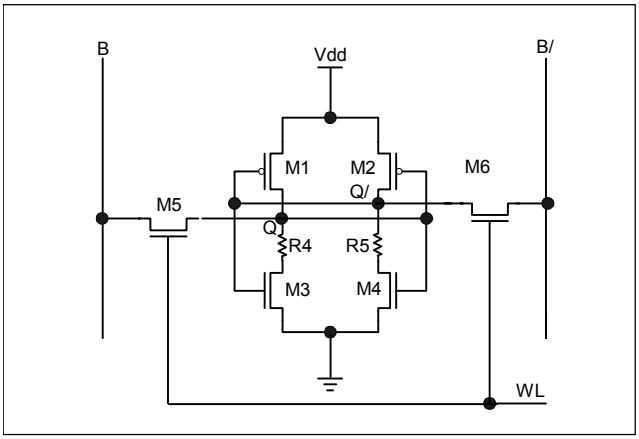

Fig. 8. Defects in pull-down transistors R4 and R5.

(6) Pre-charge both bit lines
(7) Write '1' on the cell
(8) Pre-charge both bit lines
(9) Read '1' on the cell

During the procedure, every write operation will make the dynamic current pulse whose peak value is 120uA, and every read operation will not make any current pulse. But if there is a change of the cell content during a read operation due to a de-

fective pull-down n-device, this read operation would make the measurable dynamic current pulse. The following subsections will show how the above procedure affects a dynamic power supply current of a good cell and defective cells.

1. A Good Cell

Figure 9 is a simulation result of (1) to (9) operations. As expected, write operations establish the dynamic current pulse of 120uA, but read operations can't affect a power supply current.

2. A Cell with a Defective Pull-Down N-Device

A defective pull-down due to an inserted R4 resistor made the current waveform of Fig. 10. When a read '0' operation is performed, the state of a cell is changed and the unexpected dynamic current pulse of 44.3uA is established. The simulation result for a cell with an inserted R5 is shown in Fig. 11. In this case, when a second read operation is performed, the state of a cell is changed and the dynamic current pulse of 44.3uA is also established.

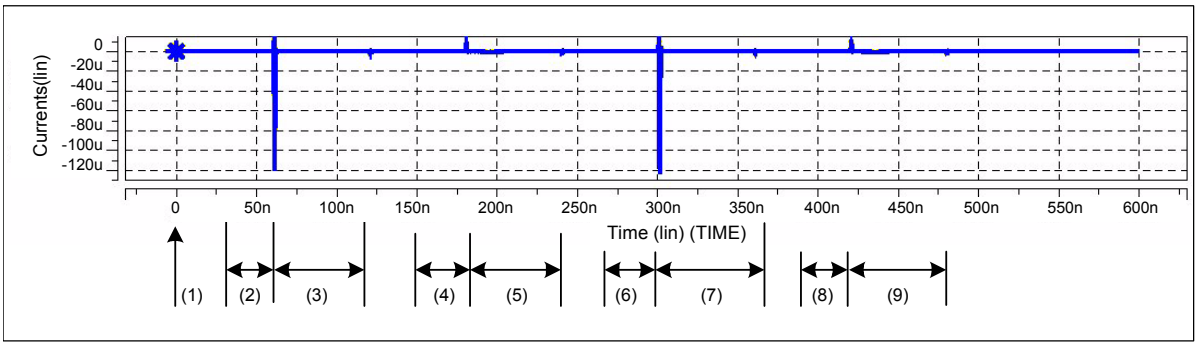

Fig. 9. A good cell.

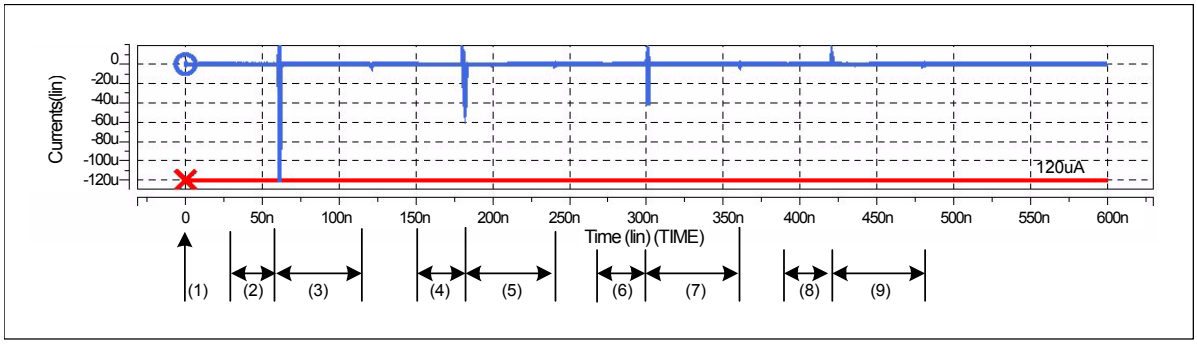

Fig. 10. A cell with R4.

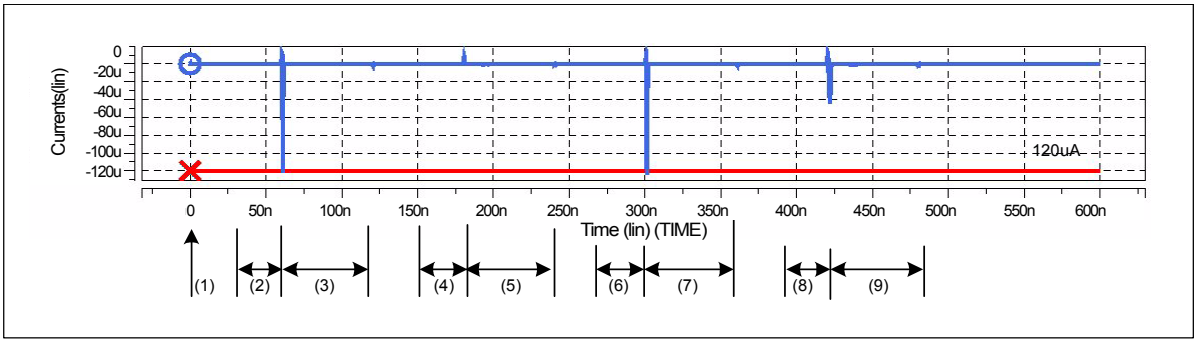

Fig. 11. A cell with R5.

V. PERFORMANCE EVALUATION

The simulation results of the Sections III and IV give the following properties.

- The peak value of a dynamic current pulse when a transition write on a cell with a defective pull-up device (data retention fault), is prominently different from that of a fault free cell.
- The read operation on a cell with a defective pull-down device (destructive read-out fault) makes the measurable dynamic current pulse whereas the read operation on a fault free cell does not.

Thus, if we can monitor the dynamic power supply current of a SRAM cell array, data retention faults can be detected by transition write '0' and transition write '1', and destructive read-out faults can be detected by read '0' and read '1'. In addition, almost all SRAM test algorithms include the transition write '0', transition write '1', read '0' and read '1'. Therefore, no additional test sequence is required to test open faults in an SRAM cell, and an additional hardware overhead is just the Iddt current sensor to detect and measure dynamic current pulses.

The method proposed in [4] consists of the following test sequences:

- W0; WR1; R1; W1; WR0; R1

Thus, in addition to the functional test, 6*n* test sequence where n is the number of cells, must be added to the functional test. And WR1 and WR0 stages take longer time than normal read and write operations. Therefore, considering the efficiency of [4] and its low hardware overhead (6 transistors per 1 column), it requires rather a long test time additionally to test data retention faults.

The method proposed in [9] requires Iddq sensor and an additional design for testability (DFT) circuitry or a power supply lowering logic is required. And an Iddq testing itself takes quite a long time. Table 1 shows comparison results.

Compared to the previous test methods, the proposed method using a dynamic power supply current has following advantages.

- No additional test sequence : Other approaches require additional test sequences.
- Low hardware overhead. : Only Iddt current sensors are required while other approaches require additional hardware according to the number of columns.

Table 1. Performance comparison.

	Additional test sequence for for open defects	Fault coverage	Hardware overhead
[4]	6*n* test sequence	Pull-up defects only	6 transistors per column and additional control signals
[9]	2 Iddq measurements and 2*n* test sequence	Pull-up defects and pull-down defects	Iddq sensor and 6 transistors per column or power supply lowering logic
New	No additional sequence required	Pull-up defects and pull-down defects	Iddt current sensor

VI. CURRENT SENSING TECHNIQUE

To detect dynamic current pulses, a current sensor is required. There are two kinds of the current sensors. One is an external sensor and the other is a built-in sensor. Since an external sensor in [12] uses the current transformers, it can be used only in the Automatic Test Equipment (ATE). To use this external sensor, an SRAM structure has to be modified. The SRAM cell array and the other peripheral circuits must use the separate power supply pins, because dynamic current pulses occur only in a cell array. Built-in sensors have been shown in [10] and [13]. A current sensor suggested in [10] is a very simple structure. Only one capacitor, one transistor, and one comparator are required. To use this current sensor, however, the special power distribution tree is required in an SRAM, and this results in additional circuit overhead. A current sensor of [13] consists of a current detector, a differential amplifier, a dummy current detector, reference voltage generators, and comparators.

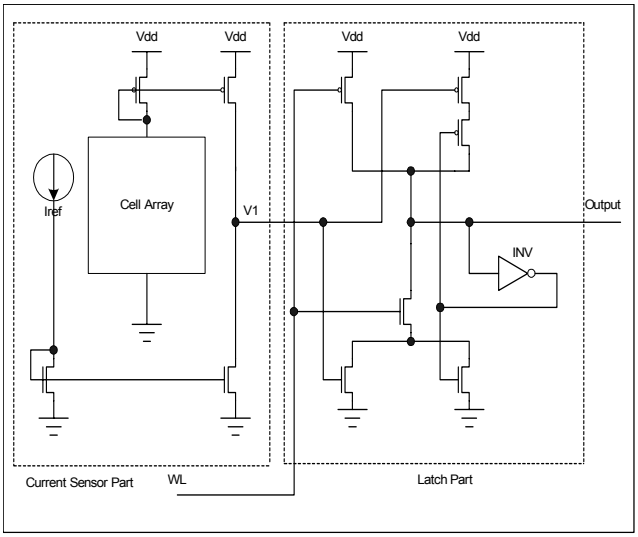

Fig. 12. A new current sensor.

A new current sensor is developed which can detect a dynamic current pulse and even can distinguish its peak value from the predetermined reference value. The current sensor shown in Fig. 12 consists of two parts: the current sensor part and the latch part. The current sensor part coverts the dynamic

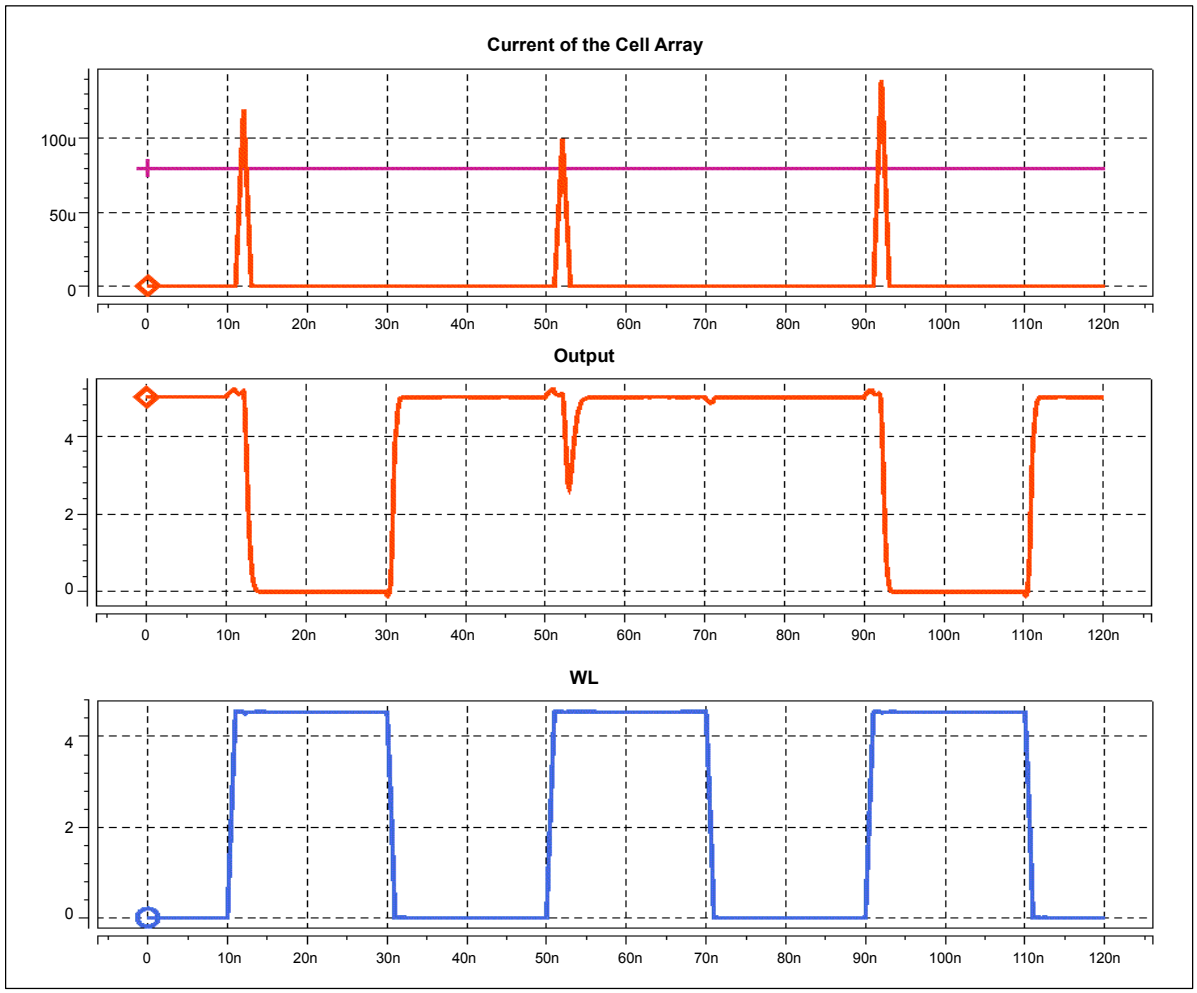

Fig. 13. Simulation results of current sensor.

current pulse into the voltage pulse at V1, and once the voltage pulse is detected by the latch part, this latch retains the value until the SRAM's word line (WL) becomes '0'. WL may be replaced by any other memory control signal.

Figure 13 shows the simulation results of the current sensor. Since the latch part retains V1 voltage of the current sensor until the end of the WL, we can read the output of the current sensor at the falling edge of the WL. This current sensor output indicates whether the peak value of the dynamic current pulse exceeds a certain reference value or not. A current sensor has its own reference value, Iref. Therefore, in order to test SRAMs, three different current sensors are required. The first is the lower bound and the second is the upper bound. If the peak value of a dynamic current pulse exceeds the upper bound, or if it could not reach the lower bound, we can conclude that the accessed cell is faulty. In addition, to detect a dynamic current pulse when a read operation is performed, the third current sensor whose Iref is about a 30uA, is required. Therefore, with 3 current sensors, dynamic power supply current testing can be performed.

VII. CONCLUSION

In this paper, the current characteristic of CMOS SRAMs is analyzed. In order to test open defects efficiently in CMOS SRAM cells, a new test method using a dynamic power supply current is developed. Also, an Iddt sensor for monitoring dynamic current pulses is designed. From the simulation results, the peak value of a dynamic current pulse is prominently different from that of a fault free cell when a transition write or a read is performed. Thus, if we monitor a dynamic current pulse during a transition write or a read, we can detect open defects in a CMOS SRAM cell. The new testing method does not require any additional test sequence for open defects as long as the functional test includes transition write '0', transition write '1', read '0', and read '1'. Since most of conventional functional test algorithms include transition write '0', transition write '1' and read '0', read '1', the new method is very attrac-

tive. Comparisons with other testing methods show the effectiveness and advantages of the new testing method.

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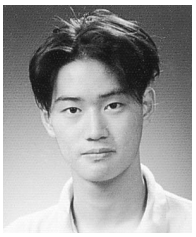

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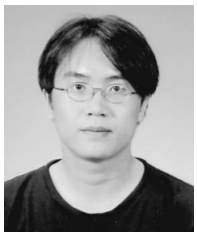

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