Statistical Modeling of 3-D Parallel-Plate Embedded Capacitors Using Monte Carlo Simulation

Ilgu Yun , Ravi Poddar, Lawrence Carastro, Martin Brooke, and Gary S. May

Examination of the statistical variation of integrated passive components is crucial for designing and characterizing the performance of multichip module (MCM) substrates. In this paper, the statistical analysis of parallel plate capacitors with gridded plates manufactured in a multilayer low temperature cofired ceramic (LTCC) process is presented. A set of integrated capacitor structures is fabricated, and their scattering parameters are measured for a range of frequencies from 50 MHz to 5 GHz. Using optimized equivalent circuits obtained from HSPICE, mean and absolute deviation is calculated for each component of each device model. Monte Carlo Analysis for the capacitor structures is then performed using HSPICE. Using a comparison of the Monte Carlo results and measured data, it is determined that even a small number of sample structures, the statistical variation of the component values provides an accurate representation of the overall capacitor performance.

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I. INTRODUCTION

As microelectronics technology continues to progress, there is a continuous focus on higher levels of system integration and miniaturization. For example, in many applications, it is desirable to package several integrated circuits (ICs) together in multichip modules (MCMs) to achieve further compactness and higher performance. Passive components (i.e., capacitors, resistors, and inductors) are essential requirements for many MCM applications [1]. A significant advantage of MCM technology is the ability to embed large number of these passive components directly into the substrate at low cost. Such an arrangement provides further advantages in component miniaturization, power consumption, reliability, and performance.

One technology that shows great promise for embedding passives in large area substrates is the multilayer low-temperature cofired ceramic (LTCC) approach [2]. The LTCC process can support well over thirty layers of metal, each on a thin ceramic tape substrate (several mils thick), with interconnectivity between layers achieved by the use of vias. LTCC is very attractive for embedding of inductor and capacitor structures, and even resistors if a high resistivity material is used. Therefore, LTCC technology shows considerable potential as an enabling technology for the next generation of highly compact systems.

Successful design of passive structures in LTCC systems requires that accurate models of the various components exist or can be easily obtained. However, for high frequency designs, most LTCC passive structures are electrically long and, due to their full 3-dimensional geometries, have very complex field patterns. Standard modeling methods for microstrip or stripline based structures do not apply for these components. In order to successfully design LTCC structures for high frequencies, the

behavior of the passive components that comprise the structure must be characterized accurately at those frequencies. Recently, computer-aided design tools such as HSPICE [3] have become indispensable in IC design. Accurate circuit simulation using HSPICE is dependent on both the structural validity of the device models and the accuracy of the values used as model parameters. Therefore, the extraction of an optimum set of device model parameter values is crucial to characterizing the relationship between the model and the measured behavior.

Recently, design and modeling issues for embedded passive components have been investigated by several authors. Since building block based modeling of integrated passives was presented by Poddar *et al*. [4], many other designs and modeling schemes have been developed. For example, electrical and mechanical modelings of embedded capacitors were investigated by Rao *et al*. using the finite element method [5]. Sood *et al*. studied macromodeling of embedded passive components in high performance LTCC packages using SPICE simulation [6]. Fathy *et al*. presented modeling and design guidelines for embedded passives in LTCC on metal technology [7]. Yun *et al*. presented accurate device model parameter optimization for embedded passives using genetic algorithms [8].

In this paper, the statistical variation of gridded parallel plate capacitors manufactured in a multilayer LTCC process is investigated. A set of integrated capacitor structures was fabricated, and their scattering parameters were measured for a range of frequencies from 50 MHz to 5GHz. Using optimized equivalent circuits obtained from HSPICE and the building block based modeling method [8], the mean and standard deviation was calculated for each component of each device model. Monte Carlo Analysis for the capacitor structures was then performed using HSPICE. Using a comparison of the Monte Carlo results and measured data, it was determined that even for a small number of sample structures, the statistical variation of the component values provides an accurate representation of the overall capacitor performance.

II. TEST STRUCTURE DESCRIPTION

Test structures were fabricated in a 12-layer LTCC process. The top metal layer was on layer 10, and the bottom layer was on layer 11, with ground connections on layer 12. The metal thickness used was 10 mils for both plates, and the grid size was held constant, with grid "holes" of 30 × 30 mils. All capacitor structures were two layers, with a separation distance of one layer of ceramic tape in order to maximize capacitance. The upper and lower conductors were completely coincident so that the metal lines of the top conductor completely overlapped the metal lines of the lower conductor. All connections to the devices were made using a ground-signal-ground probe pad pattern on the top later, with connections made to the devices using stacked vias and interconnect. All interconnect to and between structures was drawn on a single layer.

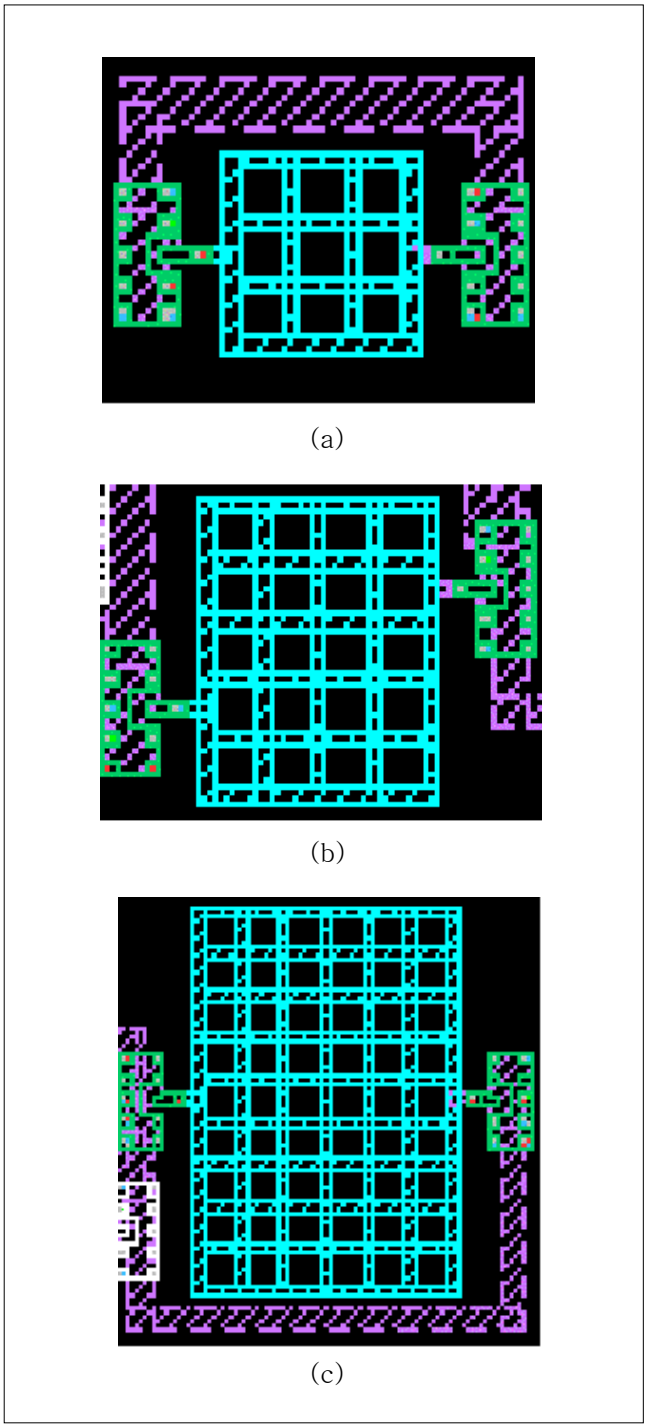


Fig. 1. Schematic diagram of (a)3×3; (b)5×4; and (c)9×6 gridded parallel plate capacitor structures.

The first test structure consisted of probe pads connected to a

3×3 grid square parallel plate capacitor. The probe pad was designed such that the interface was on the top of layer for probing, with 12-layer deep via stacks for connecting probes to the ground plane, and 11-layer deep via stacks for connecting the signal probe to the interconnect layer. The second structure tested consisted of probe pads connected to a 5×4 grid square parallel plate capacitor, and the third test structure was probe pads connected to a 9×6 grid square parallel plate capacitor. These test structures allowed modeling of probe pads, interconnects, and one square of the gridded parallel plate capacitor (consisting of four vertical parallel line segments), taking into account fringe effects and coupling to the ground layer. Schematic diagrams of the three test structures are shown in Fig. 1.

III. PROCESSING AND MEASUREMENT

The LTCC structure was physically designed using integrated circuit design tools within the Cadence *Virtuoso* design environment. A custom technology file for a 12-layer process was developed, and a process design rule-compliant test structure coupon was produced. The design was fabricated at the National Semiconductor Corporation LTCC fabrication facility. The size of the completed coupon was approximately 2.25"×2.25". The design utilized 12 layers of ceramic tape with a dielectric constant 7.8. Each layer of tape was 3.6 mils thick. Metal lines were drawn 10 mils wide, and the vias had a diameter of 5.6 mils. Interconnectivity between layers was achieved using stacked vias. The embedded structures were interfaced accessed using ground-signal-ground probe pads on the exposed top layer, with signals reaching the embedded layers through vias. The complete test structure coupon is shown in Fig. 2.

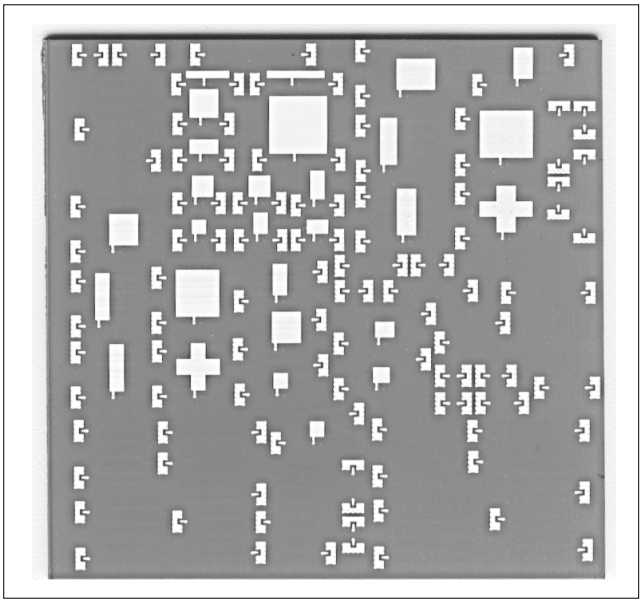


Fig. 2. LTCC coupon. (Only exposed top layer is visible.)

The test structures were measured using network analysis techniques. Since very low loss metal was used in the manufacturing process, DC resistance measurements were unreliable and not used. For high frequency measurements, an HP 8510C network analyzer was used in conjunction with a Cascade Microtech probe station and ground-signal-ground configuration probes. Calibration was accomplished using a supplied substrate and utilization of the line-reflect-match (LRM) calibration method. Data was gathered for each of the test structures at over 200 frequency points between 45MHz and 5GHz and stored with the aid of data acquisition software.

IV. MODELING SCHEME

1. Capacitor Modeling Procedure

A novel method of full 3-D embedded gridded parallel plate capacitor modeling and simulation has been utilized. This method is based on the generation of passive circuit element models [8]. This approach first determines a set of fundamental circuit building blocks for the capacitors, and then test structures are designed, fabricated, and their s-parameters are measured up to a desired frequency. Afterwards, the electrical contribution to the overall capacitor response by individual building blocks is determined. Equivalent circuit models of each building block are then extracted using a hierarchical extraction procedure. These building block equivalent circuits are then used to construct a large area gridded plate capacitor circuit that is geometrically comprised of the blocks. Simulation of the constructed circuit using the HSPICE circuit simulator provides an accurate prediction of the behavior of the test structure in a fraction of time and using far fewer resources than the traditional EM/RF solution methodology. The model of the test structure is then verified experimentally by comparing the predicted response with that measured directly from the manufactured structure.

LTCC technology is very well suited for the fabrication of large valued two-layer metal-insulator-metal (MIM) capacitors for use in applications such as power supply decoupling and filtering. In LTCC processes, however, metal is screen printed onto the ceramic tape substrates. This procedure creates limitations with respect to metal coverage. As a result, the process used here had a specified design rule, which limited the guaranteed unbroken metal coverage area to be relatively small. This directly limited the dimensions of solid parallel plates that might be used for the design of standard solid-plate parallel plate capacitors. In order to overcome the metal area design

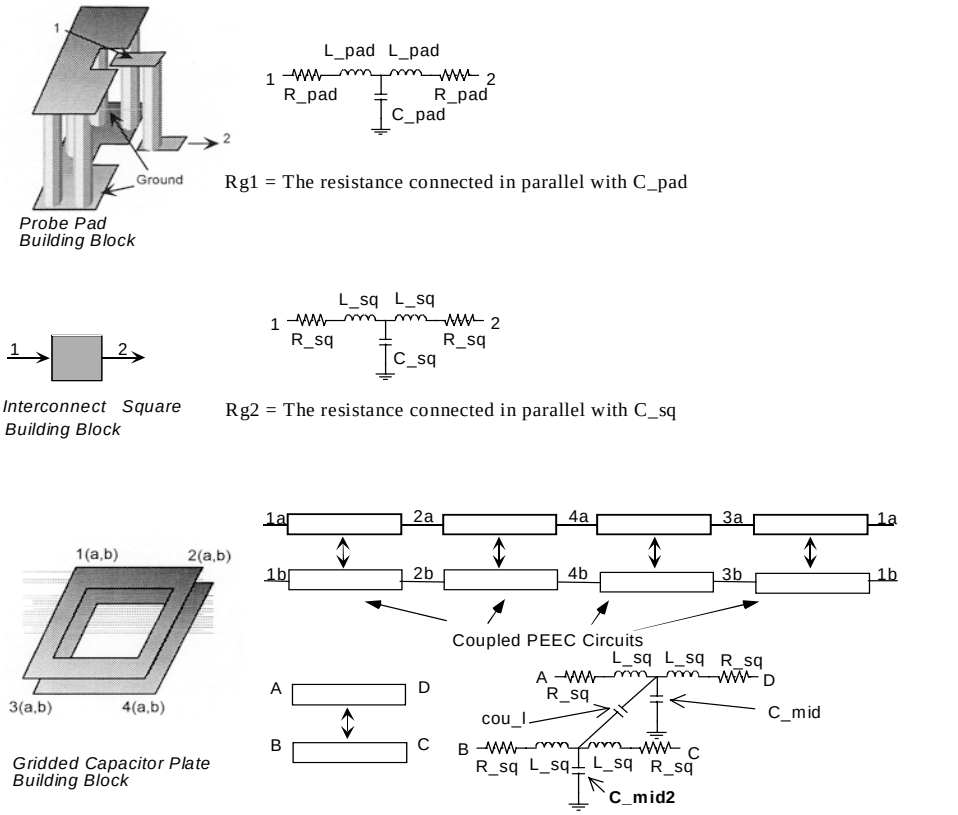


Fig. 3. Equivalent circuits associated with building blocks for test structures

Table 1. Extracted circuit model parameters.

	C (Capacitor Grid Size) c (coupon number)								
	C3×3_c1	*C3×3_c2*	*C3×3_c3*	*C5×4_c1*	*C5×4_c2*	*C5×4_c3*	*C9×6_c1*	*C9×6_c2*	*C9×6_c3*
Rg1	**1.00E+08**	5.55E+07	**1.00E+08**	**1.00E+08**	**1.00E+08**	**1.00E+08**	**1.00E+08**	**1.00E+08**	**1.00E+08**
Rg2	1.56E+11	5.30E+09	9.01E+11	5.15E+10	1.58E+10	2.62E+10	1.16E+11	1.65E+06	1.44E+10
Rg3	1.24E+05	1.65E+05	3.81E+05	3.28E+06	2.27E+08	7.08E+05	8.37E+07	1.35E+06	2.20E+07
Rg4	6.27E+04	2.74E+04	2.06E+05	1.69E+07	2.34E+06	1.02E+06	3.46E+06	6.79E+05	4.48E+05
R_pad	**1.00E-06**	2.05E-07	**1.00E-06**	**1.00E-06**	**1.00E-06**	**1.00E-06**	**1.00E-06**	**1.00E-06**	**1.00E-06**
L_pad	5.83E-10	9.25E-11	1.15E-09	3.23E-10	4.81E-10	1.40E-11	8.53E-10	1.00E-15	1.22E-09
C_pad	8.53E-13	3.95E-13	**1.00E-15**	1.86E-12	1.52E-12	1.18E-12	1.30E-12	1.49E-12	1.06E-15
cou_l	**1.00E-03**	9.57E+00	2.19E-01	2.81E+00	5.77E+00	1.03E+00	6.38E-03	1.93E+01	9.43E+00
R_sq	3.93E+00	4.36E+00	3.75E-01	3.58E+00	2.68E+00	2.39E+00	2.94E-05	1.18E+00	1.19E+00
L_sq	1.02E-25	2.82E-24	2.23E-24	5.97E-10	2.77E-10	3.14E-09	8.83E-10	4.50E-10	2.37E-10
C_sq	1.34E-13	1.41E-13	1.86E-13	1.14E-13	1.13E-13	1.18E-13	1.23E-13	1.15E-13	1.14E-13
c_mid	1.14E-14	2.73E-14	1.26E-14	2.37E-14	2.33E-14	8.39E-15	7.98E-15	1.29E-14	1.49E-14
c_mid2	2.64E-16	1.96E-14	1.29E-15	6.80E-16	1.69E-14	3.75E-15	3.25E-14	3.99E-14	2.47E-14

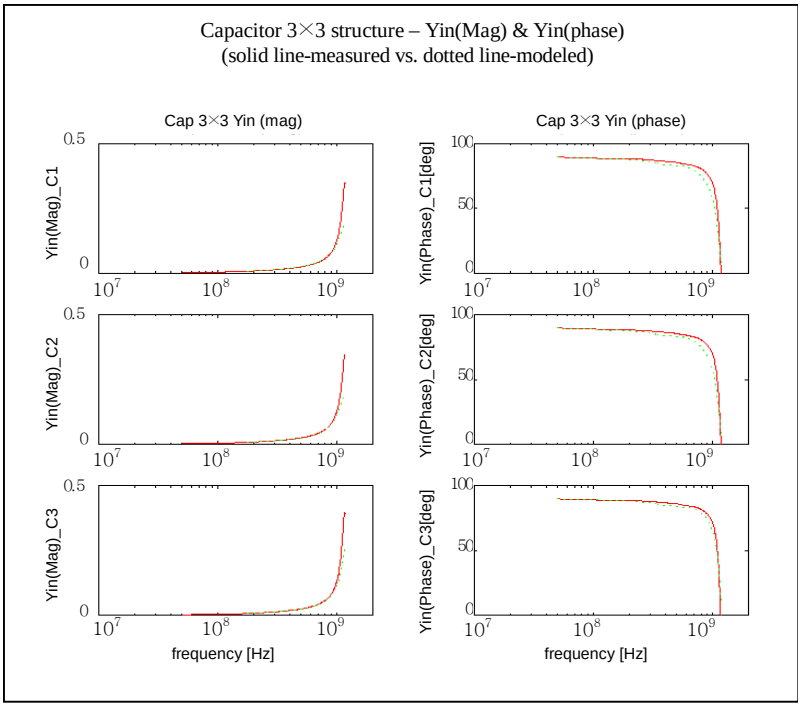


Fig. 4. 3×3 test structure optimization results: Yin (Magnitude) and Yin (Phase).

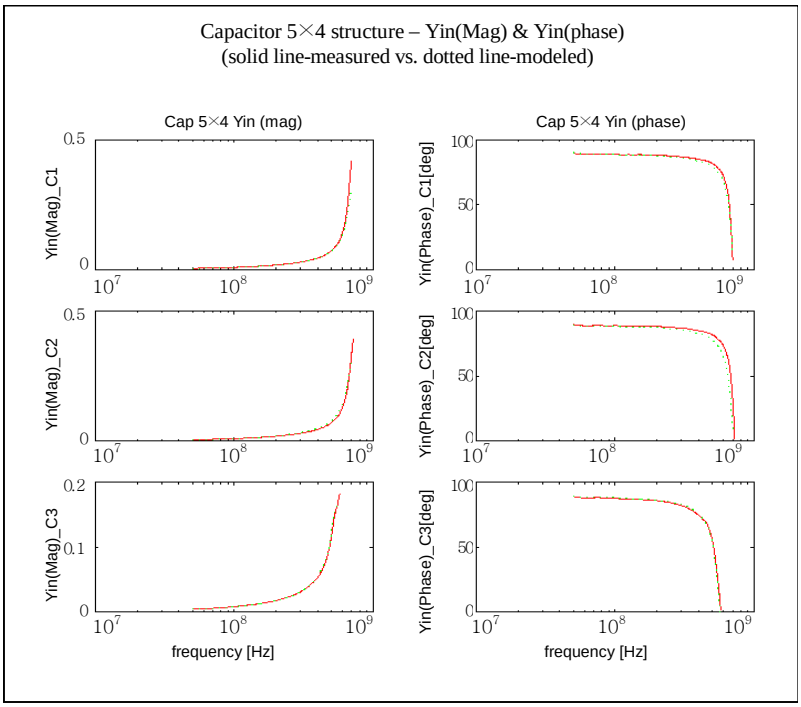


Fig. 5. 5×4 test structure optimization results: Yin (Magnitude)and Yin (Phase).

rule and still be able to generate large area capacitors, a design was developed which replaced the solid parallel plates of the capacitor with gridded plates. It was estimated that due to the many fringing fields, the gridded plate capacitor might approximate the actual capacitance achieved by the use of solid plates. The gridded parallel plate capacitor would also be quite difficult and time consuming to model using standard numerical techniques, and is therefore a good test for the modeling method.

The first step involved in the modeling procedure was a determination of what types of structures and geometries were to be modeled. As mentioned above, three different size structures were considered: 3×3, 5×4, and 9×6 grid squares. Modeling of gridded plate capacitors are very important to ensure that they function as intended at high frequencies. Gridded plate capacitor modeling using the hierarchical technique only required three building blocks: a probe pad, the interconnect material square, and the gridded capacitor square block (consisting of surrounding metal lines and one grid "hole"). These building blocks are shown in Fig. 3.

2. Parameter Extraction

After s-parameters for the test structures were measured, circuit models were extracted for the various building blocks. The fundamental circuits used were based on the partial element equivalent circuit (PEEC) [9] which has been used extensively for interconnect analysis [10] and general 3-D high frequency structural simulation [11]. The overall equivalent circuits are comprised of a combination of these building blocks with modifications to take into account building block topology and various coupling phenomena. The extraction of the circuit model parameters was achieved in several steps. Due to the highly nonlinear nature of the system equations with respect to circuit parameter values, a procedure for hierarchical optimization with respect to measured s-parameter data was chosen. The optimization algorithm was the Levenberg-Marquardt (LM) method [12], which is a combination of steepest descent and the Gauss-Newton method. Steepest descent is used initially to approach the solution, and then the Gauss-Newton method is used to refine the solution. The objective function of LM algorithm is as follows:

$$F_o(X)\Big|_{X=(x_1,x_2,\ldots,x_n)} = \sum_{i=1}^{m}\left[w_i \frac{f_i(X)-F^i_{meas}}{F^i_{meas}}\right]^2 \qquad (1)$$

where X = (x_1, x_2,…,x_n) are the component values to be extracted, n is the total number of parameters, F^i_{meas} is the measured value of the ith model parameter, m is the total number of measurements, f_i (X) is the simulated value of the ith point, and w_i is a weight factor for the ith measured data point (used for giving higher significance to a given data point). Using the LM procedure, the HSPICE optimizer finds the vector X of the device model parameters that minimizes F_o(X).

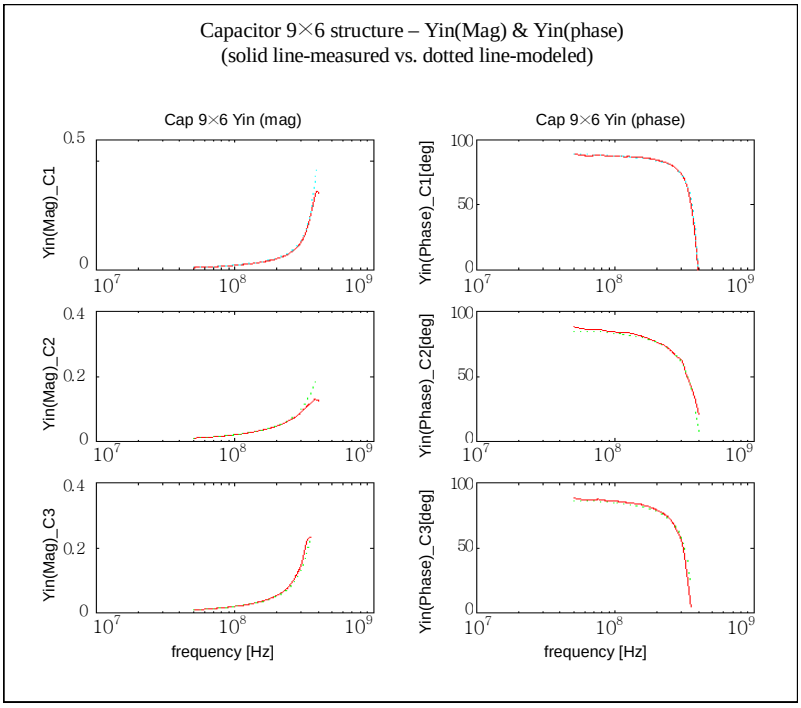


Fig. 6. 9×6 test structure optimization results: Yin (Magnitude)and Yin (Phase).

All simulations were performed using the HSPICE circuit simulator on Sun SPARC 20 series workstations. The starting point or initial guesses of the values of circuit parameters were crucial for correct optimization results, and these were approximated directly from measured data. Three test structures were optimized with respect to measured s-parameter data, and their individual building block equivalent circuit model parameters were extracted. However, for these capacitor test structures, y-parameters are more informative (especially the input admittance Y_{in} which is the same as Y_{11}) than s-parameters, and based on the input admittance, the accuracy of the s-parameter measurements could be verified. Therefore, y-parameters for the three test structures were calculated using the following parameter conversion equations [13]:

$$y_{11} = \frac{1}{Z_o}\left[\frac{(1+s_{22})(1-s_{11})+s_{12}s_{21}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}}\right] \qquad (2)$$

$$y_{12} = \frac{1}{Z_o}\left[\frac{-2s_{12}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}}\right] \qquad (3)$$

$$y_{21} = \frac{1}{Z_o}\left[\frac{-2s_{21}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}}\right] \qquad (4)$$

$$y_{22} = \frac{1}{Z_o}\left[\frac{(1+s_{11})(1-s_{22})+s_{12}s_{21}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}}\right] \qquad (5)$$

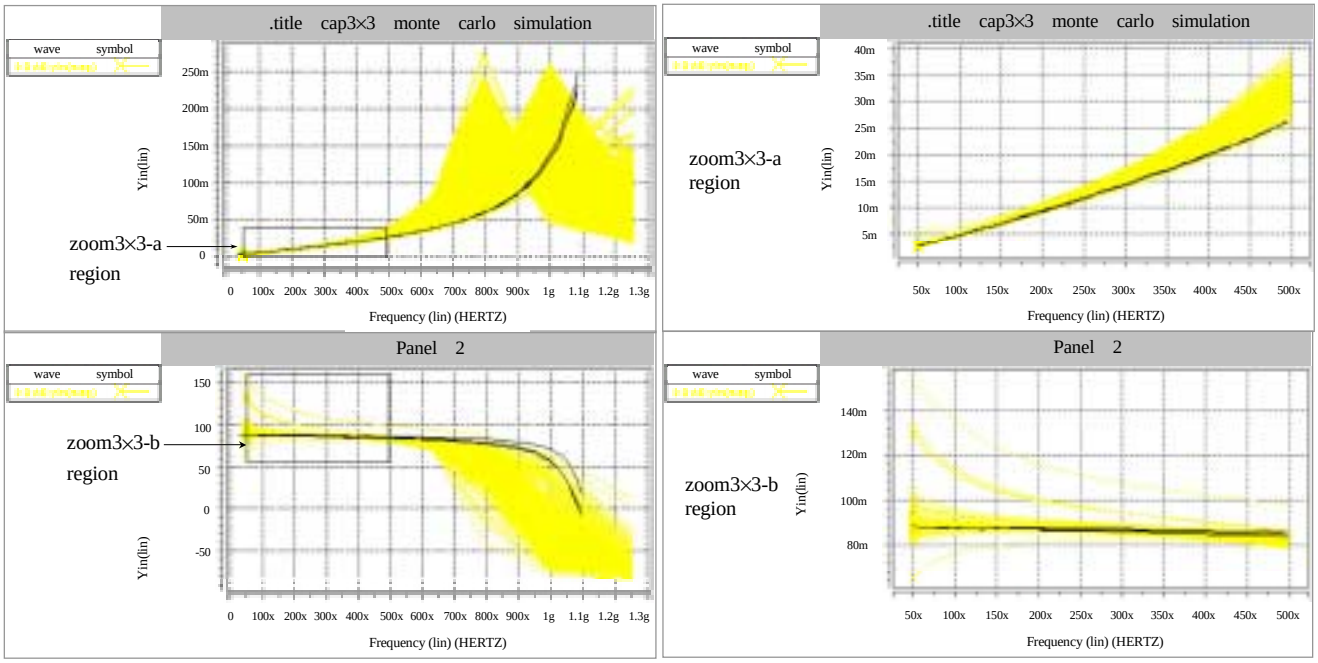
The measured versus optimized results for the three test structures are shown in Figs. 4, 5 and 6. As seen in these plots, very good agreement has been obtained for both Y_{in} (Mag) and Y_{in} (Phase) for the three test structures. In addition, the extracted circuit model parameters are shown in Table 1.

Table 2. Summary statistics for extracted circuit model parameters.

	Mean	Standard Deviation	Mean Absolute Deviation	Percent Deviation (PD)
	(Avg)	(STD)	(MAD)	(PD = MAD/Avg)
Rg1	9.51E+07	1.483E+07	8.79E+06	924.73%
Rg2	1.43E+11	2.893E+11	1.71E+11	11993.14%
Rg3	3.76E+07	7.594E+07	5.22E+07	13899.38%
Rg4	2.80E+06	5.425E+06	3.29E+06	11753.43%
R_pad	9.12E-07	2.651E-07	1.57E-07	1723.05%
L_pad	5.24E-10	4.675E-10	3.80E-10	7247.70%
C_pad	9.56E-13	6.844E-13	5.77E-13	6035.01%
cou_l	5.35E+00	6.506E+00	5.04E+00	9426.12%
R_sq	2.19E+00	1.583E+00	1.33E+00	6099.25%
L_sq	6.21E-10	9.929E-10	6.19E-10	9969.08%
C_sq	1.29E-13	2.353E-14	1.67E-14	1296.01%
c_mid	1.58E-14	7.120E-15	5.95E-15	3760.74%
c_mid2	1.55E-14	1.490E-14	1.24E-14	8031.61%

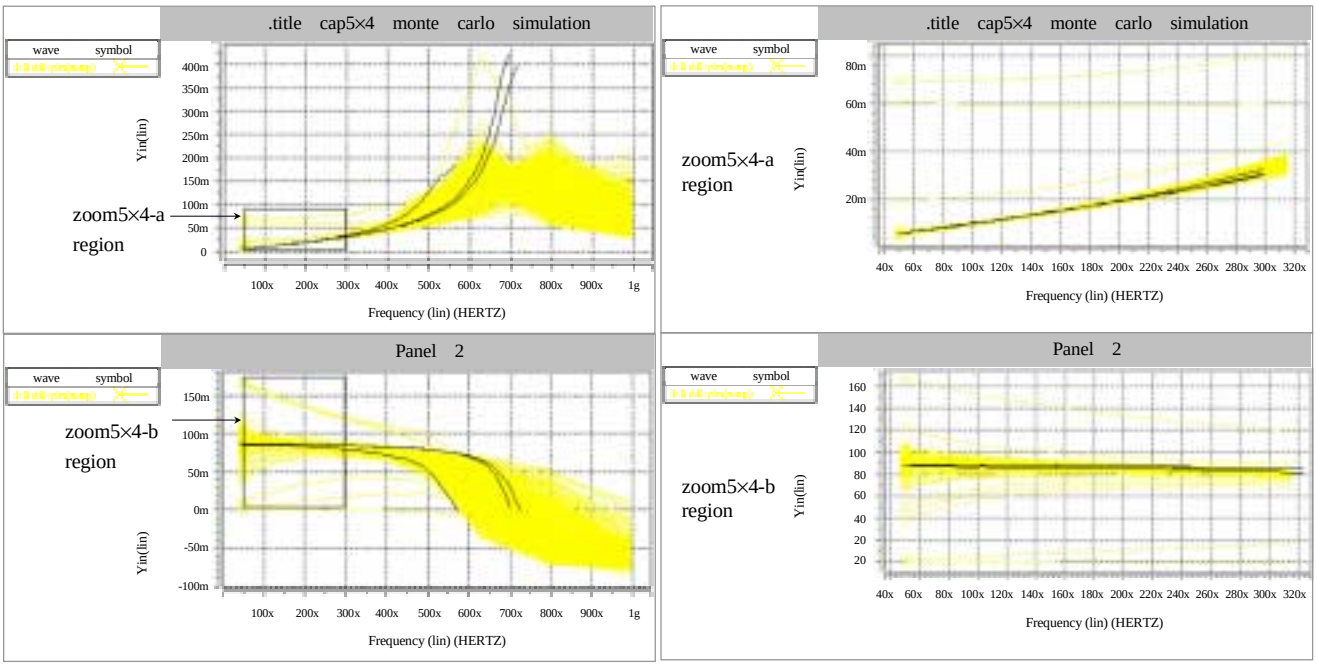
3. Monte Carlo Analysis

After circuit model parameters were extracted, the summary statistics (i.e., mean and standard deviation) from 9 sets of extracted model pa-



(a) (b)

Fig.7. Monte Carlo analysis results for 3x3 test structure: (a) whole optimized region and (b) zoom-in region for behaving as a capacitor.



(a) (b)

Fig.8. Monte Carlo analysis results for 5x4 test structure: (a) whole optimized region and (b) zoom-in region for behaving as a capacitor.

rameters (3 test structures of each size) were computed. These summary statistics are given in Table 2. Based on these statistics, Monte Carlo analysis for the capacitor structures was then performed using HSPICE. A Monte Carlo simulation with Gaussian parameter distribution was generated for 500 sets of circuit model parameters. Afterwards, the output response (i.e., y-parameters) for each test structure was obtained and compared with measurement data to determine if the statistical variation

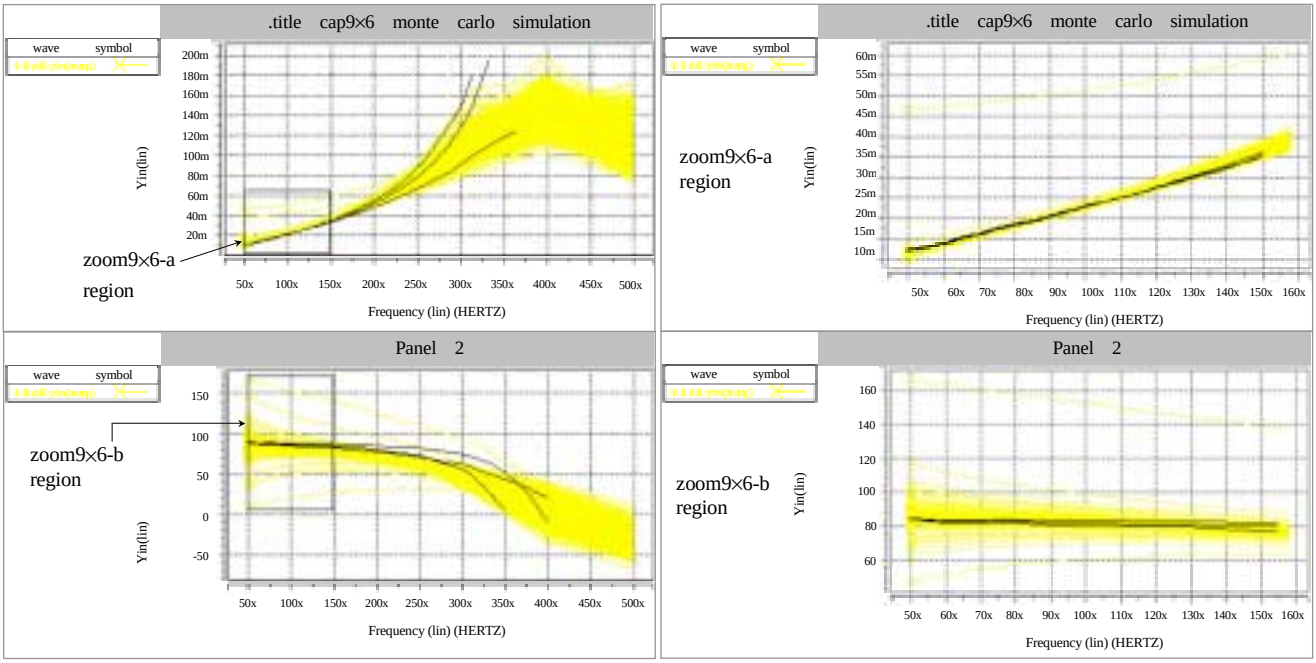


Fig.9. Monte Carlo analysis results for 9x6 test structure: (a) whole optimized region and (b) zoom-in region for behaving as a capacitor.

of model parameter values was in the range of Monte Carlo output.

V. RESULTS AND DISCUSSION

A total of nine gridded parallel plate capacitors (3 each for the 3×3, 5×4, and 9×6 test structures) were fabricated and s-parameter measurements were taken. The measured s-parameter data from one of each size capacitor was used to extract the element values of the partial element equivalent circuit of that size capacitor. This process yielded a unique equivalent circuit model for each size capacitor. After s-parameter data were obtained, the magnitude and phase of the input admittance were calculated.

Once the extraction process was completed, a Monte Carlo analysis was performed on each of the three different test structures using the equivalent circuit models. The summary statistics (i.e., mean and standard deviation) extracted from the nine capacitors were used in the Monte Carlo simulations to create a range of 500 input admittance curves (both magnitude and phase) for each test structure. The measured input admittance curves from each complete test structure were then compared to the curves generated by Monte Carlo analysis to determine if the measured input admittance curve resided in the range of the curves generated by Monte Carlo analysis. The results of this analysis for each of the three test structures are shown in Figs. 7, 8 and 9.

As seen in these plots, even for the small number of test structures investigated, the measured input admittance curves from the fabricated devices were in fact contained in the range of the input admittance curves produced by Monte Carlo simulation. However, in the higher frequency region, the admittance curves from the actual devices were on the borderline of the results of Monte Carlo simulation (shown Figs. 7a, 8a, and 9a).

Most circuit designers are interested in the region where component performance is critical for the capacitance value specified for a given design (shown in Figs. 7b, 8b, and 9a). When a capacitor structure is fabricated, a circuit designer is mostly concerned about the region where the structure behaves strictly as a capacitor. Beyond this region, the structure does not behave strictly as a capacitor because other parasitic effects are involved. As an example, consider the 3×3 capacitor test structure shown in Fig .7. This structure behaves as a capacitor in the frequency ranges between 100 MHz and 700 MHz. Beyond 700 MHz, the test structure does not behave as a capacitor due to inductive and other parasitic effects at the higher frequencies.

Using these comparisons of the measured to Monte Carlo results, it has been demonstrated that the variation in the complete capacitor equivalent circuit models based only on the circuit building blocks can be used to predict such variations in actual fabricated devices.

VI. CONCLUSION

In this paper, an investigation of the statistical variation of parallel plate capacitors with gridded plates manufactured in a multilayer LTCC process has been presented. Since accurate modeling of integrated passive components is critical for designing and characterizing the performance of next generation (MCM) substrates with integral passives, analysis of statistical variation for each circuit model parameter has been performed using the Monte Carlo approach. A comparison of the Monte Carlo results and measured data revealed that even a small number of sample structures provided sufficient statistical variation of component values to allow prediction of the performance variation of a larger population. This method could potentially be extended to allow circuit designers to predict the performance and parametric yield of a given circuit containing such devices.

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