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A Frequency Model of OCXO for Holdover Mode of DP-PLL

DP-PLL의 Holdover 모드에 대한 OCXO의 주파수 모델

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ABSTRACT

A frequency model of an OCXO (Oven Controlled X-tal Oscillator) is suggested to implement a holdover algorithm in a DP-PLL (Digital Processing-Phase Locked Loop) system. This model is presented simply with second order polynomials with respect to temperature and aging of the OCXO. The model parameters are obtained from experimental data by applying the LSM (Least Squared Method). A holdover algorithm is also suggest using the the frequency model. The obtained model is verified to simulate the holdover algorithm with experimental phase data due to variation of temperature.

요 약

OCXO (Oven Controlled X-tal Oscillator)의 주파수 모델이 holdover 알고리즘을 DP-PLL (Digital Processing-Phase Locked Loop) 시스템에 적용하기 위해 제안되었다. 이 모델은 온도와 OCXO의 노화에 따라 2차 다항식으로 간단하게 표현된다. 모델 변수들은 LSM (Least Squared Method)을 적용한 실험 데이터로부터 얻어진다. holdover 알고리즘은 다른 실험 데이터를 사용한 동일한 모델로 모의실험 할 수 있다.

Keywords: DP-PLL, holdover, OCXO, aging, temperature

Ⅰ. Introduction

In digital communication systems such as exchanges, transmission facilities and wireless mobile systems, network synchronization has an influence upon occurrence of slip and bit error rate. DP-PLL systems[1]-[3] are used for accurate network synchronization because they can be designed to have bandwidth of a few μHz using digital signal processing

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while analog PLL systems can not. In the DP-PLL system, furthermore, an OCXO is required to regenerate very accurate clock from a reference clock. A 1 pps signal from a GPS receiver is widely used as the reference clock due to its accuracy of 10^{-11} and its usefulness with no limitation of places.

When failure occurs in the reference clock, the DP-PLL system is operated in holdover mode, where the DP-PLL system should produces a average frequency of the reference clock before its failure. By doing so, the phase error between the reference clock and the OCXO clock is kept to be small. Even though an OCXO is heated by its oven according to external temperature, the frequency of an OCXO is sensitive to external temperature. To obtain good performance with an OCXO in the holdover mode, hence, it is required to compensate external temperature. Also, aging of an OCXO is considered for the good performance.

In operation of the holdover mode, a frequency model of an OCXO is need to computed its frequency variation due to external temperature and the aging. In this paper, a second order polynomial frequency model can be introduced with respect to variation of external temperature since an OCXO is operated in narrow range of temperature by controlling its oven. A holdover algorithm is also proposed using this frequency model. Parameters of the frequency model are found experimentally by applying the least squared method to phase data. To verify obtained model, the holdover algorithm is simulated with experimental phase data of an OCXO under conditions of variation of external temperature.

Ⅱ. Overview of the DP-PLL system

A DP-PLL system is composed of a controller, a VCXO (Voltage Controlled X-tal Oscillator), and a Phase Detector (PD), which are plotted in Fig. 1. An OCXO is used as a VCXO to obtain good performance of the holdover mode. The PD measures phase error between the reference clock and the OCXO clock. The phase error e(t) is counted by a digital counter as shown in Fig. 2. When the

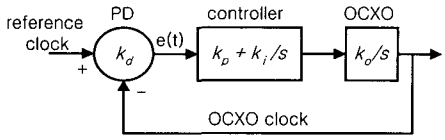

Fig. 1 The block diagram of the DP-PLL.
그림1. DP-PLL의 블록 다이어그램

unit of phase is set to UI (Unit Interval; 1UI=one periodic time of the reference clock) , gain of the PD becomes

$$k_d = f_c / f_r$$

where f_c and f_r are frequencies of the counter clock at the PD and the reference clock, respectively.

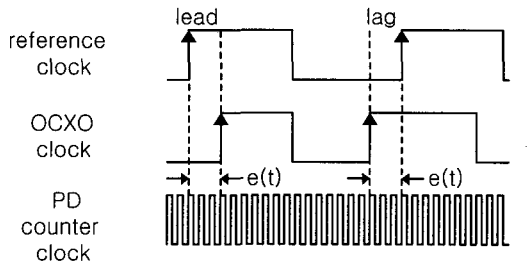

Fig.2 Timing of the PD counter.
그림2. 위상 검출 카운터의 타이밍도

The controller is implemented with a program in a microprocessor and a DAC (Digital Analog Converter) and other electric circuits. In general, proportion and integral control is used[1]-[3]. A control voltage computed from the controller drives the OCXO through the DAC. The DP-PLL system is a composite system

merged with continuous and discrete time. Since a sampling frequency of the DP-PLL system is ten times more than its bandwidth, however, the DP-PLL system can be approximated as a continuous time system for easy analysis. Then, the transfer function of the PI controller becomes

$$C(s) = k_p + \frac{k_i}{s}, \quad (1)$$
$$where \quad k_p = PG \cdot \frac{V_{DAC}}{2^{bit_{DAC}}}, \quad k_i = \frac{1}{\Delta t} \cdot IG \cdot \frac{V_{DAC}}{2^{bit_{DAC}}}$$

where PG and IG are gains of the proportion and the integral control in the control program, respectively. V_{DAC} is output voltage range of the DAC. bit_{DAC} is bit number of the the DAC. Δt is sampling interval of the phase error in the DP-PLL system. The transfer function of the OCXO is represented as k_o/s, $k_o = \Delta f / V_{OCXO}$, where V_{OCXO} is input voltage range of the OCXO, and Δf is frequency deviation range of the OCXO. The transfer function of the DP-PLL system H(s) becomes[4]

$$H(s) = \frac{\alpha s + \beta}{s^2 + \alpha s + \beta}, \quad (2)$$
$$where \ \alpha = k_d \cdot k_p \cdot k_o, \beta = k_d \cdot k_i \cdot k_o$$

The bandwidth and other specificatons of the DP-PLL system can be determined to adjust α and β. The average frequency of the reference clock until present time $t=0$ is computed through the integral controller, k_i/s.

$$V_0 = k_i \sum_{i=-\infty}^{0} e[i] \quad (3)$$

V_0 is the voltage corresponding to the average frequency of the reference clock and $e[i]$ $(i=0,1,2,\cdots)$ are the sampled data of $e(t)$ at time $t = i\Delta t$. In the holdover mode the DAC voltage is updated by adding V_0 to voltage compensated from a holdover algorithm in the microprocessor due to external temperature and the OCXO aging. A thermistor is need as a temperature sensor and it should be attached nearby the OCXO. An ADC (Analog to Digital Converter) is also need to sample external temperature from the thermistor.

III. Model of OCXO for Holdover mode

3.1 OCXO Model and Holdover mode Algorithm

A vibration frequency of a crystal has quite nonlinear relations with temperature. However, variation range of internal temperature in the OCXO is very narrow by the oven in spite of large variation of external temperature. Therefore, frequency model of the OCXO can be approximated simply to be a second order polynomial with respect to external temperature.

$$f(t, T(t)) = f_r + f_d + \int_0^t (a_0 + a_1 T(\tau) + a_2 T^2(\tau))\, d\tau + b_0 + b_1 T(t) + b_2 T^2(t) \quad (4)$$

where $f(t, T(t))$ is the frequency model of the OCXO. $T(t)$ is temperature in the thermistor at time t and f_d is frequency difference between the reference clock and the OCXO clock. a_0, a_1, and a_2 are aging parameters according to external temperature. b_0, b_1, and b_2 are temperature parameters. These parameters differ slightly in OCXO's with same specs. They need to be found from experimental data.

The DAC value, V_0 given as (3), corresponds to the following frequency f_0 of the OCXO;

$$f_0 = V_0 2^{bit_{DAC}} / \Delta f = f_r - f_d, \quad (5)$$

The main reason of $f_d \neq 0$ during the PI control is derived from frequency quantization error of Δf with limitation of the DAC's bits. From the PI control, however, this quantization error is compensated, and DAC values are varied with a certain period to result in generation of jitters in the OCXO clock. The DAC value corresponding to f_d is computed as

$V_d = 2^{bit_{DAC}} f_d / \Delta f < 1$. It is very difficult to find exactly. V_d can be estimated to subtract V_0 from average DAC value for several hours before the holdover mode.

Using the model (4) in operation of the holdover mode, the frequency variation of the OCXO is computed with sampled temperature at the thermistor and elapsed time from the start of the holdover mode. And the DAC value is adjusted to compensate the frequency variation. To implement holdover algorithm, the continuous time model (4) needs to be converted to the following discrete time model at time $t = nt_h$.

$$f[n, T[n]] = f_r + f_d + \sum_{i=0}^{n} (a_0 + a_1 T[i] + a_2 T^2[i]) t_h + b_0 + b_1 T[n] + b_2 T^2[n] \quad (6)$$

t_h is the sampling interval of temperature in the thermistor and $t = 0$ is the start time of the holdover mode. $T[n]$ is temperature sampled from the thermistor and $T_0 = T[0]$ is temperature at the start time of the holdover mode.

The DAC value, $V[n]$, in the holdover mode can be computed from the discrete model (6) with the initial temperature T_0.

$$V[n] = V_0 + V_d - \frac{2^{bit_{DAC}}}{\Delta f} [\sum_{i=0}^{n} (a_0 + a_1 T[i] + a_2 T^2[i]) t_h + (b_0 - b_0) + b_1 (T[n] - T_0) + b_2 (T^2[n] - T_0^2)] \quad (7)$$

b_0 is eliminated and does not need to be found. The only integer part of $V[n]$ is transmitted into the DAC owing to its bit limitation. For the accurate compensation, several numbers of $V[n]$ below point should be taken into account. If t_m is the minimum interval in which the microprocessor can write data to the DAC, there are L opportunities to write data to the DAC, where L is the integer part of t_h / t_s. Let the integer part of $V[n]$ and $L \times |V[n] - N|$ be set to N and M, respectively. A bit leaking method is introduced to reduce error of the DAC value below $1/L$. That is, DAC N + signum of $(V[n] - N)$ is written M times and N is written L-M times during the interval t_h. Also, if N + signum of $(V[n] - N)$ and N are written with the most regular order possible, average DAC value for very short interval can be made to be near $V[n]$.

3.2 Estimation of OCXO Model Parameters

The frequency deviation of the OCXO from its aging is much smaller than those from external temperature variation. The aging parameters need to be obtained from experimental data without variation of temperature. Aging data of the OCXO are acquired under conditions of a constant DAC value and a specific temperature in the chamber. Frequency difference between the reference clock and the OCXO clock is computed from phase data sampled at the PD.

$$\Delta f_{T_0}[n, T[n]] = \frac{e[n] - e[n-1]}{t_h} \quad (8)$$

$\Delta f_{T_0}[n, T[n]]$ is the frequency difference at time $t = nt_h$ and $T[n] = T_0$ is the specific temperature sampled from thermistor. Considering the constant temperature T_0 in the chamber, from the model (6) $\Delta f_{T_0}[n, T[n]]$ can be represented as;

$$\Delta f_{T_0}[n, T[n]] = f_d + nt_h\, a, \quad (9)$$

$$a \equiv a_0 + a_1 T_0 + a_2 T_0^2. \quad (10)$$

a and f_d can be found to apply the LSM (Least Square Method)[5] from the following object function, $G_1(f_d, a)$, with K sampled data;

$$G_1(f_d, a) = \sum_{i=1}^{K} (f_d + a\ it_h - \Delta f_{T_0}[i, T[i]])^2 \quad (11)$$

From three different values of T_0, three corresponding values of a can be obtained from (11). And then, $a_i(i=0,1,2)$ are computed from them by using simultaneous equation (10).

Experimental data for detection of $b_i(i=1,2)$ are acquired under conditions of a constant DAC value and variation of temperature in the chamber. The frequency difference, $\Delta f_{T_0}[n, T[n]]$, are also computed from these data with (8). Using the obtained $a_i(i=0,1,2)$, frequency variation according to the aging can be eliminated from $\Delta f_{T_0}[n, T[n]]$. The pure frequency difference, $\overline{\Delta f_{T_0}}[n, T[n]]$, according to variation temperature becomes

$$\overline{\Delta f_{T_0}}[n, T[n]] = \Delta f_{T_0}[n, T[n]] - \sum_{i=0}^{n}(a_0 + a_1 T[i] + a_2 T^2[i]) t_h \quad (12)$$

where $T_0 = T[0]$ is the initial start temperature. Taking account of initial frequency of the OCXO at the initial temperature T_0, the frequency variation according to temperature variation is represented as $\overline{\Delta f}[n, T[n]]$;

$$\overline{\Delta f}[n, T[n]] = f_d + b_0 + b_1 T[n] + b_2 T^2[n] - (b_0 + b_1 T_0 + b_2 T_0^2) \quad (13)$$

b_0 is eliminated naturally. b_1, b_2 and f_d can be found from the following object function, $G_2(f_d, b_1, b_2)$, by the LSM.

$$G_2(f_d, b_1, b_2) = \sum_{i=2}^{K}(f_d + b_1(T[i] - T_0) + b_2(T^2[i] - T_0^2) - \overline{\Delta f}[i, T[i]])^2 \quad (14)$$

Ⅳ. Experimental Identification of OCXO model

A DP-PLL unit was implemented for experiments to identify the frequency model (6). The reference clock in the DP-PLL unit was a 1 pps (pulse per second; f_r =1Hz) clock filtered off jitters from a 1 pps signal of a GPS receiver with a HP equipment. The OCXO in the DP-PLL unit had center frequency of 10MHz with deviation range of $\pm 0.5\times 10^{-6}$. Its frequency aging range was $\pm 2\times 10^{-10}$/day and its frequency stability was $\pm 3\times 10^{-10}$ from 0℃ to 70℃. The frequency of the PD counter clock was f_c=19.6608MHz, which counted the phase difference between 1 pps and the OCXO clock divided by 10×10^6. A Motorola 68302 microprocessor and a 12-bit DAC (bit_{DAC}=12) were used in the unit. A thermistor and a 12-bit ADC were also used to sample external temperature.

The DP-PLL unit was experimented in a champer to change external temperature. Because of heat generated from DP-PLL unit by itself, there was temperature difference of 6℃~8℃ between the chamber and the thermistor on the DP-PLL unit. To make the frequency difference, f_d, small in all experiments, the OCXO clock of the DP-PLL unit was synchronized to the reference clock by the PI control for one day with keeping a initial temperature. And experimental data were acquired for 32 hours after DAC value was fixed to V_0 of (3) resulting from the PI control. The sampling interval t_h was 30sec.

Phase data for the aging parameters $a_i(i=0,1,2)$ were acquired from three experiments where each temperature of the chamber was 0℃, 20℃, and 40℃. The experimental data at the temperature of 20℃ are plotted in Fig. 3. The aging parameters were found to be $a_0 = -2.5474\times 10^{-10}$Hz/day, $a_1 = 5.3474\times 10^{-13}$ Hz/℃/day, and $a_2 = 1.2422\times 10^{-13}$Hz/ ℃^{2}/day. The phase variation data according to the aging were computed with the obtained aging parameters and elapsed time in case of 20℃ in chamber. And errors between them and the experimental phase data at 20℃

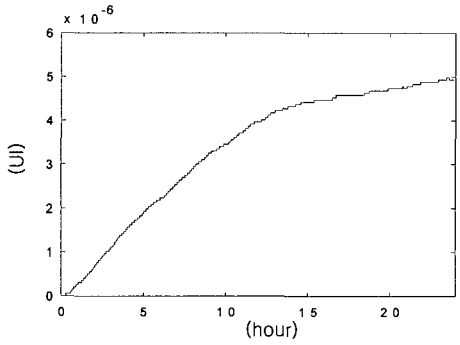

Fig.3 The experimental phase data with keeping 20℃ in the chamber.

그림 3. 챔버에서 20℃ 유지시 위상 실험 데이터

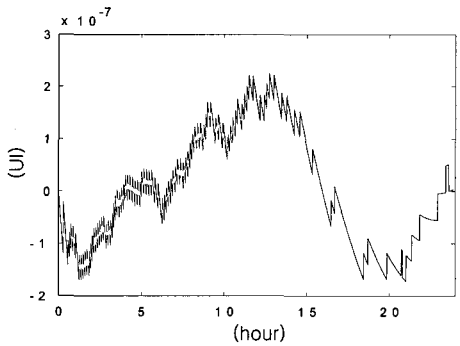

Fig.4 The errors between the experimental phase data of 20℃ and the phase data computed with the aging parameters.

그림4. 20℃의 위상 실험데이터와 에이징 파라미터들로 계산된 위상 데이터 사이의 에러

are plotted in Fig. 4.

To acquire experimental data for the parameters $b_i(i=1,2)$, temperature at the thermistor was varied like Fig. 5. The experimental phase data are shown in Fig. 6.

The aging effect was eliminated from the experimental phase data with the obtained aging parameters. The temperature parameters were found to be $f_d=9.0795\times10^{-11}$Hz, $b_1=-1.3369\times10^{-10}$Hz /℃, and $b_2=6.3302\times10^{-13}$Hz/ ℃^{2} by using the object function (14).

Using the obtained parameters, $8a_i(i=0,1,2)$, $b_i(i=1,2)$, and f_d, estimated phase data were computed with the temperature data in Fig. 5 and elapsed time. The difference between the estimated and the experimental phase is plotted in Fig. 7. Also, f_d was estimated to be 1.3439×10^{-10}Hz from the average DAC value for 8 hours before fixing DAC value to V_0 of (3). In computation of phase data with the frequency model, the estimated f_d is used instead of f_d obtained from (14). And the difference is also plotted in Fig. 7, which shows that more phase error can be introduced in the holdover mode by using f_d

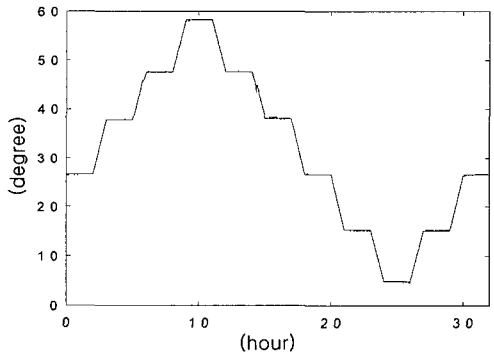

Fig.5 The data of temperature variation with the initial 20℃ temperature.

그림5. 초기온도 20℃일 때 온도변화 데이터

estimated from average DAC value.

The holdover algorithm (7) was simulated with the identified model using another experimental data under condition of temperature variation as seen in Fig. 8. The phase data of the experiment are plotted in Fig. 9, where $f_d=1.4248\times10^{-10}$Hz was estimated from the average DAC value for 8 hours before fixing DAC value to V_0 of (3) which resulted from the PI control.

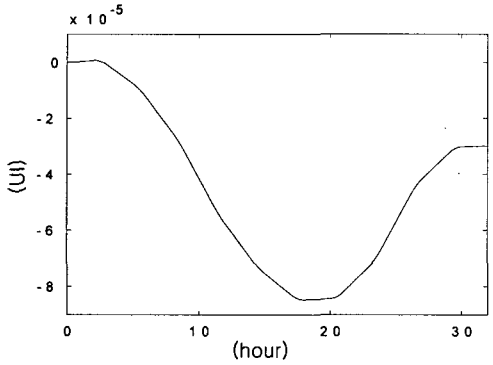

Fig.6 The experimental phase data by temperature variation with 20℃ initial temperature

그림6. 초기온도 20℃일 때 온도변화에 의한 위상 실험 데이터.

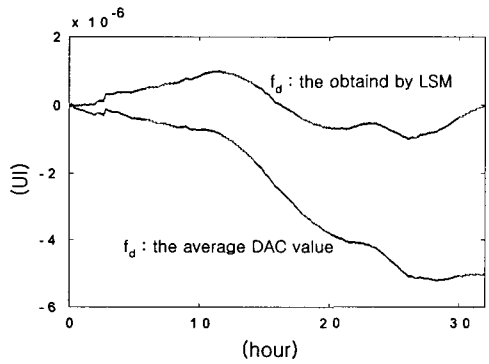

Fig.7 The phase difference between the experimental phase and the phase computed by the OCXO model with 20℃ initial temperature.

그림7. 초기온도 20℃일 때 OCXO 모델의 실험에 의한 위상과 계산된 위상 사이의 위상차.

The phase data were computed by using the identified model, and errors between the computed phase and the experimental phase are shown in Fig. 10.

V. Conclusion

For holdover algorithm of DP-PLL systems, the frequency model of the OCXO was suggested considering both of external temperature and the aging. This model is represented as the simple second order polynomial with respect to temperature. The holdover algorithm was also proposed from the frequency model. the LSM was used to identify the frequency model. The parameters of the frequency model of an OCXO were obtained experimentally and the usefulness of the model were validated by the simulation of the holdover algorithm.

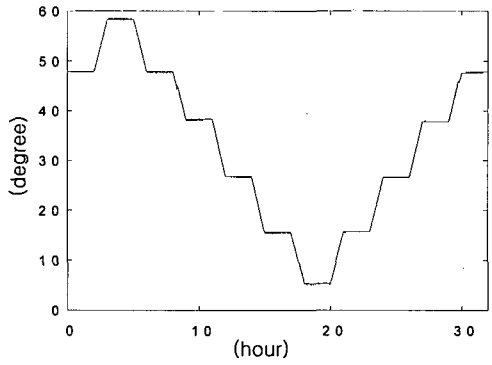

Fig.8 The data of temperature variation with the initial 40℃ temperature.

그림8. 초기온도 40℃일 때 온도변화 데이터.

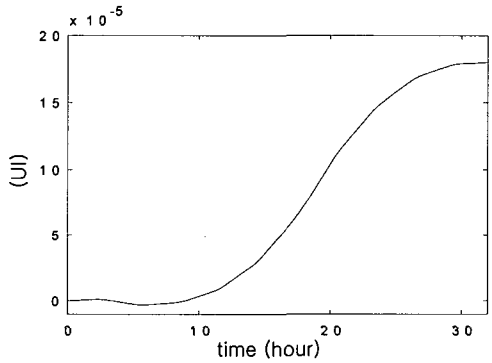

Fig.9 The experimental phase data by temperature variation with 40℃ initial temperature.

그림9. 초기온도 40℃일 때 온도변화의 위상 실험 데이터

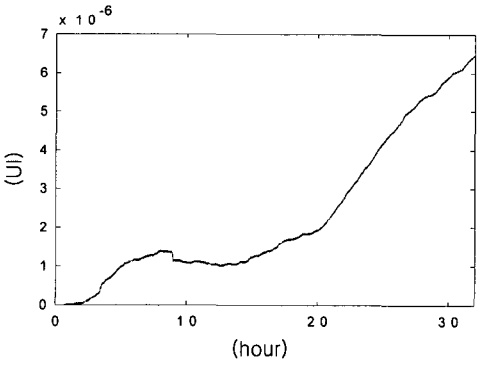

Fig.10 The phase difference between the experimental phase and the phase computed by the OCXO model with 40℃ initial temperature.

그림10. 초기온도 40℃일 때 OCXO 모델의 실험에 의한 위상과 계산된 위상 사이의 위상차

Further work is continuing to apply the holdover algorithm to the DP-PLL unit experimentally.

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VI. References

[1] E. A. Munter, "Synchronized clock for DMS-100 family," IEEE Trans. Commun., vol. 28, no. 8, pp. 1276-1284, August 1980.

[2] H. Fukinuki and I. Furukawa, "Intelligent PLL using digital processing for network synchronization," IEEE Trans. Commun., vol. COM-31, no. 12, pp. 1295-1303, December 1983.

[3] R. Metz, E. L. Reible, and D. F. Wnchel, "No. 4 ESS: Network clock synchronization," Bell System Technical Journal, vol. 60, no. 6, pp. 1109-1128, July-August 1983.

[4] R. E. Best, Phase Locked Loops: Design, Simulation and Applications, third edition, New York: McGraw-Hill, 1997.

[5] T. Soderstrom and P. Stoica, System Identification, Prentice-Hal, 1989.

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