Wall Charge Measurement in the Address Period of AC Plasma Display Panel

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Abstract

The relationship between driving voltage and the amount of wall charge in the address period of surface discharge type AC Plasma Display Panel has been investigated. The amount of wall charge on each electrode is obtained simultaneously from the current profiles after applying only one addressing discharge pulse. The wall charge Q_y on the scan electrode Y is almost the sum of Q_x on the address electrode X and Q_z on the sustain electrode Z. The Q_y increased with the driving voltage regardless of the kind of electrode, whereas the addressing T_d decreased. The Q_z and Q_y are increased considerably by blocking voltage V_z, whereas Q_x is decreased. The V_Z dependence of Q_x, Q_y and Q_z in addressing discharge was -13 × 10^{-2} (pc/V_z), and 60 × 10^{-2} (pc/V_z) and 70 × 10^{-2} (pc/V_z), respectively.

Keywords : AC PDP, wall charge, address period, addressing

1. Introduction

The amount of wall charge on each electrode has been measured in the address period of ac plasma display panels (PDP). A major motivation of this work is to provide a clear understanding of the wall charge condition on each electrode after addressing micro-discharge as parameters of the voltage on three electrodes of ac PDP, and to get the experimental data on which the detailed driving voltage can be based in the address period of ADS (address-display separating) method [1-3]. The addressing time T_d is also measured in order to define the relationship between the addressing time and the voltage parameters.

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2. Experimental

Fig. 1 shows the schematic diagram of 4 inch ac PDP model and Table 1 shows its specifications. The electrode arrangement is shown in Fig. 2. A single discharge cell has also three electrodes. Electrodes X, Y and Z are address electrode, scan and sustain electrode, and sustain electrode, respectively. In ADS method, one frame is divided into 8 subfields and each subfield consists of reset period, address period, and sustain period.

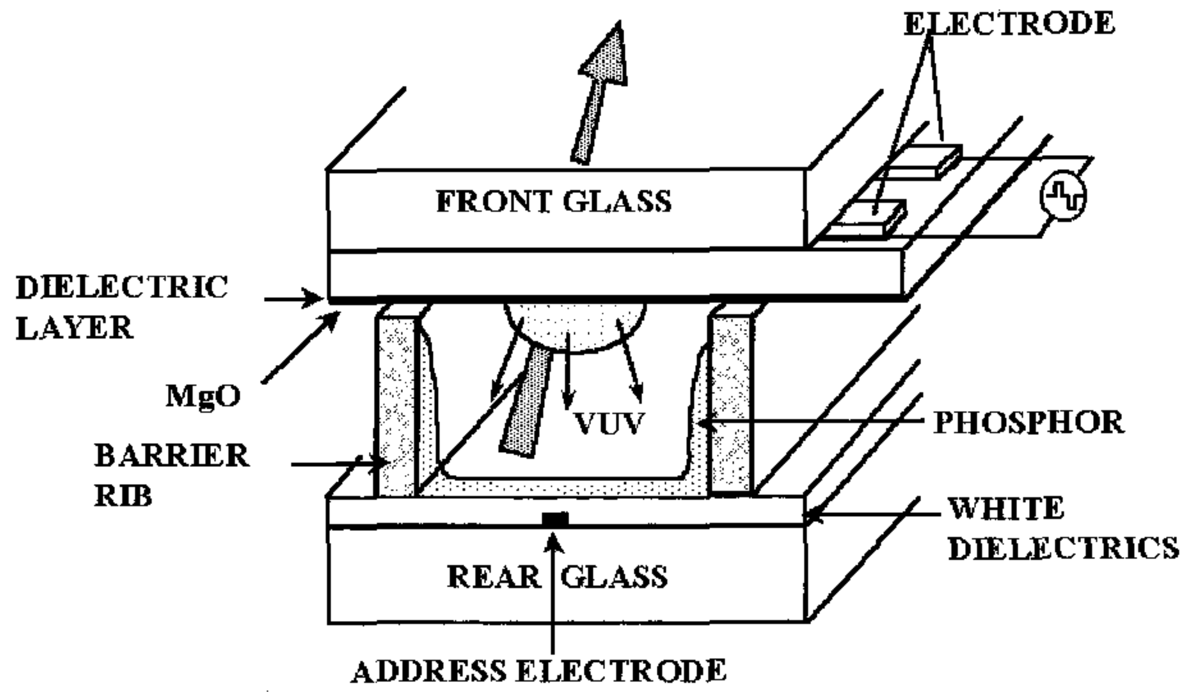

Fig. 1. The schematic diagram of surface disc harge type ac PDP.

TABLE 1. Spec. of 4-in ac PDP

Front panel		Rear panel	
ITO width	310㎛	Add width	100㎛
ITO gap	60㎛	White back thickness	15㎛
Bus width	100㎛	Rib height	150㎛
Dielectric thickness	25㎛	Rib pitch	360㎛
MgO thickness	5000Å	Rib width	70㎛
		Phosphor thickness	20㎛

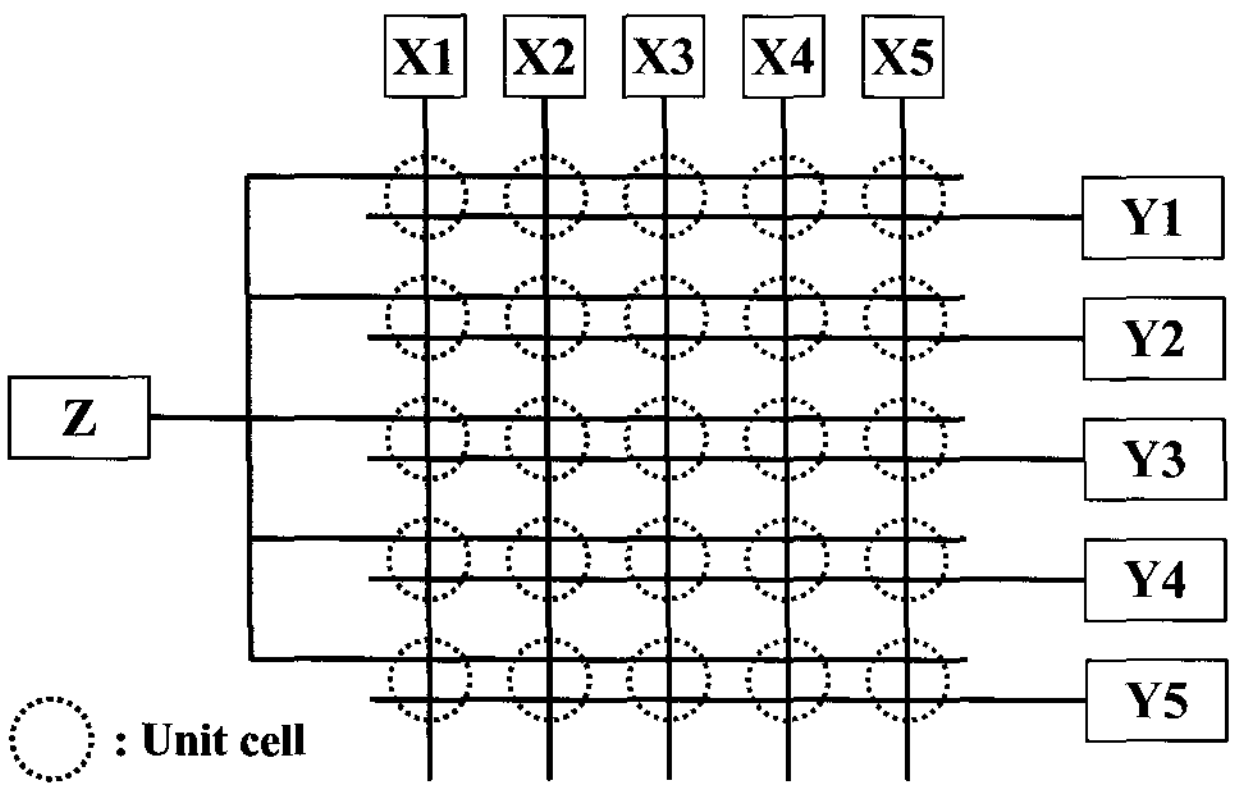

Fig. 2. The electrode arrangement in ac PDP

TABLE 2. The conditions of applied voltage.

V_y	-150V
V_y_scan base	-50V
V_x	100V
V_z	40V
V_z_reset	350V
V_s_sustain & swing	130V

Fig. 3 shows the driving scheme in this work to drive the 4 inch panel using only one addressing pulse. A previous image is to be cleared in reset period. In address period, address discharge is seen to occur between X and Y. The generated charges are distributed on the three kinds of electrodes. The distributed charge called as wall charge plays an important role in the making of the image. The well-distributed wall charge makes the exact clear image in the sustain period. In Fig. 3, the sum of reset and address period is 1.2㎳, and one subfield time is 2㎳. The wall charges at each electrode are detected from the current of each electrode after an address discharge [4-5].

Fig. 4 shows the schematic diagram of measurement system. The quartz glass diameter of a view point is 200㎜. By this system, the kinds of working gas and pressure can be controlled. In this work, He+Ne(30%)+Xe(4%) gas of 400 torr is used after back pumping of 10^{-8}torr by molecular pump. The current wave is detected by 4ch digital storage oscilloscope. The experimental parameters are the electrode voltage V_x, V_y, and V_z of X, Y, and Z electrodes in the address period. The reference values of the parameters are shown in Table 2, which are typical values in real ac PDP. The

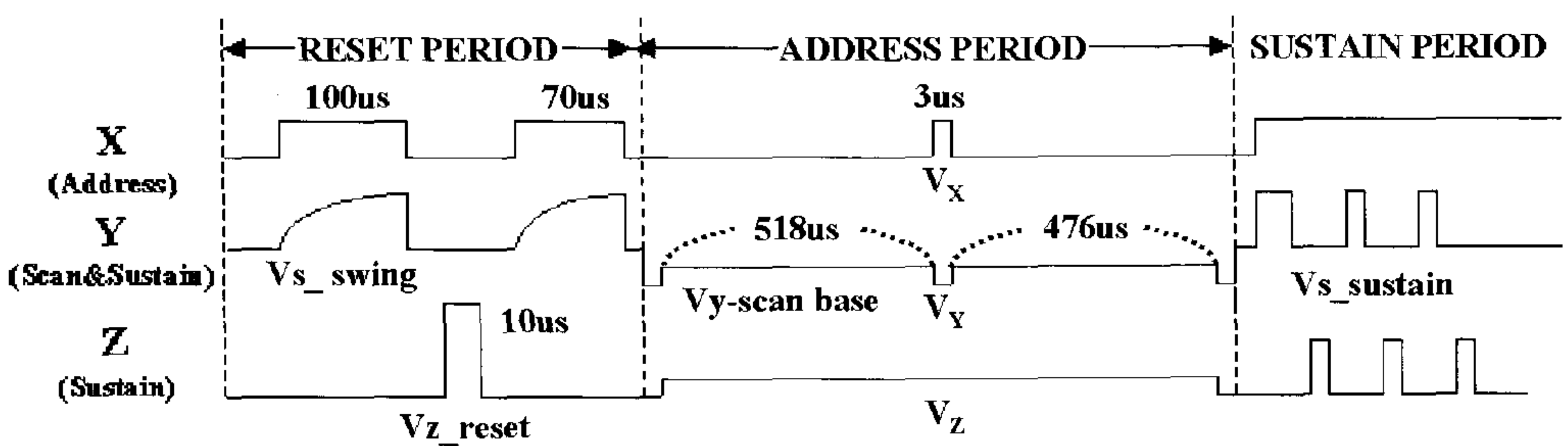

Fig. 3. The driving scheme with only one addressing pulse.

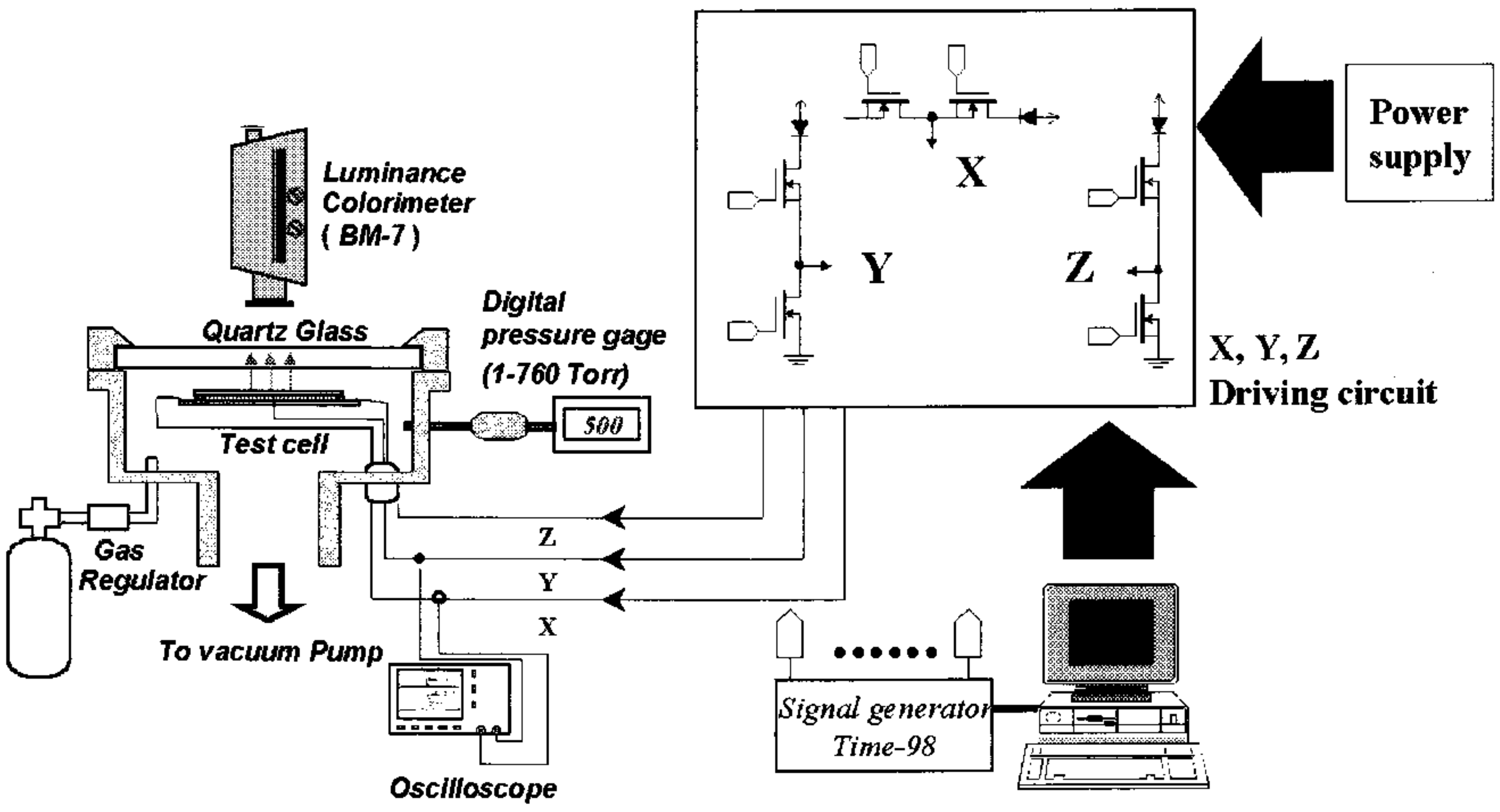

Fig. 4. The schematic diagram of measurement system.

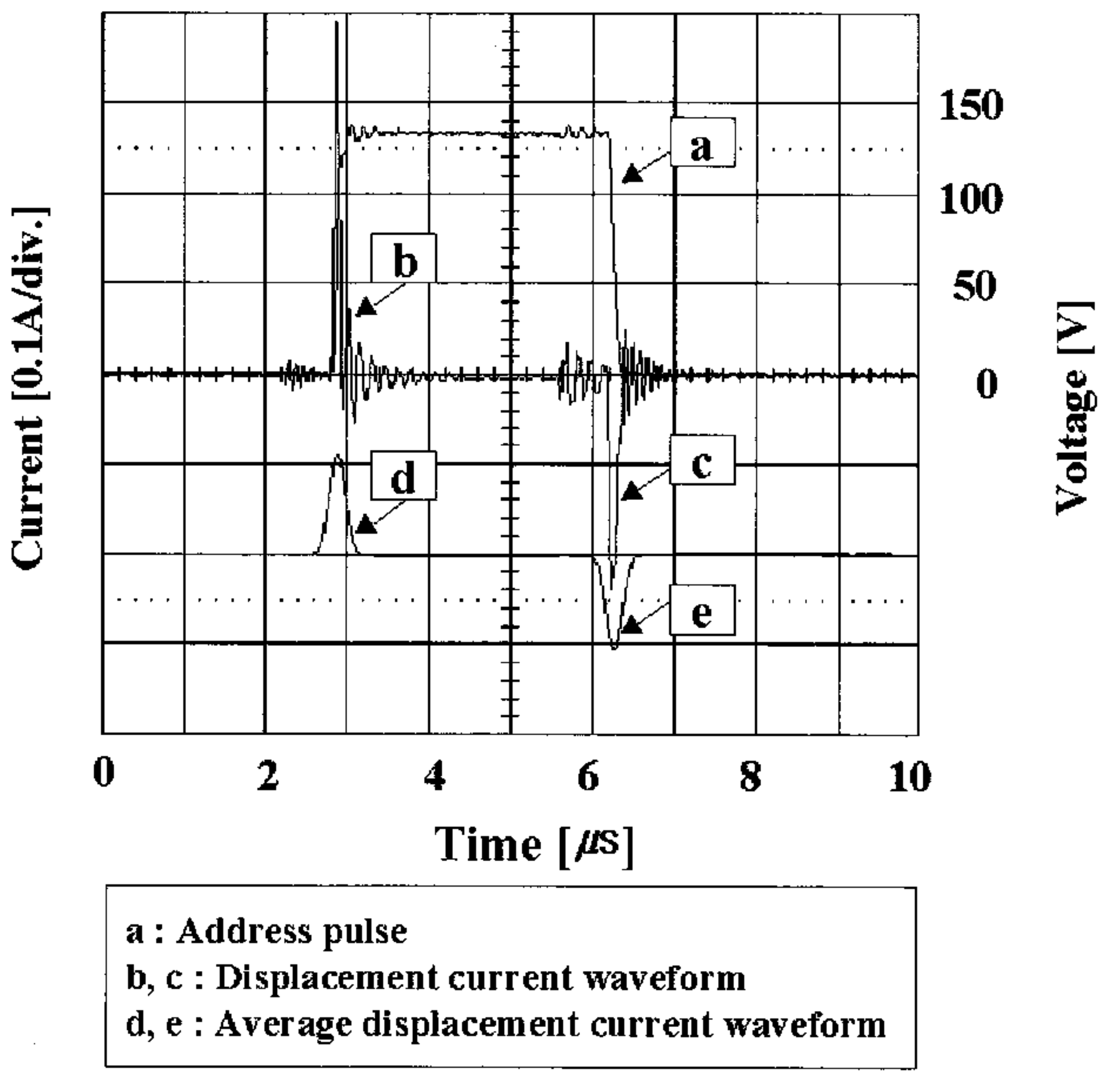

Fig. 5. The address pulse and displacement current waveform.

parameters V_x and V_y are varied in the range of $60 \leq V_x \leq 120$ and $130 \leq |V_y| \leq 160$, respectively, which is the possible range of addressing without reverse discharge.

The V_z value is varied in the range of $15 \leq V_z \leq 60$, which is the possible range of addressing without surface discharge between X and Z electrode in the address period [6]. A given parameter is varied under the condition of constant value of the Table 2 for other parameters.

3. Results and Discussion

Fig. 5 shows the address pulse with about 3μs width (pulse rising time: ~150ns, a in Fig. 5) and displacement current waveform (b and c in Fig. 5) and the average displacement current wave form (d and e in Fig 5). The oscillation parts of b and c curves may be due to the distribution parameters of R-L-C of the panel and driving circuits.

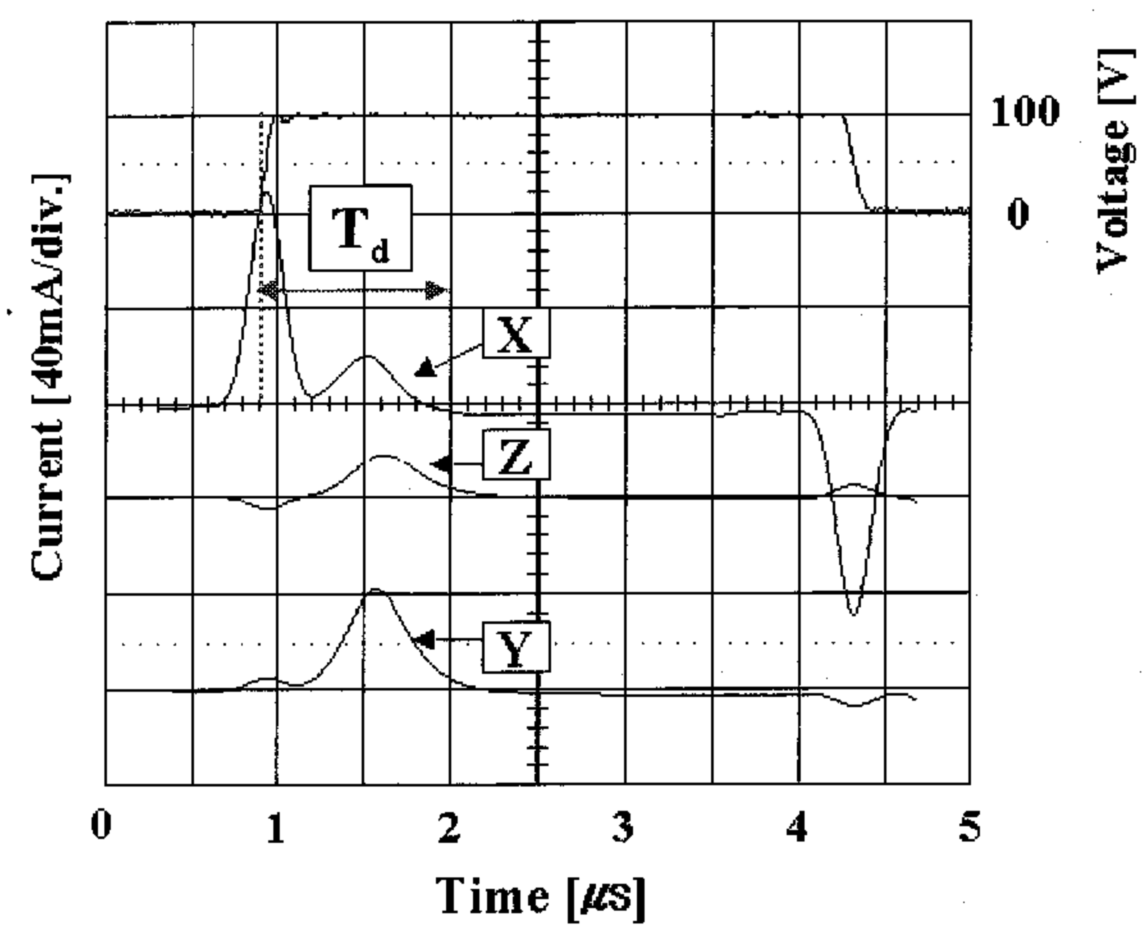

Fig. 6. The current waveforms of X, Y amd Z electrodes after an addressing discharge.

Fig. 6 shows the address pulse, and the current waveforms I_x, I_y, and I_z of X, Y, and Z electrodes, respectively, after the addressing discharge. The first part of the current waveforms are the displacement current, and 2nd part I_x, I_y, or I_z correspond to the discharge

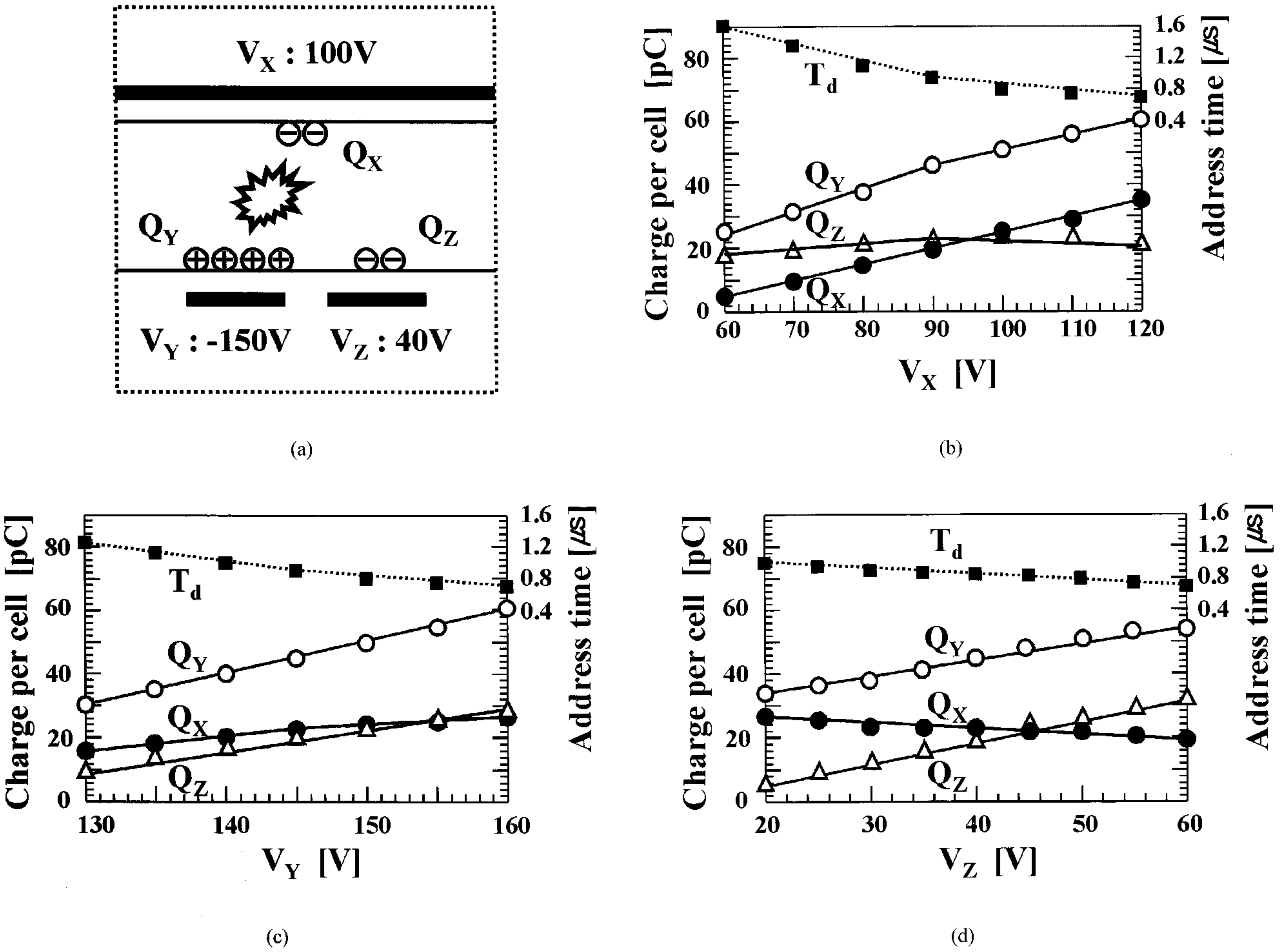

Fig. 7. Schematic charge distribution and the characteristics of Q_X, Q_Y, Q_Z and T_d as a parameter of V_X, V_Y and V_Z (a) schematic charge distribution (b) parameter V_X (c) parameter V_Y (d) parameter V_Z

current by the addressing discharge. Since V_y is negative and V_x and V_z are positive values, the following relationships can be obtained from Fig 6, that is

$$I_y \doteqdot I_x + I_z \quad \text{or} \quad Q_y \doteqdot Q_x + Q_z \qquad (1)$$

Q_x and Q_z are composed of negative electrons and Q_y is composed of positive ions. Therefore, the electrons in discharge space should be divided into two parts, that is Q_x and Q_z.

Since the diffusion loss of electrons is higher than the ion in the discharge space, the Q_y is at most 10% higher than the sum of $Q_x + Q_z$. In Fig. 6, T_d is the addressing time. T_d means that the sum of discharge time lag and discharge sustaining time. The decrease in the addressing time T_d may be due to the decrease in the discharge time lag. The discharge time lag arises from the following two conditions which must be simultaneously satisfied in order for an address discharge to occur in gas [7-8]. First, there should be at least one suitably located free electron in a gas. Secondly, the electric field must be of sufficient strength and a sufficient time should be taken to ensure that this electron produces a sequence of avalanche, which leads to addressing discharge. If the Vx, Vy or Vz are increased, the electric fields among the X, Y and Z electrodes are also increased. Therefore, the T_d can be decreased by the second condition.

After the addressing pulse is applied, the surface discharge occurs between Y and Z electrodes by the triggering discharge between X and Y electrodes. And then, the charge occurred by those discharge forms the wall charge. Therefore, the amount of wall charge depends on the electric field by applied voltage.

Fig. 7(a) shows a typical schematic diagram of charge distribution and the characteristics of Q_x, Q_y, Q_z and T_d as a parameter of V_x, V_y and V_z after addressing discharge between X and Y electrodes [9]. The gap between X and Y electrodes is made by barrier ribs.

Fig. 7(b) shows the characteristics of Q_x, Q_y, Q_z and T_d as a parameter of V_x. Q_x and Q_y increase with V_x, whereas Q_z maintains almost a constant value. The increase rates of Q_x, Q_y and Q_z are 52 $\times10^{-2}$(pc/V_x), 50 $\times10^{-2}$(pc/V_x), and $\pm8\times10^{-2}$ (pc/V_x) for a cell, respectively.

If the V_x is increased, strong address discharge is seen to occur between X and Y electrodes, which lead to generate more charges in the discharge space and in turn decreasing T_d. Furthermore, the ratio of V_x to V_z increases with V_x. As a result, Q_x increases with V_x, whereas Q_z maintains almost constant values. It can also be seen that the correlation between V_z and V_x (or Q_x) is very week because of the discharge space between them. Q_y is also increased with V_x because of equation (1).

Fig. 7(c) shows the characteristics of Q_x, Q_y, Q_z and T_d as a parameter of V_y. All of the Q_x, Q_y and Q_z are increased with V_y. The increase rates of Q_x, Q_y and Q_z are 40×10^{-2}(pc/V_y), 110×10^{-2} (pc/V_y) and 64×10^{-2} (pc/V_y) for a cell, respectively. But T_d was decreased. In particular, the increase rate of Q_z is higher than Q_x, even if V_x and V_z are maintained constant values. If the V_x increases instead of V_y, the same addressing discharge may occur. However, the charge distributions as a parameter of V_x or V_y are very different. The reason may be explained as follows.

Here, the most important point to consider is how the electron charges in the discharge space are distributed on the two electrodes X and Z. In the case of increase in V_x as shown in Fig. 7(b), the total charge in the space increases. Moreover, the ratio of V_x to V_z increases with V_x. Furthermore, the correlation between V_x and Q_z (or V_z) is very weak. Therefore, Q_x increases with V_x, whereas Q_z remains almost constant. In the case of the increase in V_y, as shown in Fig. 7(c), the total charges also increase because of increase in the electric field between Y-X electrodes. However, the electric field between Y-Z electrodes also increase more than that of Y-X electrodes, because Y-Z electrodes are in the same dielectrics of front panel and their gap is shorter than Y-X electrodes. So, V_y affects both X and Y electrodes. Therefore, Q_x and Q_z are increased with V_y, and the increase rate of Q_z is higher than Q_x.

Fig. 7(d) shows the characteristics of Q_x, Q_y, Q_z and T_d as a parameter of V_z. In this case, Q_z and Q_y are increased with V_z, while Q_x and T_d are decreased. The increase rate of Q_x, Q_y, Q_z are -13×10^{-2} (pc/V_z), 60×10^{-2} (pc/V_z) and 70×10^{-2} (pc/V_z) respectively for each cell. These results may be explained as follows. If the V_x increases, the electric field between Z-Y electrodes increases. In addition, the electric field between X-Y electrodes is also somewhat affected by V_z. However, the correlation between V_z and V_x is very weak as mentioned in Fig. 7(c). Therefore, the total charges increase with V_z, whereas T_d decreases. Furthermore, the ratio of V_z to V_x increases with V_z. In the result, Q_z increases sharply with V_z, whereas Q_x decreases with V_z.

The V_x, V_y and V_z are correlated with each other to accumulate the optimum wall charge in the address period. We believe that the optimum wall charge condition in address period may be considered as a condition under whose the charge made on the next first sustain pulse is the same with that made in the stable sustain period.

Fig. 8 shows the effect of V_z on the sustain discharge current. The sustain discharge current increases with V_z. The high discharge current leads to stable sustain operation fast. From this figure, the amount of charge in stable sustain period was about 102[pC/cell], and the voltage of V_x, V_y and V_z under which the charge on the first sustain pulse was the same as that of the stable sustain period were about 100V, -150V and 40V, respectively.

Until now, we have discussed the wall charge distribution as parameters of three kinds of electrode voltages. And it is assumed that the electrodes have no wall charge before address period.

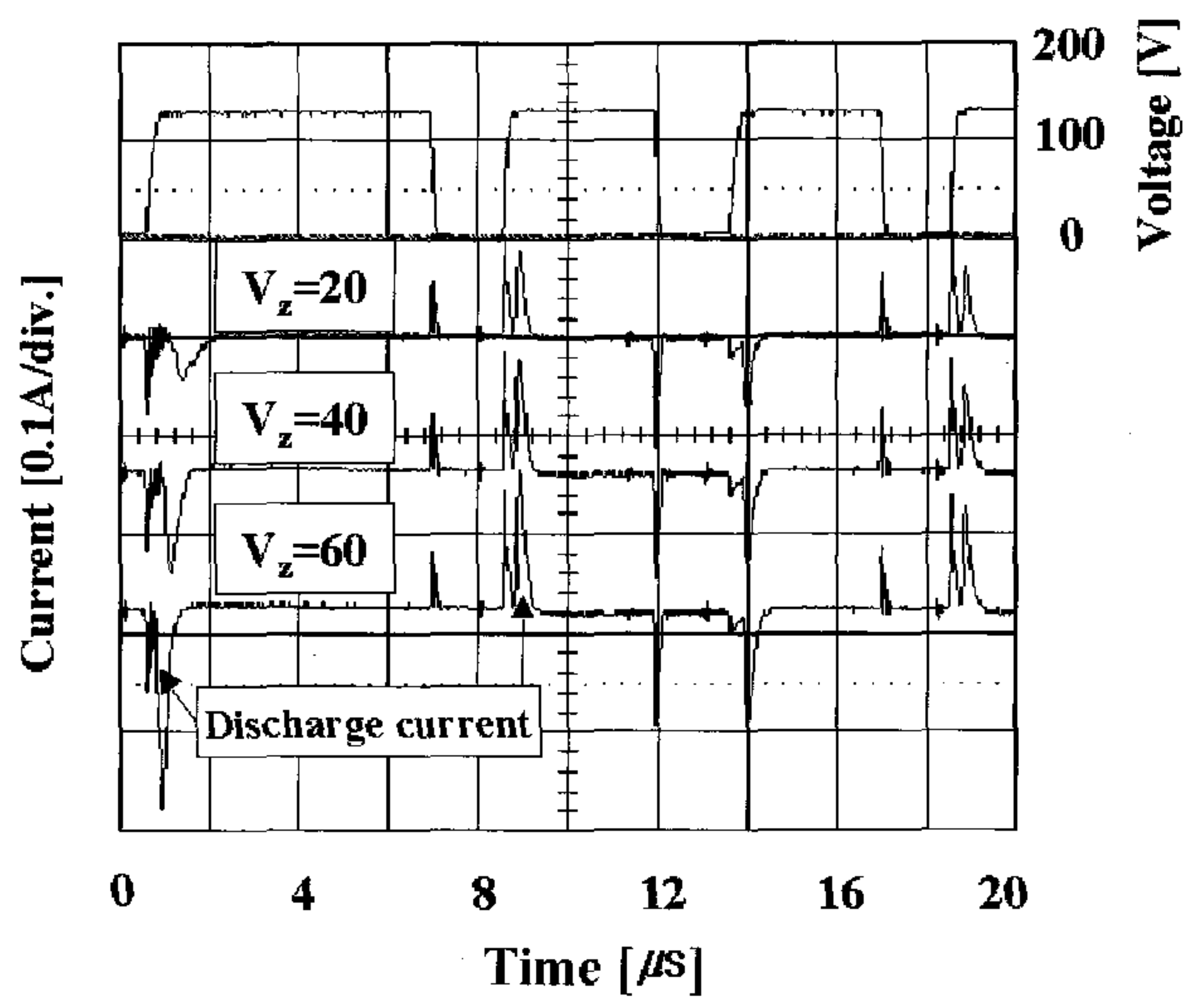

Fig. 8. The sustain current waveform as a parameter of V_z

In real PDP, Q_y and Q_z should be increased, whereas T_d should be decreased in the address period, because these conditions lead to lower address mistakes, sustain misfiring and the addressing time. In order to meet these conditions, the voltage V_x, V_y and V_z should be controlled. However, the increase in V_x or V_y leads to increase in the driving circuit cost by demanding high voltage and high capacity monolithic IC. Furthermore, too high V_y and V_z are apt to lead surface misfiring between Y-Z electrodes in the address period. Therefore, in order to decide the detailed driving voltages in real PDP, both the characteristics of the wall charge distribution and the constraint conditions on the driving voltages from the viewpoint of the driving circuit element cost should be considered.

4. Conclusion

In this work, the relationships between the amount of wall charge and the driving voltage have been investigated in the address period of AC PDP. The results may be summarized as follows.

1) The Q_y is increased with the driving voltage regardless of the kind of the electrode voltage, whereas the addressing time T_d decreased.

2) The Q_x is increased with V_x, whereas Q_z maintains almost constant.

3) Both Q_x and Q_z are increased with V_y and the increase rate of Q_z is higher than Q_x.

4) Q_z is increased considerably with V_z, whereas Q_x is decreased.

5) The Q_y and Q_z increase with increasing the V_y and V_z in the address period. And a lot of Q_y and Q_z leads to stable sustain operation fast. However, the optimum voltage of V_y and V_z may be about −150V and 40V, respectively.

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