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비동기 라이브러리 설계와 Heterogeneous시스템을 위한 인터페이스 설계

(Design of Asynchronous Library and Implementation of Interface for Heterogeneous System)

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요 약

비동기 로직 회로 설계를 위한 라이브러리와 heterogeneous 시스템을 위한 인터페이스 회로를 0.25um CMOS 기술을 사용하여 설계하였다. 그리고 heterogeneous 시스템에는 1.6GHz로 동작을 하는 고속 비동기 FIFO 회로를 사용하였다. 또한 Top-down ASIC 설계를 지원하기 위하여 비동기 기본 셀 레이아웃과 Verilog 모델들을 설계하였다. 본 논문에서는 클럭 skew에 관하여 병목현상을 줄일 수 있는 방법을 제시하였으며 클럭 제어 회로를 사용하여 동기식 회로에서 자주 발생하는 에러를 줄을 수가 있다. 이와 같이 클럭 제어 회로와 FIFO (First-In First-Out) 를 사용하여 다른 주파수로 동작하는 두개의 모듈간의 고속의 데이터 전송을 가능하게 하였으며, 32비트 인터페이스 칩의 코어 사이즈는 1.1mm×1.1mm 이다.

Abstract

We designed asynchronous event logic library with 0.25um CMOS technology and interface chip for heterogeneous system with high-speed asynchronous FIFO operating at 1.6GHz. Optimized asynchronous standard cell layouts and Verilog models are designed for top-down design methodology. A method for mitigating a design bottleneck when it comes to tolerate clock skew is described. This communication scheme using clock control circuits, which is used for the free of synchronization failures, is analyzed and implemented. With clock control circuit and FIFO, high-speed communication between synchronous modules operating at different clock frequencies or with asynchronous modules is performed. The core size of implemented high-speed 32bit-interface chip for heterogeneous system is about 1.1mm×1.1mm.

I. INTRODUCTION

As microprocessor performance moves into the GHz speed, the high-speed asynchronous design is becoming challenge due to the disadvantageous power and speed aspects in synchronous designs. Asynchronous circuit design techniques in both system level and circuit level attract a lot of attentions in recent years. System timing in asynchronous circuit, which is absence of the global clock, is performed by the elements themselves[1],[5]. The next-generation on-chip systems will consist of multiple independently synchronous modules and asynchronous modules for higher performance. To perform high-speed communication between

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several synchronous modules operating at different clock frequencies or with asynchronous modules, a reliable communication scheme is needed.A communication scheme using the PCC(Pausible Clocking Control) circuits is one method to communicate with the synchronous modules via asynchronous FIFO(First-In First-Out) communication channels[2]. Fig.1 shows this communication scheme with the handshake protocol [3].

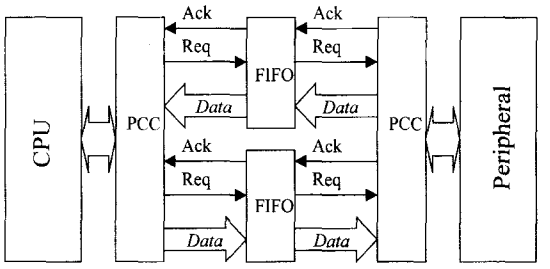

그림. 1 PCC 와 FIFO 를 이용한 통신 구조
Fig. 1. Communication scheme with PCC and FIFO.

It is unnecessary to consider the communication delay between blocks using asynchronous handshaking. In order to develop compatibility and usability of circuit design, we designed asynchronous event logic library that is useful to perform handshake protocol effectively. This library includes physical layout elements and verilog timing models for top-down design methodology. Using this library, we implement high-speed asynchronous FIFO and interface chip on ASIC 0.25um CMOS chip. This FIFO operates at 1.8GHz and two separated modules can communicate with each other via FIFO.

The rest of this paper is organized as follows. Section 2 reviews asynchronous library, key components used in asynchronous design. Section 3 describes the design and implementation of FIFO and interface circuit unit for heterogeneous system. Section 4 describes the simulation results. Section 5 concludes the paper with some remarks on the future system design.

Ⅱ. ASYNCHRONOUS LOGIC LIBRARY

Asynchronous logic library that is used in AMULET[4] is generated with 0.25um CMOS process. This library includes optimized cell layout with 8.8um-height and verilog timing model for the back-end and front-end design, respectively. The cell height is calculated as 10 tracks multiplied 10 by 0.88um that is one route pitch. Our implementation of library cell layout shows the equally same height for all logic cells and it enables to place and route effectively for building large blocks. To predict the behavior of the design, the library cells should be characterized for performance. Characterization enables designers to move from the transistor level to the logic level. The gate in Fig .2 is characterized in terms of the input slew rate Tin and output capacitive load, CL. Timing Information such as timing arcs (delays from an input pin to an output pin), slew rates on output pins, timing checks such as setup and hold, tristate delays, etc. are modeled as part of delay characterization [6]. Both the input to output pin to pin (ptp) delay, Tptp, and the output slew rate, Tout, are required for gate level synthesis and delay calculation tools. Tin

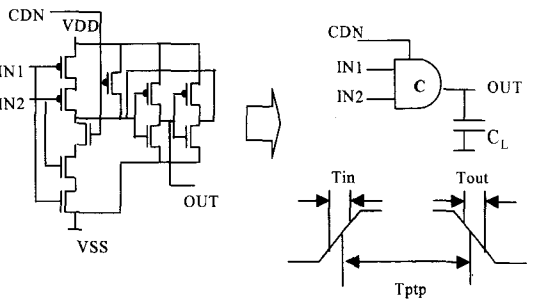

그림. 2 Muller-C gate의 지연시간 characterization
Fig. 2. Delay characterization for Muller-C gate.

and Tout are measured between two pre-determined edge threshold values and Tptp is measured between pre-determined delay threshold values [8],[9]. The gate is simulated with HSPICE (0.25um BSIM3V3 model) to obtain delay models for Tout and Tptp.

Fig.3 shows the library characterization data flow and layout verification flow. With the scale-down spacing such as 0.25um CMOS process, the p-n-p-n path in the internal cores of CMOS IC's is further sensitive to latchup [6],[7]. The methodology to verify the layout having latchup/ESD sensitive paths is shown in Fig.3, where the DRACULATM is used to check the spacing of the sensitive paths. By using the DRC and ERC functions of the DRACLATM, the latchup/ESD sensitive paths can be found and replaced by the way of insensitive layout styles.

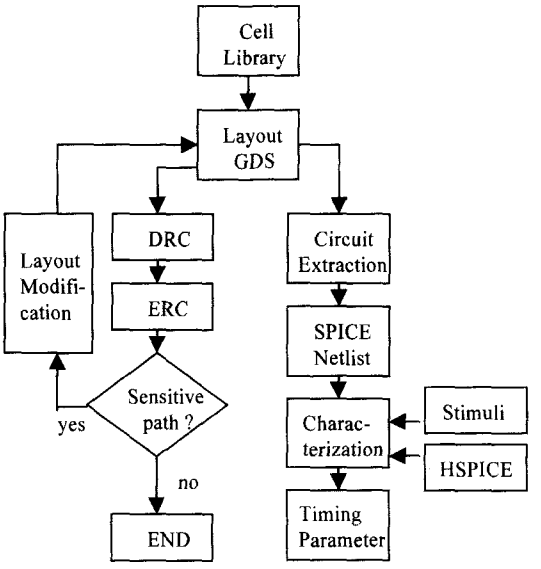

그림. 3 Layout 검증 순서
Fig. 3. Layout verification flow and library characterization data flow.

Ring oscillator simulation and design rules determine asynchronous library specification. This ring oscillator simulation decides optimized transistor size that is used to minimize the delay, power and power-delay product. Fig.4 shows structure of ring oscillator with 21 stages. The isolation buffer in Fig. 4 is used to decrease the effects of transition time caused by large load from divider block.

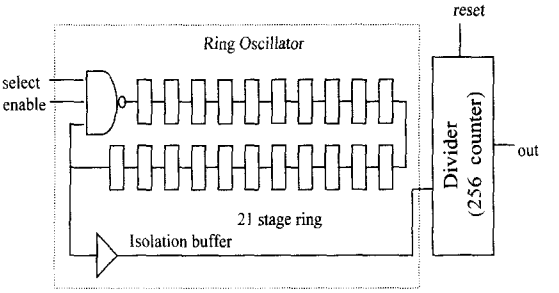

그림 4. Ring oscillator 의 구조
Fig. 4. Structure of ring oscillator.

In order to optimize the low power and high-speed, we used following methods. The first method for low power is like this: Ring oscillator simulation shows that as the size of transistor getting smaller, the power consumption also getting down because the parasitic capacitance is getting smaller. But, our suggestion is to optimize power consumption with considering logic threshold voltage of gate. This optimization results shows that the size and power of transistor are larger than those of minimized gate. The second method for high-speed is like this: Recursive SPICE simulation determines the optimized transistor size of PMOS and NMOS in order to minimize gate delay. This gate delay is calculated as average value from rise delay and fall delay by simulation that three gates are connected in series with standard load located behind each gate. This standard load is four inverters and routing capacitance. Table 1 shows the optimized layout area and gate delay for some asynchronous library.

표. 1 비동기 셀의 layout 면적과 지연시간
Table 1. Layout area and gate delay for asynchronous cells.

	Cell Size	Rise Prop.	Fall Prop.	Rise (Tr)	Fall (Tf).
Muller-C	8.8×8.8um^2	0.142ns	0.110ns	0.122ns	0.083ns
Trans.-latch	10.56×8.8um^2	0.130ns	0.203ns	0.201ns	0.095ns
Mutex	15.84×8.8um^2	0.130ns	0.216ns	0.152ns	0.009ns
Toggle	29.92×8.8um^2	0.143ns	0.216ns	0.196ns	0.109ns
Select	47.52×8.8um^2	0.235ns	0.248ns	0.176ns	0.114ns

With this same 8.8um-height of layout, the physical library can be ported into the automatic place & route tool such as Silicon Ensemble^{TM} and Apollo^{TM} software to generate optimized layout effectively. The followings are the characteristics of implemented physical library designed with 0.25um CMOS process.

- -This library is intended to function with a 2.5V.
- -This library is to be designed to support flipping and abutting cell rows.
- -We have normalized on a transistor width P/N ratio for this library of 1.3:1.
- -The horizontal track 1 and track 10 are coincident with the cell AB (Abutment Box) bottom and top, respectively.
- -It is preferred to place all input and output ports along one "Central Horizontal Grid" for all cells.
- -All input and output ports are located on the valid position.
- -Tap connections placed at the cell ends (left and/or right) are best placed directly beneath their power supply bus metals.

Ⅲ. SYSTEM DESIGN

In order to perform communication in heterogeneous system such as Fig. 1, asynchronous high-speed FIFO channel is needed for burst transmission. We implemented 4-stages micropipeline [4] FIFO that is self-timed circuits using two-phase or four-phase communication protocol and a bundled data format. Micropipeline falls into one of two types as follows: Transparent latch style and capture-pass latch style[4]. A block diagram of the transparent latch micropipeline FIFO is shown in Fig.5. Using asynchronous logic library, two types of micropipeline FIFO are designed with optimized method and are compared in aspects of layout area and delay time. The use of transparent latch in transparent latch micropipeline stage greatly simplifies the required control circuit than the control circuit of capture-pass micropipeline stage.

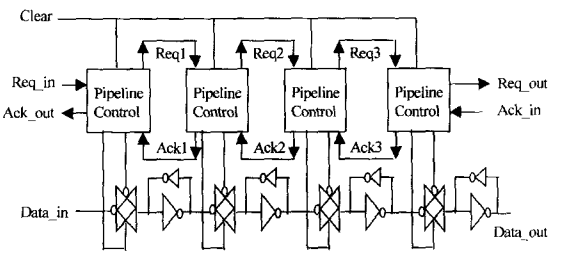

그림 5. Transparent latch 구조의 4단 FIFO
Fig. 5. Transparent latch 4-stages micropipeline FIFO.

Table 2 shows the layout area of each micropipeline stage and the simulated delay, again with appropriate output loading and full loading capacitance for a datapath latch. HSPICE(BSIM3V3 model with Nominal- Nominal strength) has been performed on extracted layout from the implemented design for the nominal case (Vdd=2.5V, at 25°C temperature). The transparent latch micropipeline is performed faster than capture-pass micropipeline. Measured control signals and data in-out signals on micropipeline stage are shown in the waveforms of Fig. 6. Fig. 6 represents the function of data transfer. The valid data is hold when *Req* is high, then as soon as *Ack* is

rising the data is transmitted to the latch output when *Req* is low. These results show that once valid data is presented at the latch input this data will be propagated to the latch output in 0.62ns for transparent latch FIFO operating at 1.6GHz.

표 2. FIFO에 대한 layout 면적과 지연시간
Table 2. Layout area and simulated delay for each FIFO.(0.25um four-layer metal CMOS process)

	Transparent latch FIFO	Capture-Pass FIFO
Control circuit	40.9×17.2um^2	35.3×17.2um^2
Datapath latch	12.3×9.2um^2	21.1×19.4um^2
Req_in to Req_out	0.73ns	0.42ns
Data_in to Data_out	0.62ns	0.89ns

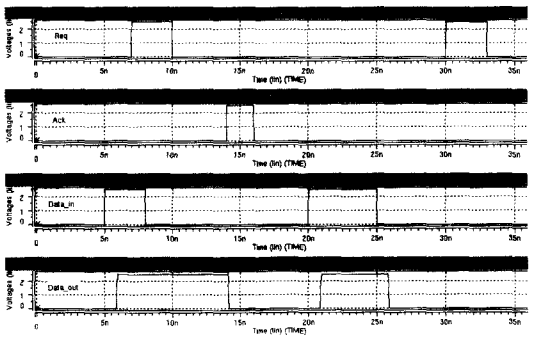

그림 6. Transparent latch FIFO의 SPICE 결과
Fig. 6. SPICE result on transparent latch FIFO.

Another key element for heterogeneous system except FIFO is interface circuit to transfer data between two modules that have different clock frequency and self-timed circuit. We used the pausible clocking scheme[1], which the local clock is paused or stretched to ensure that the handshaking signal satisfies setup and hold time constraints with respect to the local clock, to implement interface circuit. In this scheme, communication between a module and the FIFO is done using request/acknowledge handshake protocol. This method adjusts individual synchronous module's local clock, when necessary, to avoid synchronization failure. Using this scheme, the synchronous module communicating with asynchronous peripheral latches the handshaking signals from the asynchronous module by stopping or stretching its own clock. We implemented this pausible clocking scheme as PCC(Pausible Clocking Control) [1] circuit style. Fig.7 shows the block diagram of PCC scheme. In the block the clock generator should be designed as ring oscillator methods or PLL (Phase Locked Loop) methods. We used ring oscillator to produce the system clock. SOC (System On a Chip) should be designed with reusable component such as IP (Intellectual Property) block. This IP block which is standardized should be reused with little or no modification, because this IP is highly optimized for performance and speed. Ideally, this interface circuit should replace a portion of the system clock generation unit in some IP blocks to transfer data between another IP that has different clock frequency.

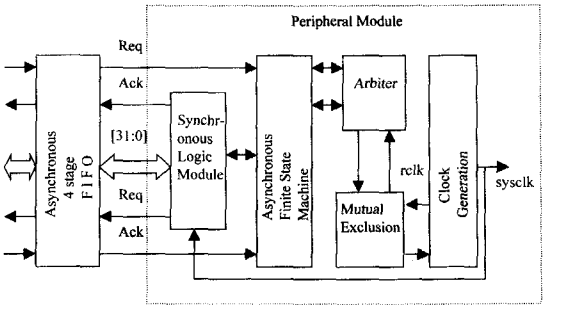

그림 7. FIFO 와 PCC 를 이용한 interface 구조
Fig. 7. Block diagram for interface using FIFO and PCC.

Ⅳ. EXPERIMENTAL RESULTS

We constructed 32-bit interface chip for heterogeneous system as shown in Fig.8. First, the asynchronous logic library, which includes layout cells and verilog models, is generated and characterized for optimized layout and

timing performance. Second, we implemented interface system using HDL with optimized timing model for functional verification and performed extensive SPICE simulation on extracted layout from the design done by VirtuosoTM layout editor. We used 0.25um CMOS process design rule with four-layer metal. With this interface chip 32bit data transfer is possible between two modules which clock frequency is different. The size of the core is about 1.1mm×1.1mm.

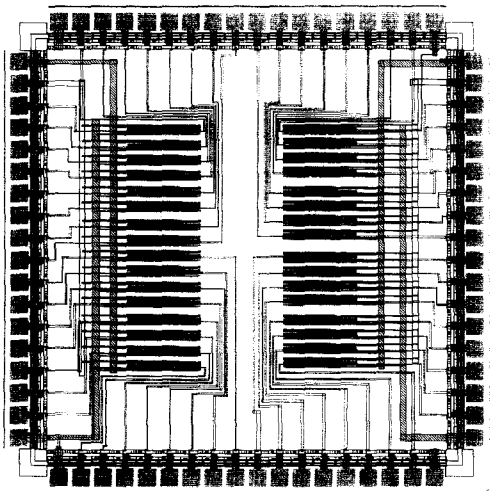

그림. 8 Chip layout
Fig. 8. The chip layout.

The timing trace in Fig.9 shows a simulation result including handshake and data signals. This result clearly indicates that the clocks do become stretched. The first event on *Req* (a rising transition) is acknowledged with pausing *sysclk*, and then second event(a falling transition) causes *sysclk* to be paused for about 0.2ns. As a result, this module operates at 2.2GHz, sysclk. The simulation was performed without FIFO module. With the addition or subtraction of ring oscillator stages, clock frequency could be changed to higher or lower. Because the module operates at higher clock frequency than the FIFO, the FIFO never occur bottleneck between them.

V. CONCLUSION

We implemented effectively optimized asynchronous logic library by characterization. Using this cell library, we designed a high-speed asynchronous micropipeline FIFO operating at 1.6GHz for heterogeneous system channels. The communication scheme, which is based on the pausible clocking scheme, is implemented with FIFO and PCC circuit on 0.25um CMOS chip. The resulting system

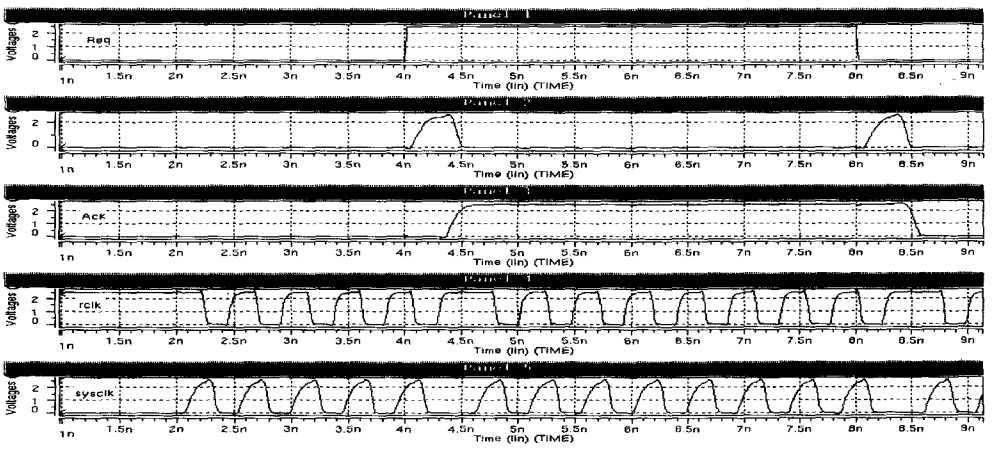

그림 9. PCC system 의 SPICE 결과
Fig. 9. SPICE result on pausible clocking control circuit system.

functions to the local clock frequency of 2.2GHz that is limited by the ring oscillator. This interface might be use efficiently in the part of microprocessor in order to minimize the power consumption and increase the performance.

In the future, we plan to implement the heterogeneous system using 32bit RISC processor and adjust at 3D graphic accelerator chip. In 3D graphic chip, there is an asynchronous block that is used to transfer data between processing block and rendering block. In addition, we will investigate a new clocking control circuit for high-speed and low power for mobile equipment.

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