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The Stress Dependence of Trap Density in Silicon Oxide

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Abstract

In this paper, the stress and transient currents associated with the on and off time of applied voltage were used to measure the density and distribution of high voltage stress induced traps in thin silicon oxide films. The transient currents were due to the discharging of traps generated by high stress voltage in the silicon oxides. The trap distributions were relatively uniform near both cathode and anode interface. The trap densities were dependent on the stress polarity. The stress generated trap distributions were relatively uniform the order of 1011~1021[states/eV/cm2] after a stress voltage. It appear that the stress and transient current that flowed when the stress voltage were applied to the oxide was caused by carriers tunneling through the silicon oxide by the high voltage stress generated traps.

Key words : Stress Current, Transient Current, Trap Density, Trap Distribution

I. Introduction

The stressing current of thin silicon oxide during and after high voltage have been studies. It has been shown that tunneling currents through thin silicon oxides at high stressing voltages generated electron traps within the silicon oxides.[1][2] Traps have been observed to be generated at the anode and cathode by the high stress voltage. The trap generation was independent of stress polarity. The stress induced trap generation has been an increase in the low level pretunneling current.[3][4]

The decay of the threshold voltage shifts caused by traps generated by avalanche injection was modeled by the tunneling discharge of the trapped electrons in the silicon oxides.[5] The discharging of shallow traps in Fowler Nordheim stressed thin silicon oxides has been traced to tunneling into the traps located near the cathode interface.[6][7]

The tunneling front model could be used to analyze the low level currents and pretunneling currents that have been observed in stressed silicon oxides. The transient currents associated with the during and removal of low voltage to the stressed silicon oxides were determined to be the charging and discharging of the traps generated in the silicon oxides. These transient currents were analyzed to determine the distribution of the stress generated traps in the silicon oxides near the anode and cathode interfaces.

II. Results and Discussion

A current density vs. voltage characteristic of an unstressed silicon oxide measured to breakdown has been shown in figure 1.

The current was composed of three regions, the low level, pretunneling region, the tunneling region and the breakdown region. Onset tunneling voltage was measured 7.2[V] with fluence $1.0^7\times10^{-8}$[C/cm^2] and Oxide breakdown voltage was measured 17.5[V] with fluence 1.29×10^{-1}[C/cm^2]. Prior to the onset of

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tunneling the currents were in the low ampere range. Constant voltages with high tunneling currents were used to stress the oxides. The stress currents were measured during the stress and integrated to obtain the fluence through the oxide. The transient currents associated with the turn off of the stress voltages were measured.

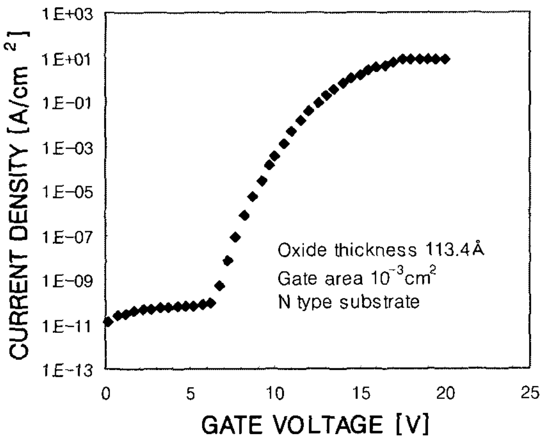


Fig. 1. A typical current voltage characteristic for a thin silicon oxide.

The stress currents through an unstressed oxide measured during application of constant positive gate voltage and the transient currents through an unstressed oxide measured after application of constant positive gate voltage has been shown in figure 2.

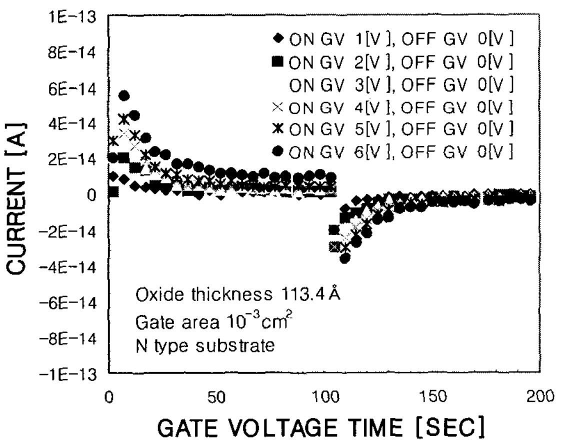
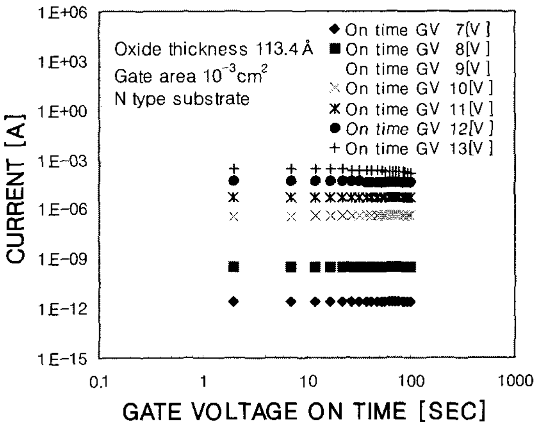


Fig. 2. The stress and transient currents through silicon oxide after/during the applied positive gate voltage for the Modified Fowler Nordheim(MFN) tunneling.

The constant gate voltage were on time when the positive currents flowed and were off time when the negative currents flowed. As long as the applied voltages were less than the onset voltage of the tunneling current, the transient currents were represented by the charging and discharging. The central 0 value of vertical axis was 10^{-15}[A] for the positive currents shown in the figure and -10^{-15}[A] for the negative currents shown in the figure.



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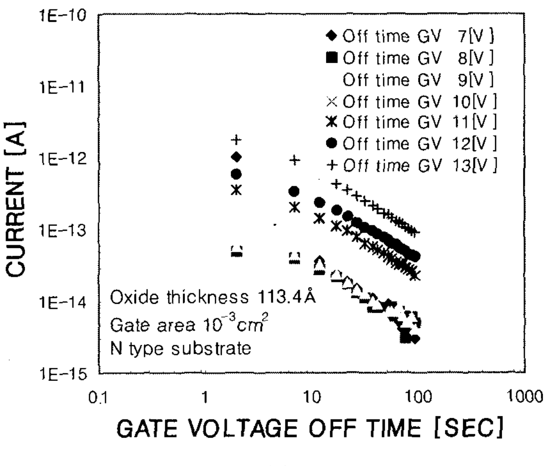

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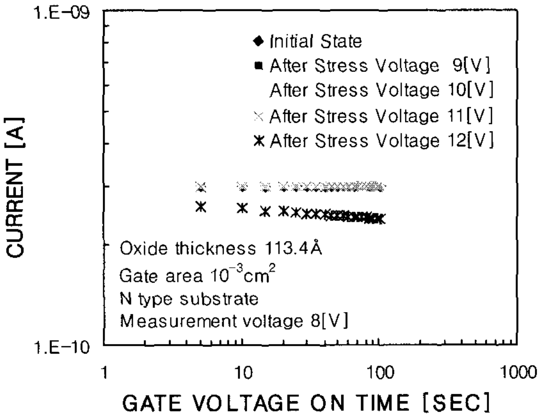
Fig. 3. The stress and transient currents through silicon oxide after/during the applied positive gate voltage for the Fowler Nordheim(FN) tunneling.
(1) The stress currents during the applied positive gate voltage
(2) The transient currents after the applied positive gate voltage

The stress currents were not exponential decay when the applied voltages were made larger than the onset of tunneling but the transient currents were exponential decay when the applied voltages were made less than the onset of tunneling. The transient currents were subsequently measured at low voltages below the onset voltage of tunneling.

When the voltages applied to the oxide were increased, the stress and the transient currents were measured, as shown in figure 3.



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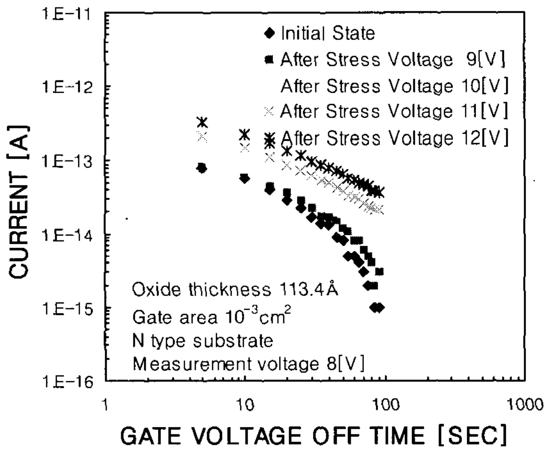

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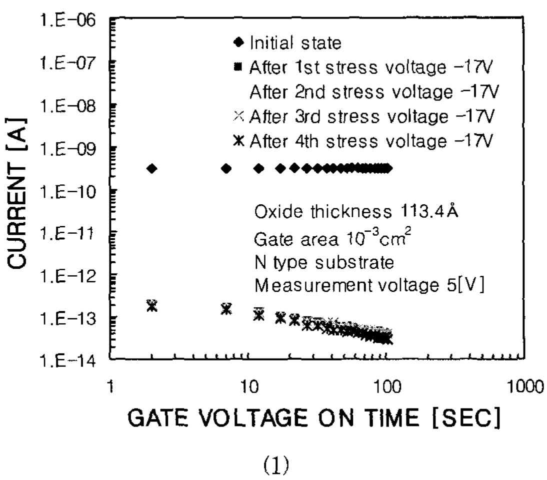
Fig. 4. The stress and transient currents through silicon oxide after stress voltage.
(1) The stress currents during the applied positive voltage 8[V] after stress voltage 9[V], 10[V], 11[V] and 12[V]
(2) The transient currents after the applied positive voltage 8[V] after stress voltage 9[V], 10[V], 11[V] and 12[V]

The stress currents when the voltage stresses were on time for the voltages for which FN tunneling was significant. The stress currents reflected the changes in the shape of the tunneling barrier due to trapping of electrons in the oxides. The transient currents after stress voltage were off time were decayed slowly. The transient currents followed an exponential decay.

The stress and transient currents were to stress the capacitor at high voltages and then measure the stress and transient currents through the capacitor at applied voltages after the stresses as shown in figure 4.

The capacitor in this case was stressed at 9[V], 10[V], 11[V] and 12[V] for 100[sec] respectively. The stress and transient currents were measured after the stress at 8[V] for 100[sec]. Higher stress voltages produced higher fluences through the oxides and associated with higher transient currents subsequently measured at low voltages. Both the charging and discharging currents measured at the low voltages rose as the stress fluence rose.

The stress and transient currents were to stress the capacitor at high voltages and then measured the stress and transient currents through the capacitor at applied voltages after the stresses as shown in figure 5.



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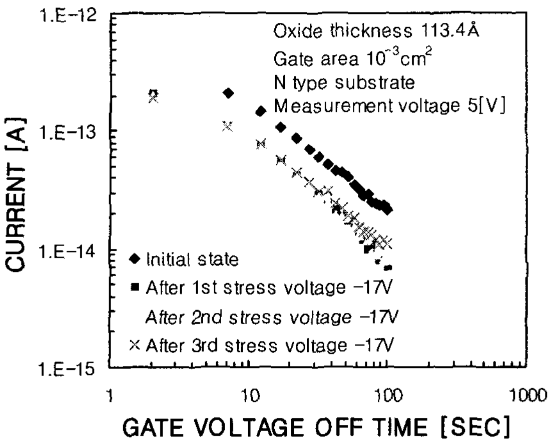

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Fig. 5. The stress and transient currents through silicon oxide after stress voltage.
(1) The stress currents after the applied pulse voltage −17[V]
(2) The transient currents after the applied pulse voltage −17[V]

The capacitor in this case was stressed at −17[V] for 100[sec] respectively. The stress and transient currents were measured after the stress at 5[V] for 100[sec].

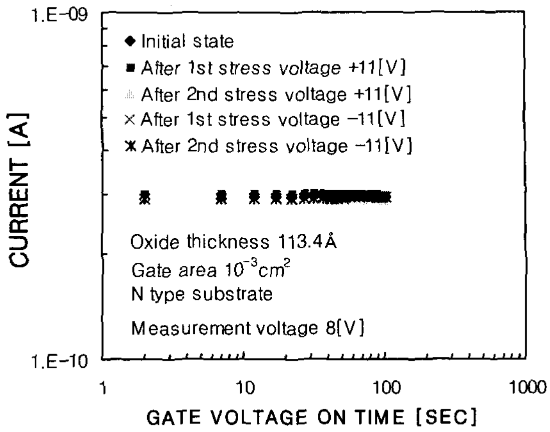
The stress and transient currents after application of a voltage pulse for an oxide that had been stressed with either positive stress voltage or negative voltage has been shown in figure 6.

The transient currents following the removal of a ±11[V] pulse have been plotted in figure 6 after both positive gate voltage stressing and negative gate voltage stressing at fluence level of $4.88\times 10^{-1}C/cm^2$ and $-6.04\times 10^{-7}C/cm^2$. The capacitor in this case was stressed at ±11[V] for 100[sec] respectively. The stress and transient currents were measured after the stress at 8[V] for 100[sec].

The density and distribution of the stress generated traps inside the oxide were based on the model used to explain tunneling. The current due to the discharge of the traps is given by

$$I(t) = qnvA = qAN(x(t))v = qAN(x(t))\frac{dx}{dt}$$

where $I(t)$ means the time dependence current due



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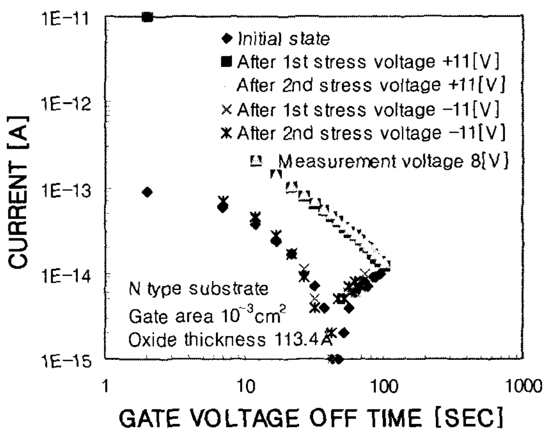

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Fig. 6. The stress and transient currents through an silicon oxide after stress voltage
(1) The stress currents after the applied pulse voltage ±11[V]
(2) The transient currents after the applied pulse voltage ±11[V]

to the discharging and charging of the traps in the oxide, q is the electronic charge 1.602×10^{-19} C, A is the capacitor area $1\times 10^{-3}cm^2$, $N(x(t))$ is the spatial distribution of the silicon oxide and $v=-\frac{dx}{dt}$ $cm\ \sec^{-1}$ is the velocity with which the tunneling distance moves through the oxides. The magnitude of the current would be proportional to the trap density.

Differentiating the position of the tunneling front leads to

$$I(t) = \frac{qN(x(t))A}{2\beta t}$$

The trap density was a function of the stress time and stress voltage. $N(x(t))$ equation is the time dependence of the transient current after removal of a stress voltage according to the discharging of the stress generated traps. The transient current after stress voltage removal was proportional to the traps generated inside of the oxide and decreased to the time.

The trap densities according to the stress and transient currents have been plotted in figure 7.

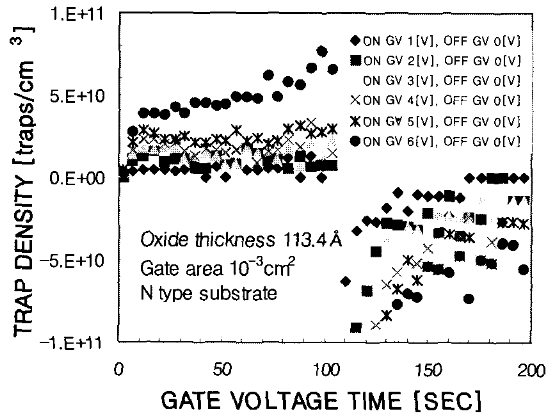
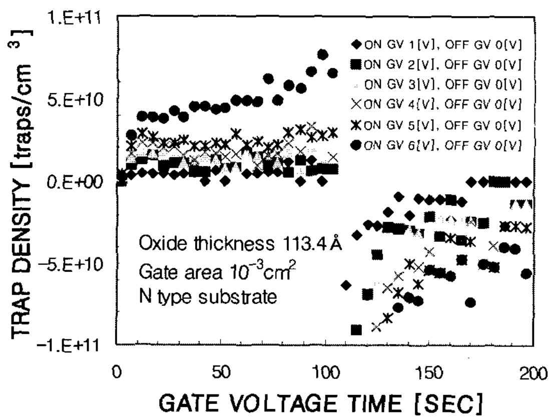


Fig. 7. The trap densities according to the stress and transient currents through a silicon oxide after/during the applied positive gate voltage for the Modified Fowler Nordheim (MFN) tunneling

The trap density measured in the oxide thickness 111.3Å was linearly proportional to the applied voltage inside the oxide.



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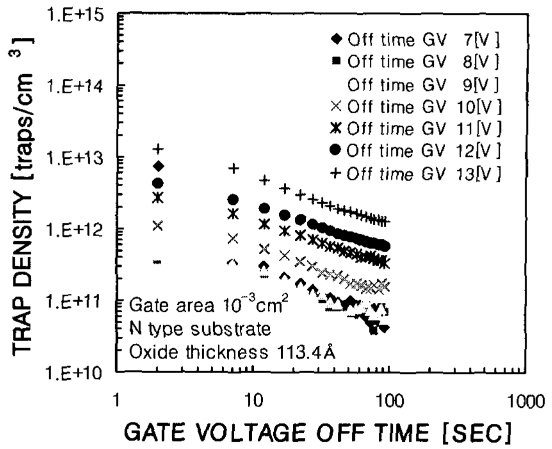

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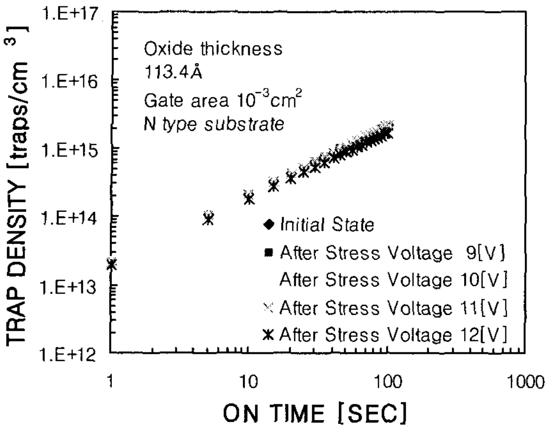
Fig. 8. The stress and transient trap densities through a silicon oxide after/during applied positive gate voltage for the Fowler Nordheim(FN) tunneling.
(1) The trap densities during the applied positive gate voltage
(2) The trap densities after the applied positive gate voltage

When the voltages applied to the oxide were increased, the stress and transient trap densities were measured, as shown in figure 8.

The trap densities are calculated using the tunneling front model as a function of stress voltage. A capacitor was stressed with different voltage for 100[sec]. After allowing adequate time for the decay of all transient currents, the stress voltages ranging from initial voltage to breakdown voltage were applied to the stress capacitor for 100[sec]. Adequated time was allowed in between pulses to ensure that all transient currents had decayed to the limit of the Ammeter.

The stress and transient trap density could be measured was to stress the capacitor at high voltages 9[V], 10[V], 11[V], 12[V] and then measured the stress and transient trap densities through the capacitor at applied voltages after the stresses as shown in figure 9.



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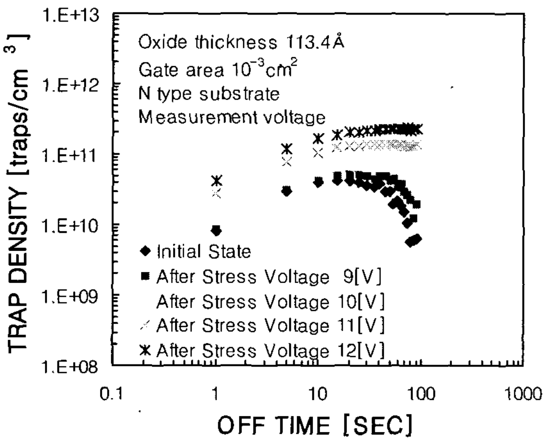

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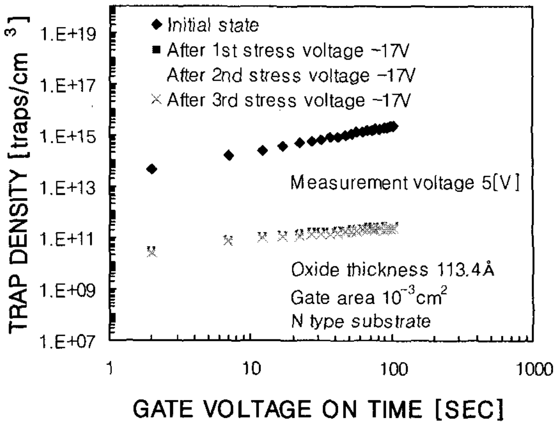
Fig. 9. The stress and transient trap densities after stress voltage
(1) The trap densities during the applied positive gate voltage 8[V].
(2) The trap densities after the applied positive gate voltage 8[V]



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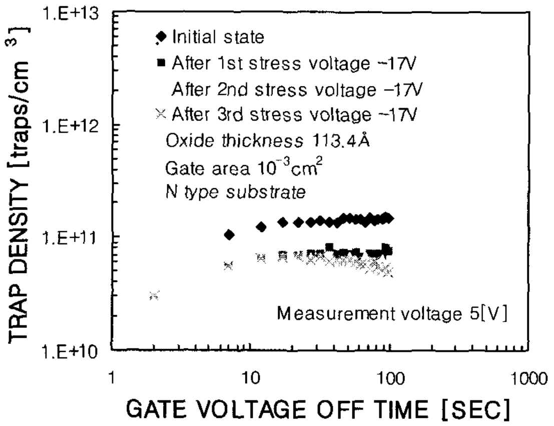

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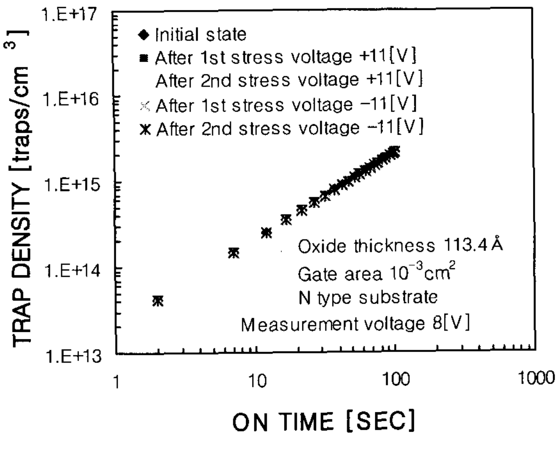
Fig. 10. The stress and transient trap densities through silicon oxide after stress voltage.
(1) The trap densities during the applied pulse voltage -17[V]
(2) The trap densities after the applied pulse voltage -17[V]

The stress and transient currents following the removal of a stress voltage pulse 9[V], 10[V], 11[V] and 12[V] have been shown after positive gate voltage stressing at fluence level of $1.46\times10^{-3}C/cm^2$, $3.48\times10^{-2}C/cm^2$, $4.78\times10^{-1}C/cm^2$ and $3.99C/cm^2$ respectively.

The stress and transient trap density was to stress the capacitor at voltages -17[V] and then measure the stress and transient trap densities through the capacitor at applied voltages after the stresses as shown in figure 10.

The stress and transient trap densities measured following high voltage stress were analyzed in terms of the currents predicted by the tunneling front model. The transient currents following the removal of a -17[V] pulse voltage have been plotted in figure 10 after negative gate voltage stressing at fluence level of $-2.40\times10^{-14}C/cm^2$ respectively.

The trap distributions in the oxide following positive and negative gate voltage stresses have been plotted in figure 11.



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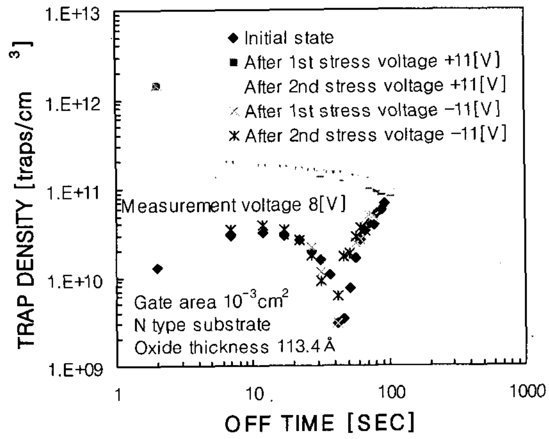

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Fig. 11. The stress and transient trap densities through an silicon oxide after stress voltage.
(1) The trap densities after the applied pulse voltage ±11[V]
(2) The trap densities after the applied pulse voltage ±11[V]

The discharge currents after negative gate voltage stressing were lower than after positive gate voltage stressing. The trap distributions were relatively uniform in the low with mid $10^{11}/cm^3$ range in the positive gate voltage stressing and mid $10^{10}/cm^3$ range in the negative gate voltage stressing. It has been shown that positive gate voltage stressing introduced negative charges in the oxide near the silicon oxide interface and negative gate voltage stressing introduced positive charges near the silicon gate oxide interface. It has been assumed that the stressing of the oxides introduced oppositely charged states at the gate oxide interface.

After the oxides had been stressed and traps had been generated in the oxides, the pretunneling currents and the discharge currents rose. The discharge currents have been adequately explained in terms of the tunneling front model. The pretunneling currents that flowed when the low measurement voltages were applied were also related to the charging of the stress generated traps. The traps were then charged by the application of 8[V] pulse was due to the ±11[V] pulse supplying the current needed to change the charge state of the traps in the oxide. The difference in these two charging currents had the 1/t time dependence that had previously been associated with the discharging of these traps by the tunneling front. Thus, by fitting the difference in the currents to a 1/t dependence, the charging of the traps in the oxide could also be explained by the tunneling front model.

Ⅲ. Conclusions

The transient currents associated with low voltage pulses applied to thin oxide MOS capacitors have been analyzed in terms of the charging and discharging of stress generated traps in the oxide. The tunneling front model was used to explain the 1/t time dependence of the decay current after application of a low voltage pulse. The trap densities derived within the oxide were the same order of magnitude as the interface trap densities measured at the silicon oxide interface on similarly stressed oxides. The trap densities were dependent on the stress polarity. The stress generated trap distributions were relatively uniform the order of 10^{11}~10^{21}[states/eV/cm^2] after a stress voltage. The trap distributions were relatively uniform near both cathode and anode interface.

Ⅳ. References

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