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# Transient trap density in thin silicon oxides

C.S. Kang, D.J. Kim, M.G. Byun* and Y.H. Kim*

*Yuhan College, Dept. of Electronic Engineering, Pucheon 422-749, Korea*
**Suwon University, Dept. of Electronic Material Engineering, Kyunggido 445-743, Korea*

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**Abstract** High electric field stressed trap distributions were investigated in the thin silicon oxide of polycrystalline silicon gate metal oxide semiconductor capacitors. The transient currents associated with the off time of stressed voltage were used to measure the density and distribution of high voltage stress induced traps. The transient currents were due to the discharging of traps generated by high stress voltage in the silicon oxides. The trap distributions were relatively uniform near both cathode and anode interface in polycrystalline silicon gate metal oxide semiconductor devices. The stress generated trap distributions were relatively uniform the order of $10^{11}$~$10^{12}$ [states/eV/cm$^2$] after a stress. The trap densities at the oxide silicon interface after high stress voltages were in the $10^{10}$~$10^{13}$ [states/eV/cm$^2$]. It was appeared that the transient current that flowed when the stress voltages were applied to the oxide was caused by carriers tunneling through the silicon oxide by the high voltage stress generated traps.

## 1. Introduction

High field stressing during program/erase cycles in EEPROM operation can lead to a significant increase in SILC (stress induced leakage current) in tunnel oxides. The stress and transient current of thin silicon oxide films during and after high voltage have been studied. It has been shown that tunneling currents through thin silicon oxides at high stressing voltages generated electron traps within the silicon oxides. Traps have been observed to be generated at the anode and cathode by the high stress voltage [1]. It has been shown that the trap generation at the cathode decreased as the fluence of electrons through the silicon oxide increased and was independent of stress polarity [1]. There had been an increase in the low level pretunneling current [2]. Low level pretunneling current has been attributed to a lowering of the tunneling barrier or to the increase at the cathode trap density [3].

The time decay of the threshold voltage shifts caused by traps generated by avalanche injection was modeled by the tunneling discharge of the trapped electrons in the silicon oxides [4]. The tunneling discharge of irradiation generated trapped electrons has been shown to be a function of the applied voltage [5]. The discharging of shallow traps in Fowler Nordheim stressed thin silicon oxides has been traced to tunneling into the traps located near the cathode interface [6-7]. The transient currents associated with the voltage application and with the removal of low voltage to the stressed silicon oxides were determined to be the charging and discharging of the traps generated in the silicon oxides. These transient currents were analyzed to determine the distribution of the stress generated traps in the silicon oxides near the anode and cathode interfaces. These techniques were to find differences in trap densities near the stress anodes and stress cathodes in silicon oxides.

## 2. Experimental

The thin silicon oxide used in this work were 113.4 Å thin fabricated using an $n^+$ polysilicon gate LOCOS process on 0.5 ohm cm n-type silicon. The oxides were grown in dry $O_2$ at 900°C. The currents through the silicon oxide were measured using a HP4140B. The measurement equipment was capable of resolving currents as low as 1fA. The currents through the silicon oxides were measured both as a function of voltage and time, both during and after high voltage stressing. Positive and negative measurement voltages by positive and negative stress voltages were used. The capacitor area were $10^{-3}$ cm$^2$.

A current voltage characteristic of an unstressed silicon oxide measured to breakdown has been measured. The prior to the onset of tunneling the currents were

in the low femto ampere range. Constant voltages with high tunneling currents were used to stress the silicon oxides. The currents were measured during the stress and integrated to obtain the fluence through the silicon oxides. The transient currents associated with the turn off of the stress voltages were measured. After stressing, the stress and transient currents were measured during long times after the voltages had been removed.

## 3. Results and discussion

A typical current voltage characteristic for a thin silicon oxide was composed of four regions, the low level, pretunneling region, the tunneling region and the breakdown region. Onset tunneling voltage was measured 7.2 [V] with fluence $1.07\times10^{-8}$ [C/cm$^2$] and oxide breakdown voltage was measured 17.5 [V] with fluence $1.29\times10^{-1}$ [C/cm$^2$]. Prior to the onset of tunneling the currents were in the low ampere range. Constant voltages with high tunneling currents were used to stress the oxides. The stress currents were measured during the stress and integrated to obtain the fluence through the oxide. The transient currents associated with the turn off of the stress voltages were measured.

The stress currents through an unstressed oxide measured during application of constant positive gate voltage and the transient currents through the stressed oxide measured after application of constant positive gate voltage has been shown in Fig. 1.

The constant gate voltages were on time when the positive currents flowed and were off time when the negative currents flowed. As long as the applied voltages were less than the onset voltage of the tunneling current, the transient currents were represented by the charging and discharging. The central 0 value of vertical axis was $10^{-15}$ [A] for the positive currents shown in the figure and $-10^{-15}$ [A] for the negative currents shown in the figure.

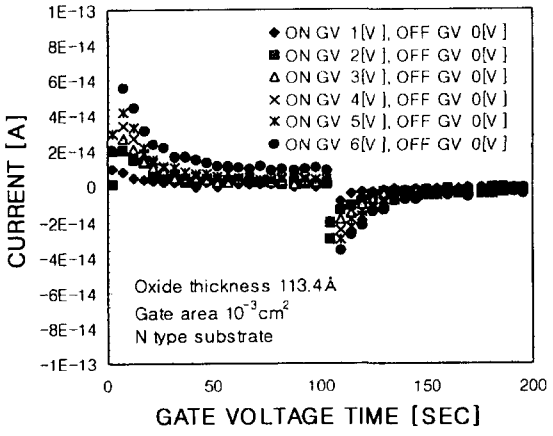


Fig. 1. The stress and transient currents through silicon oxide after/during the applied positive gate voltage.

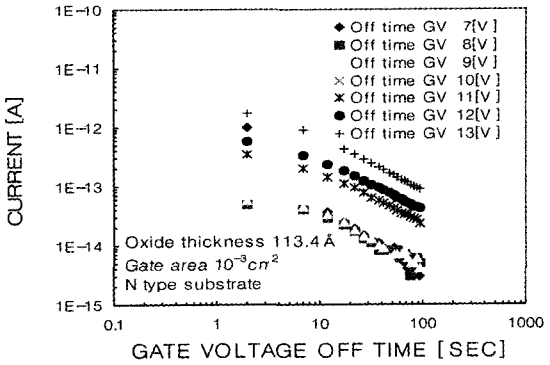


Fig. 2. The transient currents through silicon oxide after the applied positive gate voltage.

The stress currents were not exponential decay when the applied voltages were made larger than the onset of tunneling but the transient currents were exponential decay when the applied voltages were made less than the onset of tunneling. The transient currents were subsequently measured at low voltages below the onset voltage of tunneling.

When the voltages applied to the oxide were increased, the transient currents were measured, as shown in Fig. 2.

The stress currents associated with the voltage application were on time for the voltages for which FN tunneling was significant. The stress currents reflected the changes in the shape of the tunneling barrier were due to trapping of electrons in the oxides [9]. The transient currents after stress voltage were off time were decayed slowly. The transient currents followed an exponential decay.

The transient currents were to stress the capacitor at high voltages and then measured the transient currents through the capacitor at applied voltages after the stresses as shown in Fig. 3.

The capacitor in this case was stressed at 9 [V], 10 [V], 11 [V] and 12 [V] for 100 [sec] respectively. The stress and transient currents were measured after the stress at 8 [V] for 100 [sec]. Higher stress voltages produced higher fluences through the oxides and associated with higher transient currents subsequently measured at low voltages. Both the charging and dis-

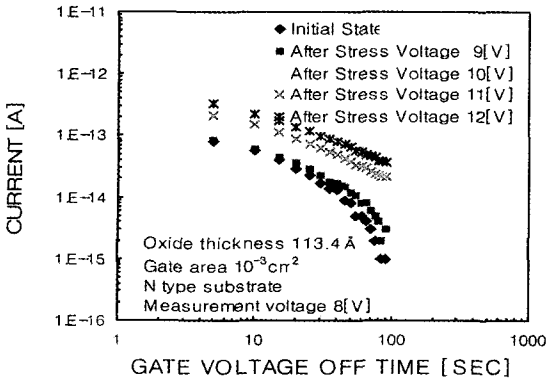


Fig. 3. The transient currents during the applied positive voltage 8 [V] after stress voltage 9 [V], 10 [V], 11 [V] and 12 [V].

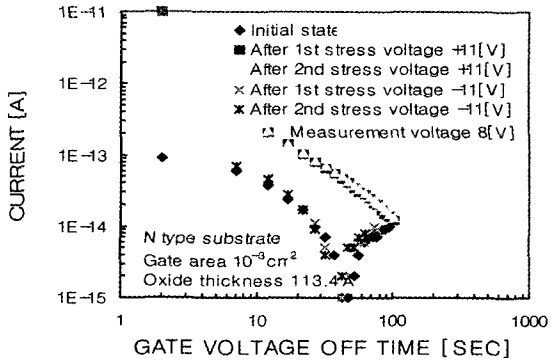


Fig. 5. The transient currents after the applied pulse voltage ±11 [V].

charging currents measured at the low voltages rose as the stress fluence rose.

The transient currents were to stress the capacitor at high voltages and then measured the transient currents through the capacitor at applied voltages after the stresses as shown in Fig. 4.

The capacitor in this case was stressed at -17 [V] for 100 [sec] respectively. The stress and transient currents were measured after the stress at 5 [V] for 100 [sec]. Whenever the polarity of the measurement voltage was opposite to the stress voltage polarity, measurement had a sufficient interval time for completely change the charge state of the traps. After the negative high voltages were applied to an oxides, the transient currents decayed due to the positively charged traps generated anodes. the trap generation processes the traps were remained in their positions inside the oxides.

The transient currents after application of a voltage

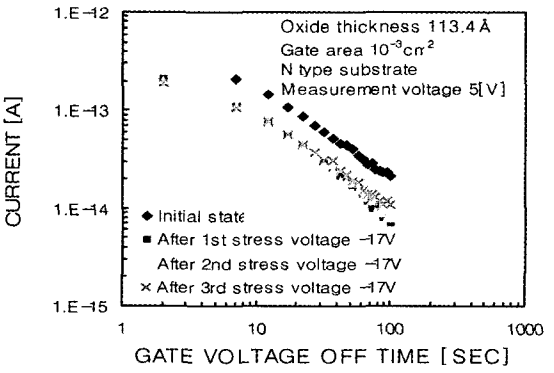


Fig. 4. The transient currents after the applied pulse voltage -17 [V].

pulse for an oxide that had been stressed with either positive stress voltage or negative voltage has been shown in Fig. 5.

The transient currents following the removal of a ±11 [V] pulse have been plotted in Fig. 5 after both positive gate voltage stressing and negative gate voltage stressing at fluence level of $4.88\times10^{-1}C/cm^2$ and $-6.04\times10^{-7}C/cm^2$. The capacitor in this case was stressed at ±11 [V] for 100 [sec] respectively. The stress and transient currents were measured after the stress at 8 [V] for 100 [sec]. The transient currents were measured before and after the stresses using both positive and negative voltages. The measurement voltages did not generate new traps. The transient currents were smaller after each stress cycle according to the increased number of cycles.

The trap densities were calculated from the decay of the transient current following removal of each stress voltage pulse. The density of the stress generated traps inside the oxide were based on the model used to explain tunneling. The current due to the discharge of the traps is given by

$$I(t) = qnvA = qAN(x(t))v = qAN(x(t))\frac{dx}{dt} \qquad (1)$$

where, I(t) means the time dependence current due to the discharging and charging of the traps in the oxide, q is the electronic charge $1.602\times10^{-19}C$, A is the capacitor area $1\times10^{-3}\,cm^2$, N(x(t)) is the spatial distribution of charge trap in the silicon oxide and $v = -(dx)/(dt)$ cm $sec^{-1}$ is the velocity with which the tunneling distance moves through the oxides. The magnitude of the current would be proportional to the trap density.

Differentiating the position of the tunneling front

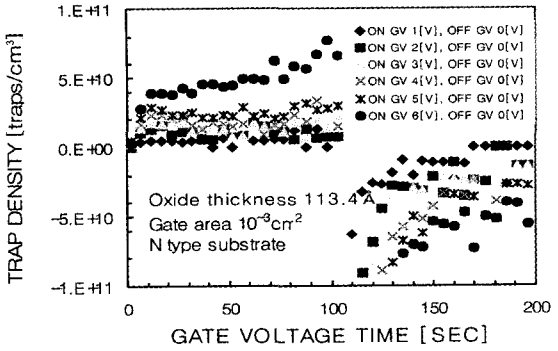


Fig. 6. The trap densities according to the transient currents through a silicon oxide after/during the applied positive gate voltage.

[10] leads to

$$I(t) = \frac{qN(x(t))A}{2\beta t} \quad (2)$$

The trap density is a function of the stress time and stress voltage. β is the tunneling constant. N(x(t)) equation is the time dependence of the transient current after removal of a stress voltage according to the discharging of the stress generated traps. The transient current after stress voltage removal is proportional to the traps generated inside of the oxide and decreased to the time.

The trap densities according to the transient currents have been plotted in Fig. 6.

The trap density measured in the oxide thickness 111.3 Å was linearly proportional to the applied voltage inside the oxide.

When the voltages applied to the oxide were increased, the transient trap densities were measured, as shown in Fig. 7.

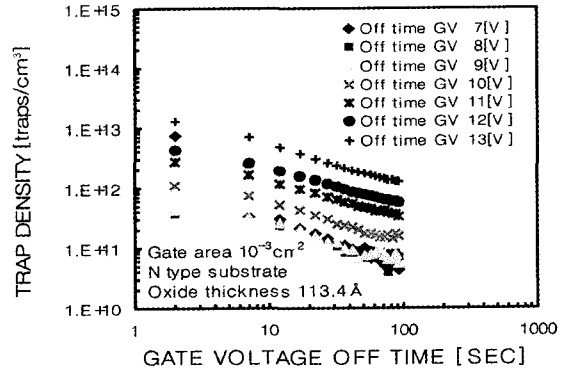


Fig. 7. The transient trap densities through a silicon oxide after applied positive gate voltage.

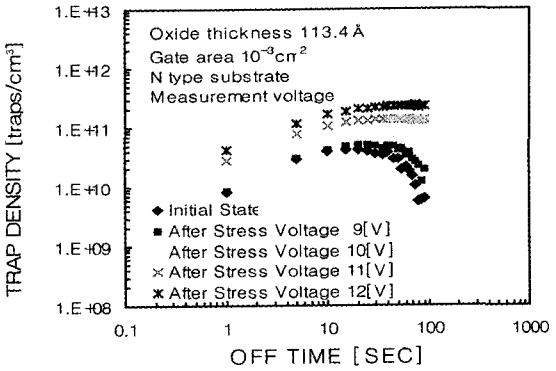


Fig. 8. The trap densities after the applied positive gate voltage 8 [V].

The trap densities were calculated using the tunneling front model as a function of stress voltage. A capacitor was stressed with different voltage for 100 [sec]. After allowing adequate time for the decay of all transient currents, the stress voltages ranging from initial voltage to breakdown voltage were applied to the stress capacitor for 100 [sec]. Adequated time was allowed in between pulses to ensure that all transient currents had decayed to the limit of the Ammeter.

The transient trap density was to stress the capacitor at high voltages 9 [V], 10 [V], 11 [V], 12 [V] and then measured the stress and transient trap densities through the capacitor at applied voltages after the stresses as shown in Fig. 8.

The transient currents following the removal of a stress voltage pulse 9 [V], 10 [V], 11 [V] and 12 [V] have been shown after positive gate voltage stressing at fluence level of $1.46\times10^{-3}$C/cm$^2$, $3.48\times10^{-2}$C/cm$^2$, $4.78\times10^{-1}$C/cm$^2$ and 3.99C/cm$^2$ respectively.

The transient trap density was to stress the capacitor at voltages -17 [V] and then measured the tran-

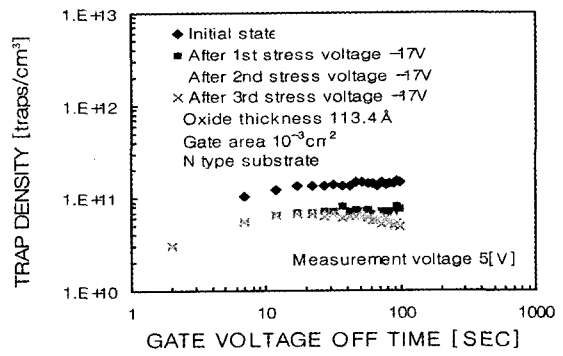


Fig. 9. The trap densities after the applied pulse voltage -17 [V].

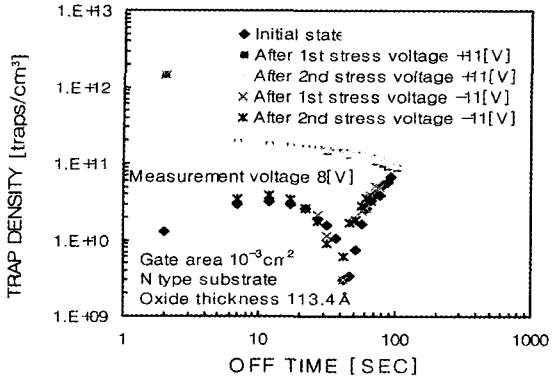


Fig. 10. The transient trap densities through an silicon oxide after the applied pulse voltage ±11 [V].

sient trap densities through the capacitor at applied voltages after the stresses as shown in Fig. 9.

The transient trap densities measured following high voltage stress were analyzed in terms of the currents predicted by the tunneling front model. The transient currents following the removal of a -17 [V] pulse voltage have been plotted in Fig. 10 after negative gate voltage stressing at fluence level of $-2.40\times10^{-14}$C/cm$^2$ respectively.

The trap distributions in the oxide following positive and negative gate voltage stresses have been plotted in Fig. 10.

The discharge currents after negative gate voltage stressing were lower than after positive gate voltage stressing. The trap distributions were relatively uniform in the low with mid $10^{11}$/cm$^3$ range in the positive gate voltage stressing and mid $10^{10}$/cm$^3$ range in the negative gate voltage stressing. It has been shown that positive gate voltage stressing introduced negative charges in the oxide near the silicon oxide interface and negative gate voltage stressing introduced positive charges near the silicon gate oxide interface [9]. It has been assumed that the stressing of the oxides introduced oppositely charged states at the gate oxide interface [10].

After the oxides had been stressed and traps had been generated in the oxides, the pretunneling currents and the discharge currents rose. The discharge currents have been adequately explained in terms of the tunneling front model. The pretunneling currents that flowed when the low measurement voltages were applied were also related to the charging of the stress generated traps. The transient traps by the application of measurement voltage 8 [V] was due to the applied pulse voltage ±11 [V] supplying the current needed to change the charge state of the traps in the oxide. The difference in these two charging currents had the 1/t time dependence that had previously been associated with the discharging of these traps by the tunneling front.

## 4. Conclusions

The transient currents associated with low voltage pulses applied to thin oxide of the polysilicon gate Metal Oxide Semiconductor capacitors have been analyzed in terms of the charging and discharging of stress generated traps in the oxide. The tunneling front model was used to explain the 1/t time dependence of the decay current after application of a low voltage pulse. The trap densities derived within the oxide were the same order of magnitude as the interface trap densities measured at the silicon oxide interface on similarly stressed oxides. The trap densities were dependent on the stress polarity. The stress generated trap distributions were relatively uniform the order of $10^{11}$~$10^{12}$ [states/eV/cm$^2$] after a high field stress voltage. The trap distributions were relatively uniform near both cathode and anode interface.

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