

## Critical Cleaning Requirements for Back End Wafer Bumping Processes

Mike Bixenman

Kyzen Corporation

(2000년 2월 25일 접수, 2000년 3월 10일 게재승인)

**Abstract:** As integrated circuits become more complex, the number of I/O connections per chip grow. Conventional wire-bonding, lead-frame mounting techniques are unable to keep up. The space saved by shrinking die size is lost when the die is packaged in a huge device with hundreds of leads. The solution is bumps; gold, conductive adhesive, but most importantly solder bumps. Virtually every semiconductor manufacturer in the world is using or planning to use bump technology for their larger and more complex devices.

Several wafer-bumping processes used in the manufacture of bumped wafer. Some of the more popular techniques are evaporative, stencil or screen printing, electroplating, electroless nickel, solder jetting, stud bumping, decal transfer, punch and die, solder injection or extrusion, tacky dot process and ball placement. This paper will discuss the process steps for bumping wafers using these techniques.

Critical cleaning is a requirement for each of these processes. Key contaminants that require removal are photoresist and flux residue. Removal of these contaminants requires wet processes, which will not attack, wafer metallization or passivation. Research has focused on enhanced cleaning solutions that meet this critical cleaning requirement. Process parameters defining time, temperature, solvency and impingement energy required to solvate and remove residues from bumped wafers will be presented herein.

### Introduction

A key development in electronics manufacturing is the convergence of circuit board and die packaging technologies. This combination enhances the best attributes of each technology for higher performance. As technology evolves there will be many challenges that require innovation, a key challenge will be critical cleaning. To better understand critical cleaning, I will compare popular definitions of precision cleaning and critical cleaning.

**Precision Cleaning:** The removal of detectable contamination that contains specific undesirable physical or chemical properties known to affect product reliability and/or performance.

**Critical Cleaning:** The removal of detectable ionic and non-ionic contamination, where the physical or chemical properties prevent the successful completion of subsequent assembly/manufacturing processes, or the ability to comply with specific performance requirements.

Semiconductor processes have long been classified as critical applications by virtue of the fine geometry on devices and the disastrous effect particulate and film contaminants have on semiconductor products during the fabrication process. As demands on the electronic packaging industry to produce faster, smaller and lighter devices increase, industry is propelled to innovate packages that achieve cost advantages and superior performance. The design and fabrication of integrated circuits have been the prime movers in interconnection technology, forcing the search for smaller conductor widths, smaller spaces, smaller holes and pad sizes, improved materials, and innovations in manufacturing processes. These emerging technologies will drive the need for critical cleaning. This requirement will continue to drive technology development in the area of precision cleaning formulations.

### Wafer Level Packaging

Bumps are applied directly to the die themselves

before the wafer is cut up. These processes produce Chip Scale Packages and Flip Chip. Chip scale packaging refers to the fact that the package is no larger than 1.2 times that of the chip die. Flip chip refers to the practice of mounting the chip face down on the circuit board rather than face up as in traditional lead frame packages. One of the distinguishing features in CSP is bringing IC signals to pads arrayed across the surface of the die rather than along the edge. Solder is then applied, using one of various techniques. Solder is then reflowed to bond it to the pad metal and form it into uniform spheres or balls. Reflow is done in special infrared or hot nitrogen reflow ovens. Finally the entire wafer is bumped before it is cut up into dies.

In the future ICs will be designed specifically for bump mounting. Signals will be routed directly to pads within the die face rather than to the edges.

#### Bumping Techniques

##### C4 Controlled Collapse Chip Contact

- ◆ Developed by IBM in the 1960s
- ◆ First method of applying solder bumps.
- ◆ Evaporative technique.
- ◆ A molybdenum mask is applied to the wafer. A high lead alloy (95%Pb/5%Sn) is deposited onto the bump sites as well as the molybdenum mask and all over the inside of the process chamber.
- ◆ Only about 5% of the solder lands where it is useful.
- ◆ The process is slow but is very precise.
- ◆ Molybdenum mask is removed.

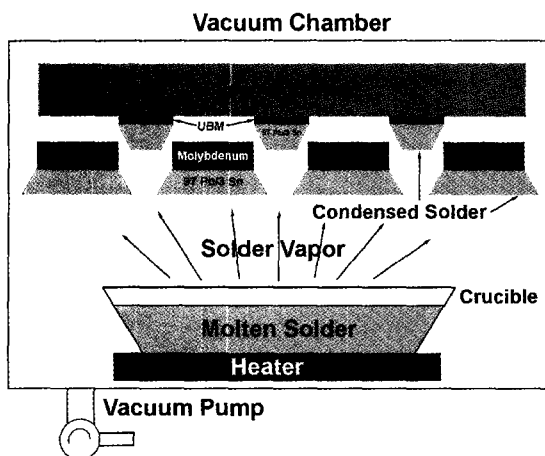


Fig. 1. Heated Crucible/Evaporative Process.

- ◆ The cylinders of solder are reflowed.
- ◆ About 20% of all solder bumps are applied by evaporation (C4).

##### Stencil or screening

- ◆ Essentially the same technique used to apply solder paste to circuit boards for attaching surface mount devices.
- ◆ Fine mesh solder paste and a semi-liquid flux is applied through using a screen stencil printing process.
- ◆ The size of the stencil holes and the thickness of the stencil material determine the amount of solder applied.
- ◆ An alternate method, used for finer holes and more precise positioning, is to use a layer of resist as the screen and press the paste into the holes with a flexible wiper.
- ◆ Resist or metal stencil is removed.
- ◆ Solder is reflowed to attach it to the base metal and form uniform spherical bumps.

##### Typical Process for Stencil Print Bump Formation

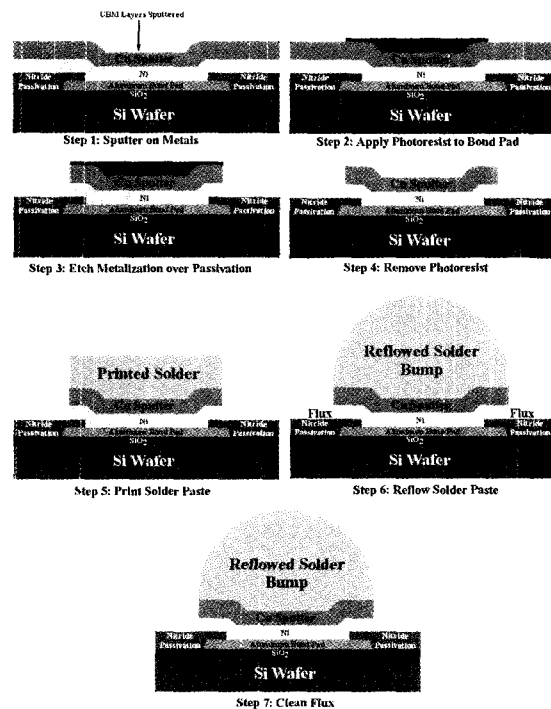


Fig. 2. Example of Stencil Printing Process Flow.

- ◆ Flux is removed.
- ◆ Stencil application is the least expensive method of applying solder bumps and accounts for about one third (33%) of all solder bumps.
- ◆ Quick and inexpensive, but generally limited to bumps of 100 microns (0.1mm) diameter or larger.

**Electroplating**

- ◆ Most common method of applying solder bumps, accounting for 46% of all bumps.
- ◆ As with all pattern-plating applications, a conductive seed layer is deposited (with CVD or PVD) and the wafer is coated with a resist, the resist is then exposed and developed, and the solder plated into the holes.
- ◆ Unlike C4 (IBM process), solder is deposited only where it is wanted.
- ◆ The solder bumps are large compared to typical IC pattern plating applications, the resist must be very thick-up to 100 microns thick so multiple layers of resist are typically applied.
- ◆ After plating, the resist is stripped, the solder reflowed, flux is removed and UBM (seed layer) is etched away.

**Solder Wires**

**Electroplating Eutectic Process Flow**

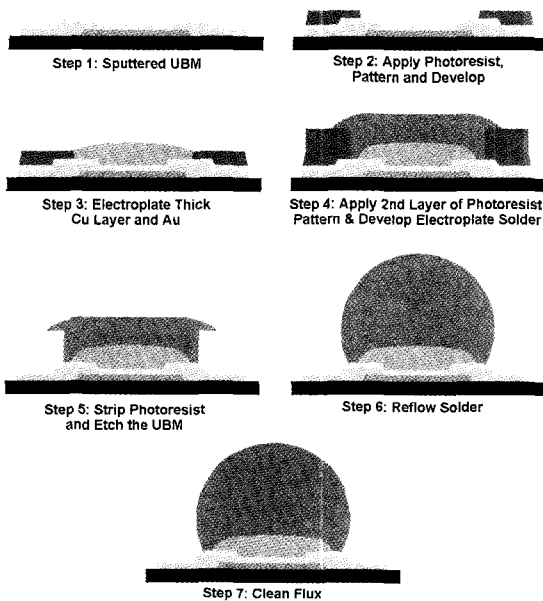


Fig. 3. Electroplating Process Flow Example.

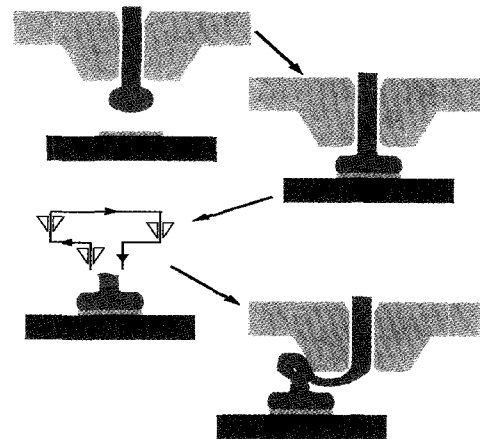


Fig. 4. Example of Wirebonding Process.

- ◆ This technique uses a wire of solder, which is pressure bonded to the substrate (wirebonding technology).
- ◆ Wire is crimped and broken off to a precise length.
- ◆ These short stubs of broken solder wire are then reflowed into bumps.
- ◆ Bump uniformity depends on precise control of the length of the wire stub.
- ◆ Very slow for wafers with hundreds of contacts per die.

**Solder jets**

- ◆ Molten solder is injected through an ink-jet printer.
- ◆ A platen holds the wafer and moves it around in front of the solder nozzle.
- ◆ The nozzle spits out precise balls of molten solder which stick to the wafer.
- ◆ The solder is reflowed to firmly attach it to the wafer.

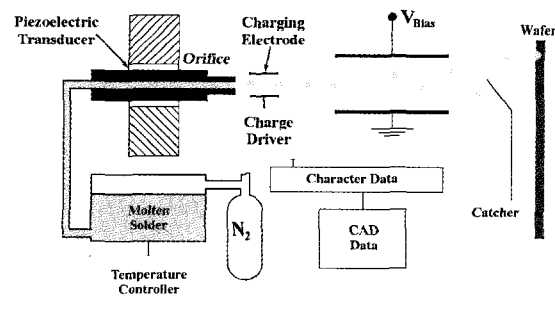


Fig. 5. Solder jetting process flow example.

### Ball Placement

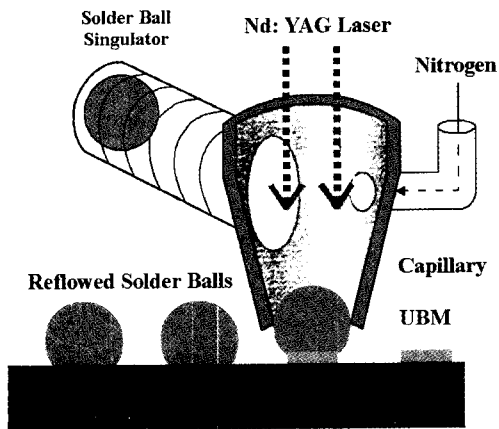


Fig. 6. Example of ball placement process.

- ◆ Top rates are roughly 400 bumps per second.
- ◆ Through put depends on the number of bumps per die and the number of dice per wafer.

#### Solder Balls:

- ◆ Balls of solder are placed onto the wafer.
- ◆ Pre-manufactured solder balls precisely controlled size is mechanically placed on a wafer covered with a thin adhesive layer of tack flux.
- ◆ The solder balls are then reflowed into bumps to bond them to the pads.
- ◆ Flux residue is removed.
- ◆ Technique is slow and the size of the solder bump depends on the size of the balls.
- ◆ Process control is limited.

### Wafer Bumping Critical Cleaning Requirement

Cleaning plays an important role in solder bumping. Key contaminants are photoresist and flux residue. A key consideration is the cleaning solvent compatibility with metallization and passivation layer. Industry standards require wafer cleanliness to meet the following criteria:

- ◆ No active residues that will cause pitting or corrosion during storage may be present.
- ◆ The cleaning chemistry must not attack metallization (i.e. copper, aluminum, tungsten, nickel, gold, silver, titanium, silicon etc.)

- ◆ The solder bumps must reflow and wet the substrate contact pads during the subsequent assembly process.
- ◆ The surface must be clean enough to insure good underfill adhesion during subsequent assembly process.

### Masks used to Expose Bond Pads for Bump Sites

The bond pads for the bump sites are small (50-150  $\mu\text{m}$ ) with a pitch of 50-200  $\mu\text{m}$ . Accuracy of solder deposition is critical. As a result, many bumping processes use a mask to expose the bump site. For evaporative processes the mask is molybdenum. For electroplating and stencil printing the mask is typically photoresist. The mask has to be removed or cleaned from the surface of the wafer following the bumping process. In most cases this occurs prior to reflow, but there are processes where the resist is removed following solder bump reflow.

The type of mask used and where it is removed in the bumping process requires different chemical properties to either dissolve or break up the mask material. Some of the material types used for the masking process vary in structure and composition. Cleaning chemistries tend to be process selective depending on cure, thickness of mask and exposure to high temperature.

### Molybdenum Mask

Molybdenum alloy is used to expose the bond pads for the evaporative high lead process. This alloy will stand up to the high temperatures used to evaporate high lead alloys. The wafer is clamped to the molybdenum mask. During the evaporative process, excess lead will accumulate onto the mask surface.

### Photoresist Mask

#### Liquid

There are two types of liquid photoresist, negative and positive. The resists are named according to the image on the wafer compared to the image on the mask

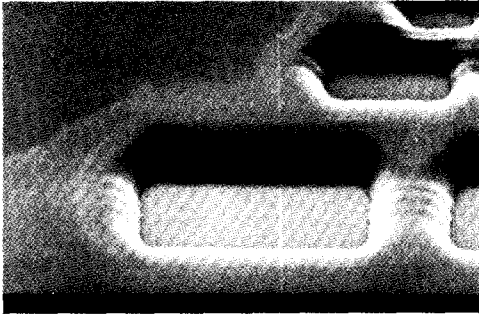


Fig. 7. 150 m gap, "D" optics-note diffraction.

or reticle. If the images are the same a positive resist was used. If the image on the wafer is opposite that of the image on the mask, a negative resist is used.

Liquid photoresist, whether positive or negative, is comprised of a thermoplastic phenol aldehyde resin and solvent. The solvent components allow the resist to be applied in liquid form. A solid photoactive compound and sensitizers are used to modify the spectral response of the resist.

Liquid resist is used to pattern the bump site when using **electroplating & stencil printing** bumping techniques. Thick resist films ranging from 20-50  $\mu\text{m}$  are used in some of these processes. The lithography of thick resists differs from that of the thinner layers commonly used in the semiconductor front-end processes. Thick resists have higher solvent content. The absorption of the film for thick resists is more critical, and delay times for re-hydration and nitrogen diffusion may vary.

Thin liquid resist films may also be used in stencil printing and preparation of electroless nickel under bump metallurgy. In certain processes, the solder paste is printed and reflowed with the resist and flux residue being the final cleaning step. Removal of the photoresist and flux residue is more difficult when this process is employed due to the additional heating step.

#### Films

Dry films are also used to pattern the bump sites. These films are typically used in stencil printing processes. Dry films do not dissolve in resist strippers. They are more difficult to remove and may have a tendency to leave residue on the wafer surface after cleaning.

#### Flux Technology

Fluxes are classified in accordance with their activity, low, moderate and high. For wafer bumping operations rosin, wafer soluble, synthetic and low solids flux technologies may be employed.

#### Rosin

Rosin alone has a mild fluxing activity. Its ability to induce solder wetting of many metals with more than a very slight oxide deposit is, however, limited. To enhance the fluxing activity of rosin flux, various chemical "activators" are commonly added. These can be nonionic organic materials that become active only at elevated temperatures of soldering or more active ionic materials such as amine halides or organic acids.

#### Water Soluble

Water-soluble organic fluxes, unlike rosin fluxes, have very little commonality with each other. This group of materials represents a very wide variety of chemicals. This class of fluxes is water-soluble. The residues of fluxes after soldering may, however, not show the same water solubility characteristics exhibited by the flux prior to soldering. The soldering processes expose the flux very high temperatures causing chemical reactions such as oxidation or decomposition. Such reactions generally give rise to products that may be partially insoluble in water. Residues are in the form of organometallic compounds or mineral salts.

#### Synthetic Activated

These materials are based on synthetic materials, which are not chemically related to rosin. These fluxes are mixtures of two or more synthetic organic compounds. They are normally formulated to be active fluxes and therefore, must be removed completely. The residues of SA fluxes are readily soluble in organic solvents.

#### Low Solids

This class of flux has a solids content of typically less than 5%. To ensure sufficient activity, the ratio of activator to rosin may be much higher than for conventional fluxes. The vehicle in low solids flux is a synthetic resin material, rosin or modified rosin. This

flux may be relatively difficult to remove.

#### **Wafer Bumping Cleaning Requirements**

Wafer bumping process contaminants consist of masking material and flux residue. Chemical strippers used to remove photoresist must not attack the metallization and passivation layer. Due to this issue, the cleaning solvents may be different from the strippers used to remove photoresist in front-end semiconductor process steps. Removal of flux residues is well known to electronic assembly. Technologies used in electric assembly may be adopted in these processes as well.

#### **Liquid Photoresist**

Removal of liquid resists are dependent on the process steps used. A solvent based stripper works well in processes where the resist is used as a mask and removed prior to reflow. If the resist is hard baked the solvent-based stripper may require additional ingredients, which are more active. If the resist is not removed until after the solder bump is reflowed, the stripper formulation may require more aggressive activators which may be aqueous in form.

#### **Dry Film Photoresist**

Removal of dry film resist is typically more difficult. Solvent-based strippers do not work well in most cases. Additional ingredients or activators may be required to break down the polymer. Another potential problem area with dry film resist is lifting the film instead of dissolving. When the film is lifted from the surface residues tend to stick to the wafer surface. Filters also clog when sheets of resist are lifted.

#### **Advanced Cleaning Chemistry Technology**

Back end semiconductor processing demands are driven by the need for higher I/O. As the demand for flip chip technology continues to grow the demand for bumped wafers also grows. As bumping technologies evolve the need for advanced cleaning processes will also evolve. Cleaning technologies for back end processing must be aggressive to dissolve the soil but not so aggressive to incur compatibility issues.

The design of the cleaning chemistries for back end semiconductor processing must be:

- ◆ Dissolve or break down contaminant
- ◆ Improve cycle time
- ◆ Environmentally friendly
- ◆ Adaptable to cleaning equipment technology
- ◆ Compatible
- ◆ Long life
- ◆ Economical

Three classes of cleaning solvent technology have emerged.

#### **Semi-Aqueous**

This technology consists of organic solvent blends designed to solvate the soil and then rinsed with deionized water. Key benefits are non-flammable, high soil loading, environmentally friendly, low toxicity and effective. Several newly developed semi-aqueous cleaning solvents have emerged for back end cleaning processes.

#### **Kyzen Non-linear Alcohol Semi-Aqueous**

This alcohol is produced from natural organic material or biomasses like spent rice hulls and corn cobs. As an organic material it is composed from the most universal of molecules: carbon, hydrogen, and oxygen without the use of mineral, metals and salts. Formulations composed from this alcohol are entirely biodegradable, completely water-soluble and water rinsable.

Formulations based on this solvent are excellent choices for removing flux residues and ionic contaminants. These characteristics of superior solvency while minimizing flammability give these alcohol-based products potential to be used in the widest range of cleaning equipment and processes. This technology has been industry proven for electronic assembly defluxing. They are used for defluxing commercial electronics, military approved, EPA/DOD/IPC Phase II tested, SNAP approved and widely available for use in aqueous and solvent equipment. Examples of its utility:

#### **Cleaning RMA Flux Residues in a High Lead Wafer Bumping Process**

During a high lead (5Sn/95Pb) wafer bump process

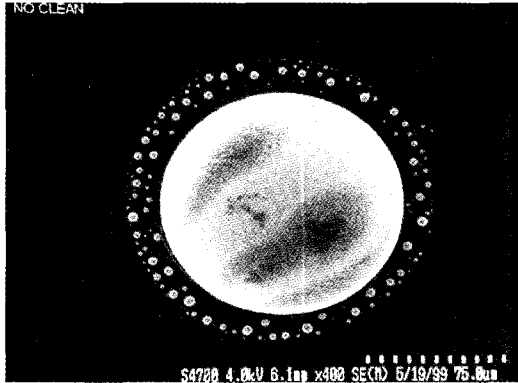
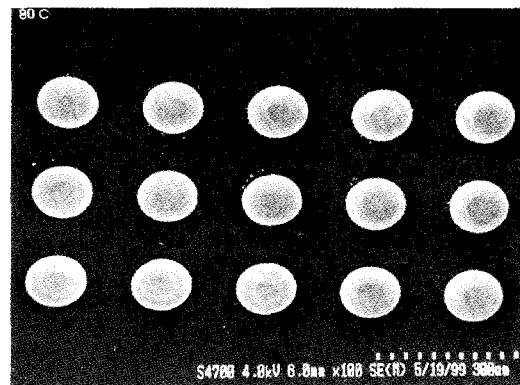


Fig. 8. SEM photograph of uncleaned solder bump courtesy of agilent technologies.

RMA flux is generally used for the solder reflow process following solder evaporation. Because the reflow temperatures reach 340-360°C, flux residues can be polymerized and are very difficult to remove. A cleaning solvent with high solvency for flux residue is required, yet must not cause pitting or corrosion of the solder bumps. Additionally, the solvent must rinse clean and leave no detrimental residue that would affect the subsequent die-attach process. Finally, it is attractive for the cleaning solvent to be recycled multiple times to prevent excessive amounts of waste. Environmental concerns such as biodegradability and treatment issues were also considered during the selection of the cleaning solvent. In a typical case study, Kyzen semi-aqueous non-linear alcohol cleaning solvent formulation combined with a centrifugal batch cleaner has been proven to be effective. The solvent is currently recycled through 800 cleaning cycles before being discharged to the wastewater stream.

Due to the nature of the evaporative solder deposition process, small solder balls remain around the main solder bump after reflow. These are referred to as "satellites". The satellites are not known to be a reliability problem, except for the following hypothesized effects. First, flux residue tends to collect around the base of the satellites, and since this is an active flux, it must be removed entirely to avoid corrosion. Second, satellites form on the passivation layer, and are not adhered as well as the solder bumps to the under bump metallurgy. Therefore, satellites are

a potential underfill failure-mode during long-term use and during thermal excursions. Satellites are formed during the initial reflow from an evaporated truncated cone to the spherical wafer bump. The combination of the effective solvent for removal of the subsequent and the centrifugal action of the equipment successfully removed the satellites.



Solder bumps cleaned at 178°F using ionox HC. Courtesy of agilent technologies

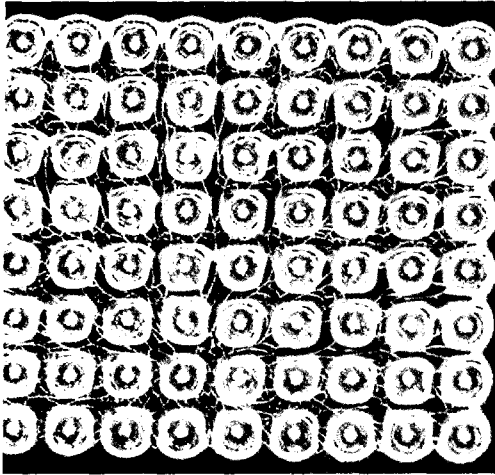
#### Oxygenated Semi-Aqueous Technology

Semi-aqueous oxygenated solvents are hydrocarbons, which are slow evaporating, non-flammable, water soluble and active solvents. Formulations based on these solvents are effective in defluxing and ionic salt removal. These products are low in odor and provide excellent solvency for polar and non-polar substances. Due to the very low vapor pressure the formulations based on these solvents may not be considered a VOC under some circumstances of use.

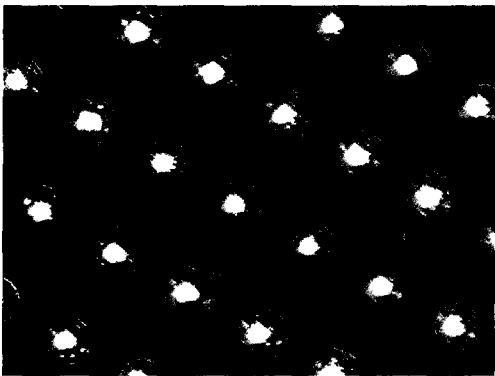
Temperature plays a critical part in the effectiveness of these products. These products are highly stable at operating temperatures. They provide long life and high soil loading characteristics. These examples show the effectiveness of the Oxygenated semi-aqueous technology is for removal of flux residues from high lead wafer bumping.

#### New Aprotic Solvent Semi-Aqueous Technology

A new isomeric solvent blend consisting of an aprotic solvent based piperidone. This solvent blend is a



Electroplating high lead flux residue

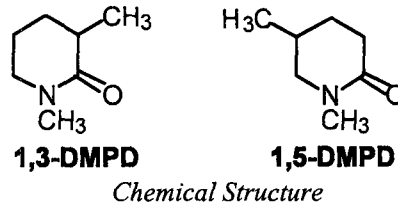


Removal of flux residue using an oxygenated solvent based formulation

colorless, high boiling liquid with a mild odor. Its chemical stability, solvency, and low toxicity are very similar to other aprotic solvents (e.g., n-methyl pyrrolidone). Because of its low metal content, low vapor pressure, non-flammability, and good solvency, formulations based on this solvent technology has good utility for back end wafer bumping critical cleaning requirements. This technology is highly effective on both photoresist stripper and defluxing.

This solvent has a solubility parameter very similar to n-methyl pyrrolidone (NMP). Its high solvency power for resins makes it an ideal selection for removing thick resists used to mask bond pads. Solvent-based photoresists will dissolve in formulations based on this technology. These formulations are

completely water rinsable and totally miscible. It may be rinsed as well with vapor degreased solvent technology as a co-solvent. Advantages over NMP are lower volatility, lower flammability, and lower viscosity and lower surface tension. This solution is thermally, chemically and hydrolytically stable. Formulations are of the highest purity with metals less than 100ppb. This technology is compatible with wafer metallization and passivation. Additional features are complete biodegradable, low toxicity, low vapor pressure, and low odor, non-flammable and recyclable.



#### Solvent Vapor Phase Technology

Vapor degreasing solvent technology has been practiced in this industry for many years. Prior to the discovery of the ozone layer depletion, CFC offered a universal cleaning solvent option. CFC vapor phase solvents have been limited in scope due to toxicity and ozone depletion issues. Fully fluorinated solvents have favorable toxicity and environmental characteristics. They are however poor cleaners for the soils encountered in back end wafer bumping processes.

Vapor phase formulations based on normal propyl bromide technology are highly effective on liquid photoresist and flux residues. The formulation characteristics are similar to other halogenated solvents such as 1,1,1-trichloroethane and trichloroethylene. These formulations have no flash point and have low ozone depletion potential. They are compatible with the metallization encountered on semiconductor devices.

#### Aqueous Technology

Water-soluble flux technology may be used to remove oxides prior to solder bump reflow. Neutral aqueous detergent blends will aid in both removing and neutralizing water-soluble fluxes. These cleaning agents are used at concentrations of less than 3%. The addition of a small amount of chemistry into the wash solution aids in the rinsing of materials that may have become



less soluble after reflow.

Dry film photoresist is very difficult to dissolve. When the films are lifted off the surface while cleaning, small film fragments tend to adhere to wafer surface. This causes issues with yields and forces a secondary cleaning process. Aqueous based formulations may provide an answer. These technologies are presently under development. Initial results indicate that this technology will break down the dry films as well as remove flux residues. Key issue of concern is compatibility. The aqueous formulation must provide inhibition on soft metals.

### Conclusion

Semiconductor processes have long been classified as critical applications by virtue of the fine geometry on devices and the disastrous effects particulate and film contaminants imposed on semiconductor products during the fabrication process. As the demands on the electronic packaging industry to produce faster, smaller and lighter devices increase, industry is propelled to continually improve and innovate packages that achieve cost advantages and superior performance. The design and fabrication of integrated circuits have been the prime movers in interconnection technology, forcing the search for smaller conductor widths, smaller spaces, smaller holes and pad sizes, improved materials, and innovations in manufacturing processes. These emerging technologies will drive the need for a critical cleaning requirement. This requirement will continue to drive technology development in the area of precision cleaning formulations.

Back end wafer level packaging is an outgrowth of flip chip technology. Several diverse technologies have been developed for bumping wafers. Photoresist is commonly used as a mask to expose the bond pad. Flux is used to remove oxides prior to reflow. Both residues must be removed. The technology used to remove photoresist in front-end processes may not be feasible

for back end processes due to compatibility issues. Remove of flux residues is a common technology used in electronic assembly and may be adapted for this technology.

Cleaning methods will be dependent on the bumping process and contaminant. Semi-aqueous, solvent and aqueous cleaning technologies will be selected based on the process need. All these cleaning technologies have proven robust and effective in each of these unique applications.

Please contact the author for any additional details on the above mentioned technologies at: Mike\_Bixenman@kyzen.com

### References

1. Considerations for an Electroplated Flip Chip Process, Dr. Paul A. Magill, J. Daniel Mis, and Glenn A. Rinne, IMAPS Boston, Unitive Electronics, May 1998
2. A Comparison of Popular Flip Chip Bumping Technologies, Deborah S. Patterson, Flip Chip Technologies
3. C4: A legacy Technology for the Future, Michael G. Nealon, IBM
4. Wafer Bumping Technologies-A Comparative Analysis of Solder Deposition Processes and Assembly Considerations, Deborah Patterson, Peter Elenius, James A. Leal, Flip Chip Technologies
5. Flip Chip Bumping for IC Packaging Contractors, Peter Elenius, Flip Chip Technologies
6. The Introduction of a new aprotic solvent, which is useful in semi-aqueous based formulations for electronic critical cleaning applications, Frank Herkes, Ph.D., DuPont Nylon, Mike Bixenman, Kyzen Corporation, Nepcon West 2000
7. Cleaning Issues Related to flip chip, ball grid array and chip scale packages, Mike Bixenman, Erik Miller, Kyzen Corporation, APEX 2000
8. Semitool Solder Story "Advanced Packaging"
9. New Developments in Thick Photoresist Applications, Dr. E. Cullmann, Karl Suss, DG GmbH, Munich, Germany