Implant Anneal Process for Activating Ion Implanted Regions in SiC Epitaxial Layers

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The mechanical strength of silicon carbide does not permit the use of diffusion as a means to achieve selective doping as required by most electronic devices. While epitaxial layers may be doped during growth, ion implantation is needed to define such regions as drain and source wells, junction isolation regions, and so on. Ion activation without an annealing cap results in serious crystal damage as these activation processes must be carried out at temperatures on the order of 1600°C. Ion implanted silicon carbide that is annealed in either a vacuum or argon environment usually results in a surface morphology that is highly irregular due to the out diffusion of Si atoms. We have developed and report a successful process of using silicon overpressure, provided by silane in a CVD reactor during the anneal, to prevent the destruction of the silicon carbide surface. This process has proved to be robust and has resulted in ion activation at a annealing temperature of 1600°C without degradation of the crystal surface as determined by AFM and RBS. In addition, XPS was used to look at the surface and near surface chemical states for annealing temperatures of up to 1700°C. The surface and near surface regions to approximately 6 nm in depth was observed to contain no free silicon or other impurities thus indicating that the process developed results in an atomically clean SiC surface and near surface region within the detection limits of the instrument (± 1 at. %).

Keywords: Ion implantation, Anneal, Silane overpressure

1. INTRODUCTION

Silicon carbide is an ideal semiconductor for high-power and high-temperature applications due to the high level of material stability at elevated temperatures. This high degree of mechanical stability, while it lends itself well to these applications, makes the formation of device structures that require selective area doping difficult. Indeed, SiC is primarily an epitaxial technology where ion implantation is used to selectively dope regions in the epitaxial layer to implement a specific device structure. Although dopant diffusion is the preferred process in silicon technology to achieve selective doping, diffusion rates in SiC are simply too low to permit this approach. Ion implantation in SiC has been demonstrated to be a suitable means for achieving degenerate doping densities for both p and n-type material with reasonable ion flux[1].

Unfortunately, the high bonding strength of the SiC lattice requires not only that the implant be carried out at elevated temperatures[1] but that the implant anneal be performed in excess of 1600 °C if full doping activation is to be achieved. It is widely believed that the degradation of the silicon carbide material surface after implant annealing is one reason responsible for MOSFET inversion layer carrier mobilities of less than 10 cm^2/V-s in 4H-SiC, a serious problem leading to unacceptable on-state resistances in these power devices[2]. As a consequence, the highest mobility MOSFET devices reported in SiC are either buried channel devices[3] or devices with a low thermal implant activation temperature[4] which also increases the series resistance in the drain and source regions. While the SiC lattice is inherently stable at lower temperatures, Si can out diffuse at elevated temperatures leading to a severe degradation in the surface morphology known as step bunching[5]. Numerous researchers have reported work on annealing SiC with various encapsulants which suppress the out diffusion of Si during the annealing process[6,7] but require that the encapsulating material be removed prior to continuing device fabrication.

2. EXPERIMENTAL

Ion Implanted 4H-SiC samples

Two sets of 4H-SiC samples were investigated during the course of this experimental study. Both sets of consisted of epitaxial layers with a thickness of approximately 5 μm grown by the Emerging Materials Research Laboratory using a process described elsewhere[8]. The epitaxial samples were diced into 5 mm square samples and ion-implanted at 700°C at Auburn University with either Al or C. The first set contained an n-type epitaxial layer with a doping density in the mid 10^{15} cm^{-3} range and were implanted with Al.

The second set of samples were composed of a p-type epitaxial layer with a doping density in the mid 10^{16} cm^{-3} range and were implanted with C. By investigating the implant anneal process on a single epitaxial layer the implant annealing could be optimized on epitaxial layers of the same doping and thickness.

A typical Al ion implantation profile is shown in Fig. 1. Implants were carried out at 700°C through a 110nm Mo mask layer in order to implant the near surface regions of the SiC epilayers.
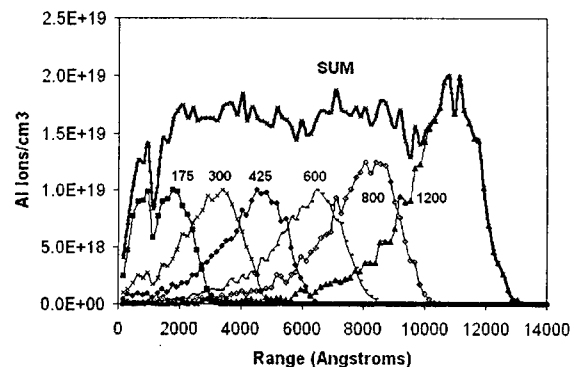

Fig. 1. Implant schedule used for the implant anneal studies. Al was implanted at 700°C. Multiple implants starting at 175 keV used to achieve the box profile shown (SUM in fig.).

Molybdenum was used since it does not react with SiC at the implant temperature used. Following ion implantation, the mask layer was etched away prior and the samples cleaned using the same cleaning process used for SiC epitaxial growth. The AFM photograph in Fig. 2 shows that the surface of the epilayer is somewhat degraded by the implant process. However, bulk crystalline quality is well preserved, as indicated by the ion channeling spectra also shown. These spectra were generated using standard Rutherford backscattering techniques and 2MeV He$^+$ ions scattered at 170° to the direction of the incident beam.

Silane Overpressure Annealing Process

A silane-based CVD reactor suitable for performing high-temperature anneals in a silicon rich ambient was used for these experiments. Annealing temperatures in excess of 1700 °C are possible by placing the sample to be annealed on a SiC coated graphite susceptor and heating the graphite using an RF induction coil, as has been discussed elsewhere for CVD growth of SiC epitaxial layers[8]. The final process schedule developed during this research is shown in Figure 3 and is as follows. After a 6 slm UHP Ar flow is established in the reactor, the RF generator is turned on and the susceptor heated to the annealing temperature (typically 1600°C) using a controlled thermal ramp. The silane is not introduced into the reactor until a substrate temperature of 1490°C is reached to suppress Si droplet formation.

At that time the premixed silane in Ar gas is introduced into the Ar carrier flow at a flow rate of 80 sccm. All flows are controlled using calibrated mass flow controllers to

ensure process repeatability. After the annealing temperature is reached a 30 minute anneal is conducted. At this point the reactor is purged of silane by simultaneously turning off the silane in Ar flow (3 slm UHP Ar flow remains on) and changing the set point temperature to 1400°C.
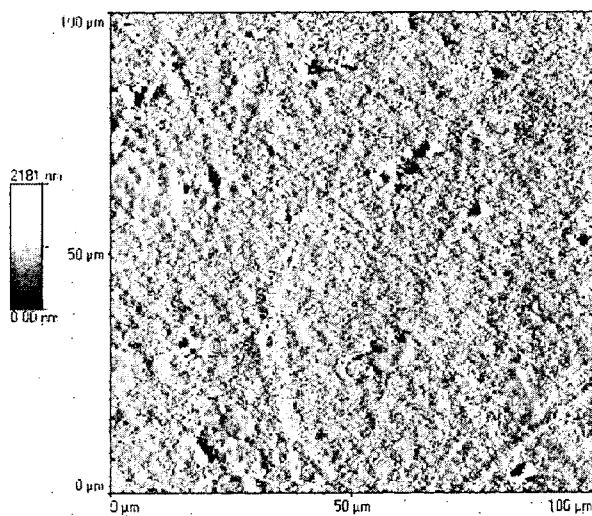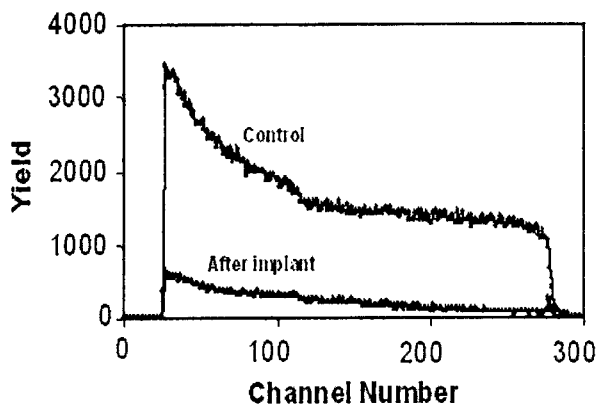

Fig. 2. Channeling RBS and AFM data of 4H-SiC implanted with Al at 700°C. Note the crystal quality is degraded due to implant damage, as expected.

This was found to be necessary as the surface morphology was often damaged under Ar purge conditions at the annealing temperature even for times as short as 1 minute. After the one minute Ar purge at 1400°C, the RF generator is turned off and the sample cooled to room temperature under Ar flow. This same process was used for both the Al and C implanted samples to ensure process stability.
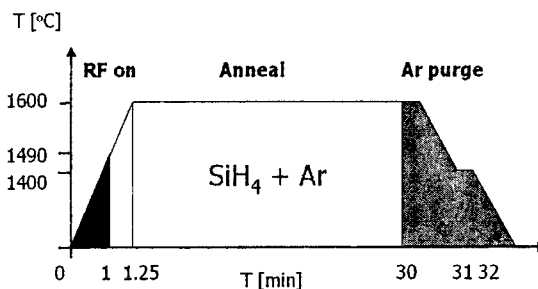

Fig. 3. Implant annealing process schedule indicating gas flow timing versus sample temperature.

30 mm CVD Annealing Experiments

Preliminary annealing experiments were conducted on Al implanted samples at 1600 °C at atmospheric pressure and under various silane flow conditions.
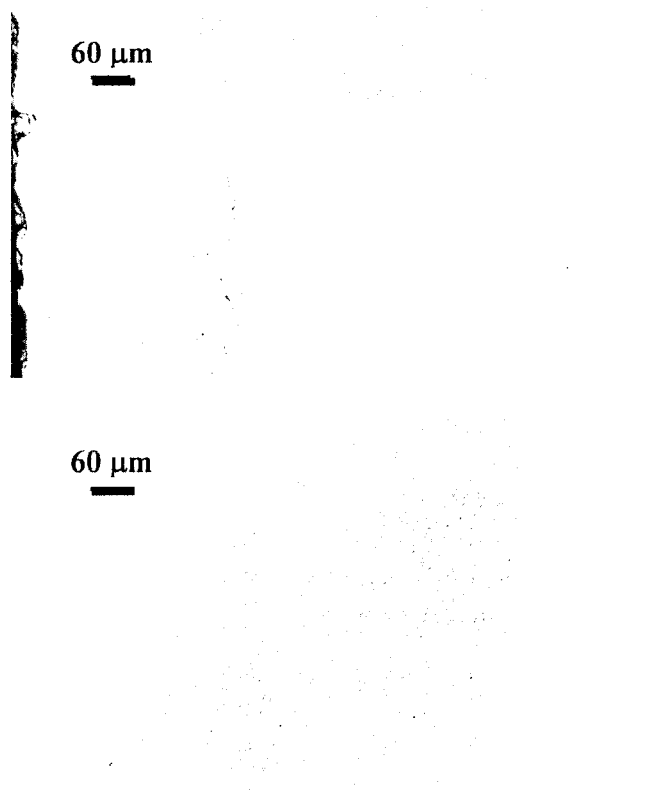

Fig. 4. Optical micrographs showing the surface morphology after silane overpressure annealing in SiH_4/H_2 Step bunching was observed to occur on numerous occasions motivating the development of a SiH_4/Ar process.

This research used a 3% silane in UHP Ar gas flow of 5 to 20 sccm with an Ar carrier gas flow of 2 slm and was conducted in a 30 mm cold-wall reaction tube[9]. Prior to annealing the material was n-type with a doping density of 4-5E15 cm^{-3}. After annealing the doping density was observed to be in excess of 1E19 cm^{-3} at the surface and was observed to be p-type.

Figure 4 shows the surface morphology of Al implanted n-type 4H-SiC after annealing. Note that the surface morphology was not affected during the annealing process, indicating that a sufficient overpressure of Si was present during the anneal. RBS measurements were also performed which indicate that the crystal quality, while degraded after the ion implantation process, was equal to the as-grown epitaxial layer quality.
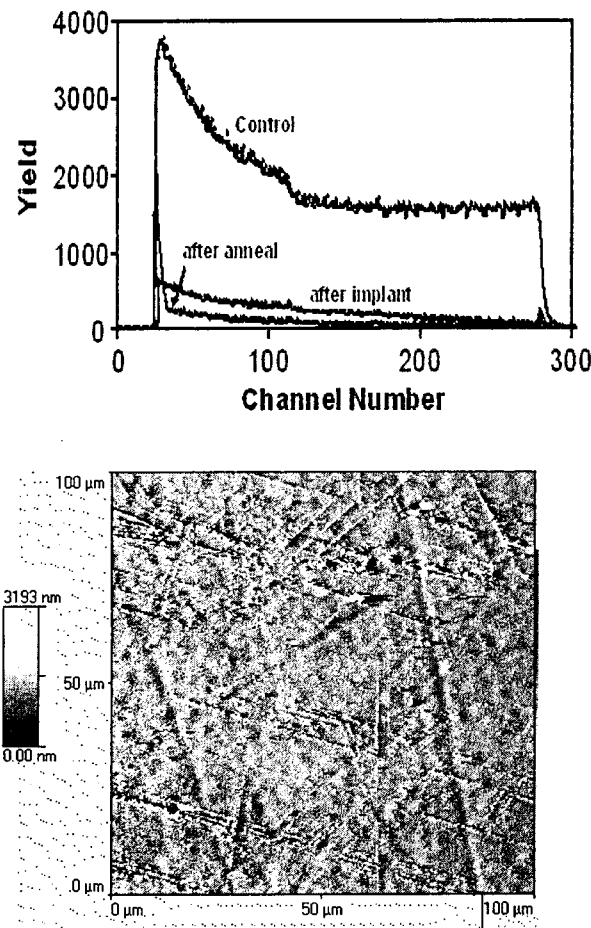

Fig. 5. Channeling RBS and AFM data of 4H-SiC annealed using the Silane/Ar process. Note crystal damage from implant has been repaired.

100 mm CVD Annealing Experiments

Once a stable process for Al implanted n-type 4H-SiC epitaxial layers was achieved, attention shifted to donor implants in p-type epitaxial layers. While it was intended to implant N+ into the p-type epitaxial layers using a TiN target, it was discovered that C+ was actually implanted into the material. While this did not permit us to correlate doping activation (as determined by CV) with atomic concentrations (as determined by SIMS), it did permit the evaluation of the mechanical stability of p-type epitaxial layers after implant anneals were performed. In addition, the crystal surface was investigated as a function of implant anneal conditions in an effort to optimize the implant annealing process. For this set of samples three ion implantation box profiles were designed to achieve net ion densities of 1E17, 1E18 and 1E19 cm^{-3} in the same p-type epitaxial layer.
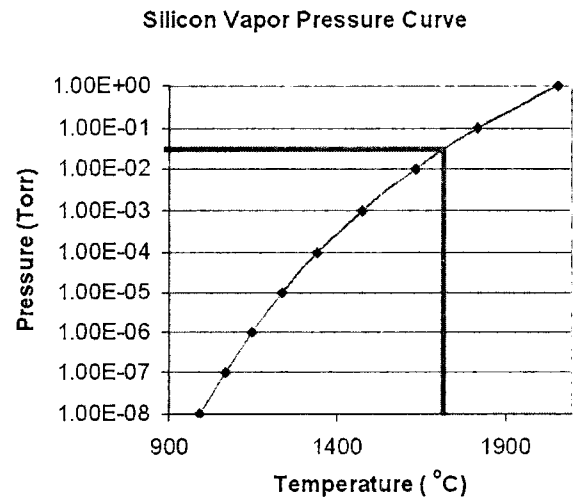

Fig. 6. Plot of the Si partial pressure versus Si vapor pressure for the 100 mm diameter tube annealing process described here. The Si vapor pressure was calculated for a Si wafer. Note the partial pressure exceeds the vapor pressure for the annealing temperatures as high as 1700°C.

The first step was to transfer the annealing process to the larger 100 mm CVD reactor used. This was basically a matter of optimization of the partial pressure of Si in the reactor during the annealing process. Calculations were conducted to ensure that the partial pressure of Si was greater than the vapor pressure of Si in the crystal. A process identical to the one described in the last section but with higher gas flow rates (which are needed since the

reactor cross section in the 100 mm tube is much larger than in the 30 mm tube) was experimentally investigated and it was determined that a Ar carrier flow of 6 slm with a silane in Ar mixture flow of 80 sccm resulted in excellent surface morphology after annealing. Using a standard thermodynamic analysis, a plot of partial pressure versus vapor pressure was formed (see Figure 6). Based on gas flows that were experimentally determined, and assuming a cracking efficiency of approximately 1% in the reactor, a partial pressure of Si at 1700°C of 100 mT was calculated.
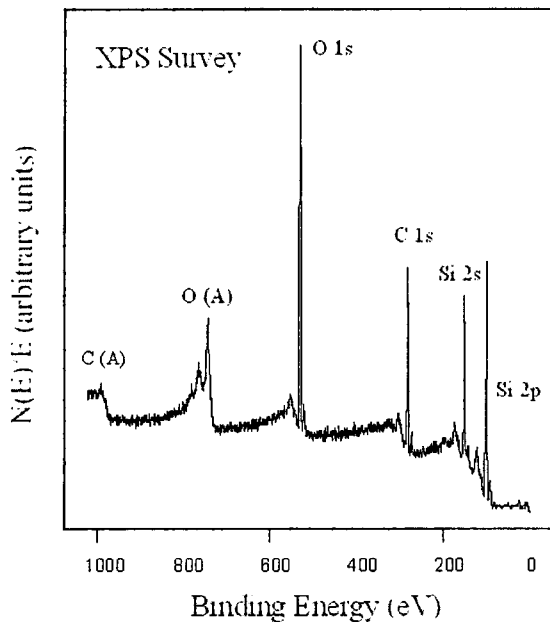

Fig. 7. XPS survey obtained from a C-implanted p-type 4H-SiC epitaxial layer after a 1600°C anneal. Besides the presence of O in the form of SiO_2 the surface consists primarily of Si and C.

At this temperature of vapor pressure of Si in a Si substrate would be approximately 20 mT, thus the partial pressure exceeds the vapor pressure and should suppress the outdiffusion of Si from the SiC crystal. A Si substrate was used since data for a 4H-SiC substrate was not available and also this would clearly be a worst-case scenario for the annealing process since Si-Si bonds are not nearly as strong as Si-C bonds.

Annealing experiments were performed at temperatures of 1400, 1500, 1600, and 1700°C, respectively. Based on the analysis shown in Figure 6, all processes were carried out with a silane in Ar mixture flow of 80 sccm. In an

effort to prevent elemental Si from forming on the crystal surface during the 1400 anneal, the flow was cut back to 60 sccm.

Figure 7 shows the results of an XPS survey conducted on the heaviest doped ($1E19$ cm^{-3}) sample annealed at 1700°C. With the exception of O, which is in the form of SiO_2 at the surface, elemental surface and near surface species consist exclusively of Si and C, indicating that after the annealing process the bulk species are preserved.

High resolution XPS data was taken for all the prominent photoelectric peaks shown in the survey to determine the chemical states of Si and C.
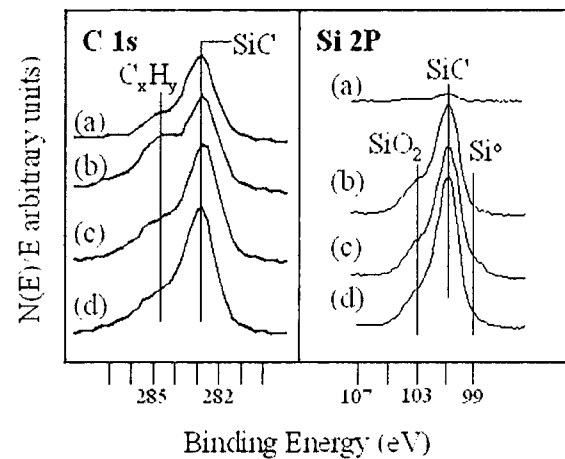

Fig. 8. High resolution XPS for the C 1s (left) and Si 2p (right) photoelectric peaks shown in Figure 6 as a function of annealing temperature. (a) before sample clean (b) after sample clean (c) after IA at 1400°C and (d) after IA at 1700°C. Si 2p shows evidence of elemental Si on the surface while the anneal at 1700°C does not. IA at 1600°C also did not show evidence of elemental Si on the surface (not shown).

In addition to inspection of the crystal surface using optical microscopy, the surface chemistry was evaluated using XPS.

For both species it was found that the predominate chemical state originates from SiC bonds. In fact, adventitious C, which is always present on air-exposed substrates, was of a much lower concentration than expected, givng further support to our assertion that the surface after annealing is in a nearly ideal state. High resolution XPS performed on the Si peak is shown in Figure 8. Since there is a genuine possibility of elemental Si forming on the crystal surface due to the silane

overpressure process, this data is particularly important. As seen in the figure, excess Si is present only on the 1400°C annealed sample despite the silane in Ar mixture flow being reduced. Fortunately for the other annealing temperatures no free Si was observed with XPS at the surface, indicating a near ideal process chemistry. That Si would form on the surface of 1400°C annealed crystals is also not unexpected since the melting point of Si at standard temperature and pressure is 1410°C which is clearly at the annealing temperature. Fortunately, SiC crystals may be annealed at 1400°C in Ar with little surface morphology degradation as we have demonstrated in our reactor.

3. SUMMARY

Implant anneal experiments were performed to develop a process schedule for silane overpressure annealing of ion implanted n-type and p-type SiC epitaxial layers. First the process was optimized by varying the process chemistry (silane in Ar) for an annealing of 1600 °C in a 30 mm cold-wall CVD reaction tube. The process was found to not only activate the ions but to leave the surface morphology in tact, as determined by optical microscopy, AFM and RBS measurements. Using a larger (100 mm) cold-wall CVD reaction tube, the process was modified for the necessary higher flow rates using C-implanted p-type 4H-SiC epitaxial layers. But investigating both n and p-type implanted epitaxial layers, process stability for either conductivity type was verified and it is believed that the process is robust up to 1600°C. Annealing conducted at 1700°C, while not resulting in step bunching, did result in a small amount of pitting, indicating that further process refinement is necessary for this implant temperature. However, most implant anneals can be conducted at 1600°C (for e.g., N in p-type epitaxial layers) and therefore the process developed and reported here will fulfill a majority of device process needs until the 1700°C process is optimized.

A surprising outcome of this research is the observation of nearly ideal surface chemistry after the anneals which indicates that anneals may be directly followed by additional epitaxial layer growth, which is of interest for buried structures in some device topologies.

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