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Electrical Characteristics of Metal/*n*-InGaAs Schottky Contacts Formed at Low Temperature

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Abstract

Schottky contacts on *n*-$In_{0.53}Ga_{0.47}As$ have been made by metal deposition on substrates cooled to a temperature of 77K. The current-voltage and capacitance-voltage characteristics showed that the Schottky diodes formed at low temperature had a much improved barrier height compared to those formed at room temperature. The Schottky barrier height, ϕ_B, was found to be increased from 0.2eV to 0.6eV with Ag metal. The saturation current density of the low temperature diode was about 4 orders smaller than for the room temperature diode. A current transport mechanism dominated by thermionic emission over the barrier for the low temperature diode was found from current-voltage-temperature measurement. Deep level transient spectroscopy studies exhibited a bulk electron trap at E_c - 0.23eV. The low temperature process appears to reduce metal induced surface damage and may form an MIS (metal-insulator- semiconductor)-like structure at the interface.

Key Words : Schottky barrier, Low temperature process, InGaAs, Current transport mechanism, Metal-semiconductor interface

1. Introduction

The III-V compound semiconductor $In_{0.53}Ga_{0.47}As$ lattice matched to InP is a promising material because of its high electron mobility and high saturation velocity. For this reason, *n*-$In_{0.53}Ga_{0.47}As$ is desirable for high speed and 1.3 μm optoelectronic applications. However, Schottky barrier height of a conventional diode on *n*-InGaAs prepared at room temperature (RT=300K) is too low (ϕ_B=~0.2eV) to be used for realization of good Schottky devices including FET applications. Several approaches have been made to fabricate elevated barrier height diodes to n-InGaAs using chemical passivation with $P_2S_5/(NH_4)_2S$[1], intentional surface oxidation in deionized water[2], ion-implantation with Be[3], a highly doped p^+-InGaAs interfacial interlayer[4], an excimer laser photodeposited Cd interlayer[5], and Pr_2O_3 and In_2O_3 interlayers in the liquid phase epitaxy[6].

Shi and Anderson have developed at low temperature (LT=77K) metal deposition to fabricated stable, high quality and high barrier height Schottky contacts to *n*-InP[7]. For evaporation with the substrate cooled to low temperature, evaporated metal films tend to be uniformly distributed on the semiconductor whereas this is often not the case at room temperature. A Pd/*n*-InP LT diode made by this

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cryogenic processing in their study showed on ultrahigh barrier height of 0.96eV and excellent long term stability. Their Raman spectroscopy studies indicated that the metal-semiconductor interface of the LT diode had an amorphous nature which served as a stable insulator and enhanced the barrier[8].

In this work, the same low temperature deposition process is applied to improve Schottky barrier height on *n*-InGaAs diodes[9]. Ag contacts formed on *n*-InGaAs substrates at room temperature and low temperature are studied by current-voltage-temperature (*I-V-T*) and capacitance-voltage-temperature (*C-V-T*) measurements to estimate the electrical characteristic parameters and to examine current transport mechanism in the LT diodes.

2. Experiment

The Schottky diodes used in this study were fabricated on 1.0μm thick *n*-InGaAs epilayers with two different free-carrier concentration of 1 x 10^{17} cm^{-3} (called S1 in this paper), and 5 x 10^{15} cm^{-3} (S2) grown on an n^+-InP substrate by MOVPE. There exist InGaAs and InP buffer layers between the top epilayer and the substrate. The diode fabrication consisted of three steps; i.e. ohmic contact on the back of the substrate, native oxide removal from the front of the InGaAs layer by chemical etching, and Schottky contact formation on the substrate cooled to low temperature[9]. First, the samples were sequentially cleaned by trichloroethylene, acetone, methanol and de-ionized water, and then blown dry with nitrogen gas. The ohmic contact was formed on an n^+-InP substrate by evaporating Au:Ge/Ni and alloying by rapid thermal annealing (RTA) at 360℃ for 10s. A proximity cap was also used to protect the front surface during the annealing process. The native oxide on the front surface of the sample was then removed by wet chemical etch with diluted H_2SO_4 solution for 60s. After the samples were rinsed in de-ionized water and blown dry with hydrogen gas, they were quickly loaded into an evaporator. Schottky metals Au or Ag, 1000Å thick, were deposited on the *n*-InGaAs layers at a substrate temperature of 77K under a high vacuum of 2 x 10^{-7}torr. The low temperature was achieved by continuous liquid nitrogen flow into the sample holder and monitored with a chromel-alumel surface mounted thermocouple.

The *I-V-T* and *C-V-T* characteristics of the 0.8mm^2 diodes were measured from 100K and 300K in an auto data acquisition cryogenic system. The DLTS measurements were performed in a Polaron DL4600 deep level transient spectrometer system with temperature from 100K to 380K. The reverse bias was kept at -0.5V while the filling pulse was changed from 0 to 0.4V to distinguish the bulk and interface traps.

3. Results and discussion

Figure 1 and Table 1 show the room temperature current-voltage (*I-V*) characteristics

Table 1. Electrical characteristics for InGaAs LT diodes

Sample	Metal	N_D(cm^{-3})	ϕ_{BIV}(eV)	ϕ_{BCD}(eV)	n	V_{BR}(V)	J_R at -1V(Acm^{-2})
S1-1	Au	1 x 10^{17}	0.49	0.51	1.66	~1.5	4.0 x 10^{-2}
S1-2	Ag	1 x 10^{17}	0.57	0.59	1.32	~5.0	2.0 x 10^{-4}
S2-1	Au	5 x 10^{15}	0.50	0.52	1.57	~3.0	5.0 x 10^{-3}
S2-2	Ag	5 x 10^{15}	0.60	0.61	1.23	~6.0	8.7 x 10^{-5}

It is impossible to calculate meaningful diode characteristics from RT diodes due to their near-ohmic behavior.

and processed data for Ag/InGaAs RT and LT diodes. *I-V* characteristics for Au/InGaAs LT diodes are also presented in the same table. The device behavior is clearly dependent on the substrate temperature during metal deposition, the choice of metal and free carrier density. For the RT diodes, the *I-V* characteristics look almost ohmic due to their low Schottky barrier height. For the LT diodes, however, higher barrier heights Φ_B calculated from the following Eq. 1 were obtained:

$$J_0 = A^*T^2\exp(-\Phi_B/kT), \quad (1)$$

where J_0 is the saturation current density and A^* = 5.04Acm^{-2}K^{-2} is the Richardson constant of *n*-InGaAs. The ideality factor, *n*, was determined from the forward current characteristics using the relation:

$$n = (q/kT)[\partial V/\partial(\ln J)] . \quad (2)$$

For Au/*n*-InGaAs LT devices (S1-1), Φ_B and *n* were found to be 0.49eV and 1.66, respectively. For Ag/*n*-InGaAs devices (S1-2), Φ_B and *n* were 0.57eV and 1.32, respectively. Compared with the RT diode, the reverse leakage current density of the LT diode was reduced by 3 to 4 orders. The highest barrier height was obtained from Ag/*n*-InGaAs LT diodes fabricated on a substrate with N_D = 5 x 10^{15}cm^{-3}. The barrier height Φ_B and an ideality factor *n* for S2-2 were 0.60eV and 1.23, respectively. The breakdown voltage V_{BR} of S2-2 was also much improved to a value of more than 6V. A 5 order reduction of the reverse leakage current was obtained for this sample and a soft reverse current characteristic was not observed. Ni, Cr, Pd and Al were also tried as a barrier metal, but no significant improvement of barrier height was observed. It is interesting that for all LT diodes, Schottky barrier height and reverse current characteristics were better with Ag compared to Au. This relates to Ag as the only metal studied to date which shows no tendency to chemically bond to or react with GaAs[10]. Also, the surface chemistry of InGaAs is similar to that of GaAs[1]. Even at the low temperature, Ag may have less probability to cause chemical reactions with the substrate compared to Au. Thus, the

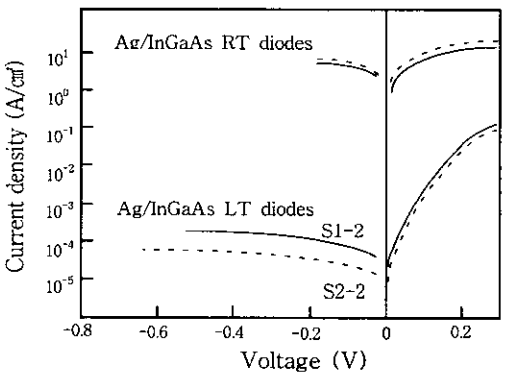

Fig. 1. Room temperature I-V characteristics for RT and LT diodes.

barrier height changes for the Ag barriers could be due to a change in the InGaAs substrate caused by low temperature processing.

The barrier heights from 1MHz capacitance-voltage (*C-V*) measurement were in good agreement with those from *I-V* measurement, which indicates the lack of frequency dependence of interface states. The effective barrier height was calculated from the expression:

$$\Phi_B = V_i + \xi + kT/q, \quad (3)$$

where V_i is the built-in potential, and ξ is the potential difference between the Fermi-level and the conduction band-edge. From Eq. 3, the Schottky barrier heights of Ag/InGaAs LT diodes S1-2 and S2-2 at 300K were determined to be 0.59 and 0.61eV, respectively. *C-V-T* characteristics were also measured for S1-2 and S2-2 in the temperature range of 100-300K. Good

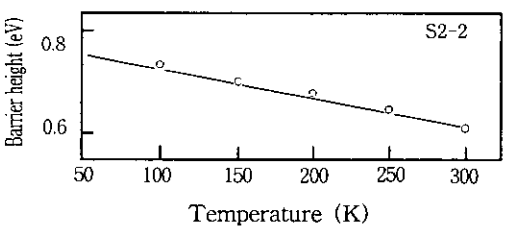

Fig. 2. Temperature dependence of zero-bias barrier heights for the Ag/InGaAs LT diode.

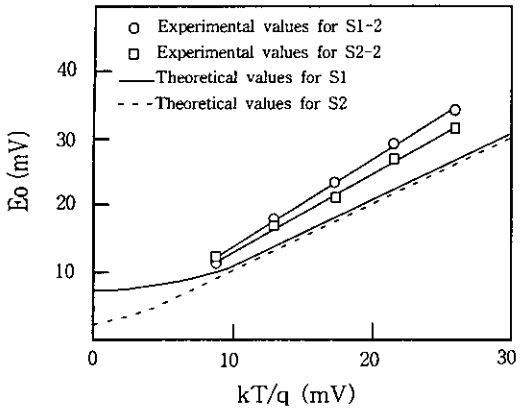

Fig. 3. Temperature dependence of E_0 for Ag/InGaAs LT diodes.

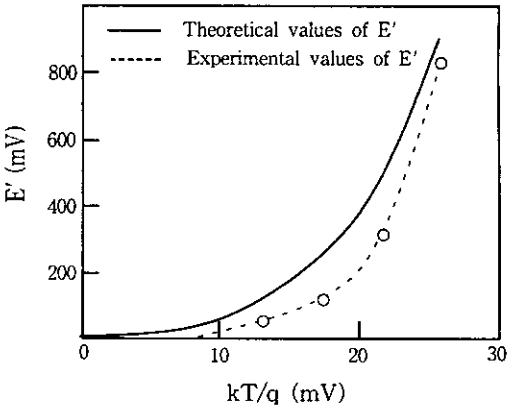

Fig. 4. Theoretical and experimental values of E' as a function of temperature for diode S1-2.

linearity was shown over the entire temperature range at reverse bias less than 1.5V. Temperature dependence of zero bias barrier height ϕ_{B0} is described by:

$$\phi_{B0} = \phi_0 + \beta T, \quad (4)$$

where ϕ_0 is the barrier height at zero temperature and zero bias, and β is the temperature coefficient of zero bias barrier height. The values of ϕ_{B0} vs temperature are shown in Fig. 2. The experimental values of ϕ_{B0} fit well to Eq. 4 with ϕ_0 = 0.78eV and β = -6.0 x 10^{-4}eVK^{-1} for S2-2.

Figure 3 shows experimental and theoretical values of E_0 as a function of temperature for samples S1-2 and S2-2 under forward bias. E_0 is a characteristic value dependent on the transport mechanism of carriers through the barrier[11]. Theoretically, sample S2-2 should give TE(thermionic emission) as a transport mechanism in all of the temperature regions due to its low doping concentration. Tunneling can be expected for sample S1-2 in the low temperature region less than 100K due to its rather high doping concentration. Experimentally, S1-2 and S2-2 showed a conduction dominated by thermionic emission in a measured temperature region from 100 to 300K. But, ideality factors were a little larger than unity as a deviation from the theoretical curve. Large ideality factors observed from Ag/InGaAs LT diodes are possibly related to a thin interface layer having an amorphous structure. This is also confirmed by a low value of measured Richardson constant[12]. The Richardson constant of 0.37Acm^{-2}K^{-2} and the activation energy of 0.51eV for the Ag/InGaAs LT diode were found from a Richardson plot $\ln(J_0/T^2)$ against $1000/T$.

The reverse current for S1-2 with a high free carrier concentration was found to be independent of temperature with increase of bias. Its reverse current at a fixed bias was exponentially higher with a decrease of temperature compared to a low doped sample S2-2. Theoretical and experimental curves of E' as a function of kT/q are shown in Fig.4, where E' is a characteristic value under reverse bias[11]. The two plots do not match perfectly due to steep increase of reverse current but a similar shape is observed. Using the theoretical value for E_0 at 0K for S1 and the boundary conditions from Padovani and Stratton[11], even field emission may be considered at low temperature less than ~100K with the reverse bias higher than 0.1V. Thus, this excess reverse current may be attributed to a tunneling current component due to a high barrier and high doping density.

This low temperature process also made it possible to measure deep level transient spectroscopy spectra shown in Fig. 5 since leakage current was low. One electron trap

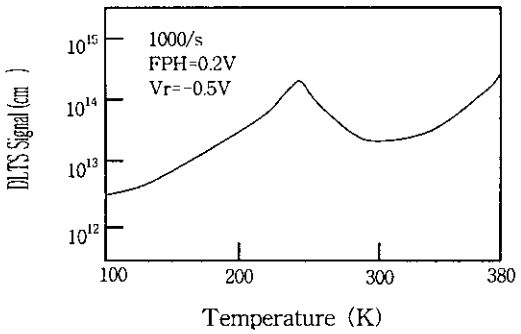

Fig. 5. A DLTS curve for the low temperature sample.

located at E_c - 0.23eV was identified as a bulk trap. No surface trap was found.

Several models for the metal-semiconductor interface have been proposed, relying on effective work functions, defects at the interface, reactivity between metal and semiconductor, and the inhomogeneous Schottky barrier model[12-13]. For the LT diode, a combined type with the models mentioned above should likely be considered, because metal deposition at LT has shown a low trap density, uniform metal coverage and nonreactivity of Ag[9]. The fundamental mechanisms determining the Schottky barrier height for the InGaAs LT diodes are so far not well understood. Further investigation using structural analysis technique can be needed to correlate the LT film with the electrical characteristics.

4. Conclusions

The LT process provides a simple way to improve the Schottky barrier height on n-$In_{0.53}Ga_{0.47}As$ from ~0.2 to 0.60eV with Ag metal. Compared with the RT diode, the reverse leakage current density of the LT diode is reduced by five orders. From I-V data for the Ag/InGaAs LT diodes, it is found that the forward and reverse I-V-T characteristics are dependent on the free carrier concentration of n-InGaAs layers. A relatively high free carrier concentration and the enhanced barrier height of the sample increase the tunneling component of the reverse current and lead to a large leakage current. For the low doped LT sample, however, thermionic emission is a dominant conduction mechanism over the Schottky barrier. This low temperature process also makes it possible to measure the DLTS spectra. A bulk electron trap for LT diodes is found and its activation energy is ~0.23eV. The improvement in ϕ_B and reverse leakage current with LT metal deposition could be attributed to the uniform metal coverage on an InGaAs surface and the formation of an amorphous-like structure instead of an alloy layer at the metal-semiconductor interface. Thus, metal induced surface damage can be greatly reduced by LT processing and the amorphous layer could serve as an insulator to make the LT diode an MIS-like structure.

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