Application of Correlation-Aided DSA(CDSA) Technique to Fast Cell Search in IMT-2000 W-CDMA Systems

Byoung-Hoon Kim, Byeong-Kook Jeong, and Byeong Gi Lee

Abstract: **In this paper, we introduce the *correlation-aided distributed sample acquisition* (CDSA) scheme for fast cell search in IMT-2000 W-CDMA cellular systems. The proposed scheme incorporates the *state symbol correlation process* into the *comparison-correction based synchronization process* of the original DSA scheme to enable fast acquisition even under very poor channel environment. For its realization, each mobile station (MS) has to store in its memory a set of state sample sequences, which are determined by the long-period scrambling sequences used in the system and the sampling interval of the state samples. CDSA based cell search is carried out in two stages: First, the MS first acquires the slot timing by using the *primary synch code* (PSC) and then identifies the *igniter code* which conveys the state samples of the current cell. Secondly, the MS identifies the scrambling code and frame timing by taking the comparison-correction based synchronization approach and, if the identification is not done satisfactorily within preset time, it initiates the state symbol correlation process which correlates the received symbol sequence with the pre-stored state sample sequences for a successful identification. As the state symbol SNR is relatively high, the state symbol correlation process enables reliable synchronization even in very low chip-SNR environment. Simulation results show that the proposed CDSA scheme outperforms the 3GPP 3-step approach, requiring the signal power of about 7 dB less for achieving the same acquisition time performance in low-SNR environment. Furthermore, it turns out very robust in the typical synchronization environment where large frequency offset exists.**

Index Terms: **Correlation-aided distributed sample acquisition, state symbol correlation process, comparison-correction based synchronization process, primary synchronization code (PSC), igniter code, 3GPP 3-step synchronization approach.**

I. INTRODUCTION

The DS/CDMA cellular systems for IMT-2000 services take two different forms depending on cell-site reference time synchronization scheme: The inter-cell *asynchronous* system [1], [2] and inter-cell *synchronous* system [3], respectively supported by the *third generation partnership project* (3GPP) and the 3GPP2 associations. The inter-cell synchronous system relies on the external timing reference source such as *global positioning systems* (GPS) and uses different time-shifted versions of a single PN sequence as the forward link scrambling code of each cell site. This single code scheme enables each mobile station (MS) to acquire the scrambling codes in relatively short time with simple hardware. On the other hand, the inter-cell asynchronous system assigns different PN sequences to different cell sites, eliminating the dependency on external timing references. Consequently, very sophisticated and complex synchronization schemes are needed to acquire the scrambling codes within the allowed time limit, and the code identity and the time shift have to be searched simultaneously [1], [2], [4].

For a fast acquisition of the scrambling codes in the inter-cell asynchronous systems, the 3GPP three-step synchronization scheme based on the *generalized hierarchical Golay* (GHG) code [5] and the *Comma-free* code [2], [6] has been proposed and regarded as a promising candidate of the IMT-2000 W-CDMA cell search (or, initial code synchronization) standard [7], [8]. The three steps in this scheme refer to slot boundary identification, code group and frame boundary identification, and cell-specific primary scrambling code identification. For the first and the second steps, each base station (BS) respectively broadcasts the primary synchronization code (PSC) and the secondary synchronization code (SSC) of length 256 each through the synchronization channel (SCH) at every beginning of the slot. In the third step, the cell-specific primary scrambling code is identified by correlating all candidate scrambling codes belonging to the identified code group with the incoming primary common control physical channel (CCPCH) sequence.

Recently, the harmonization efforts among the 3GPP and the 3GPP2 associations have brought in the common pilot channel (CPICH), which used to be exclusively adopted in the inter-cell synchronous systems [3], [9], for use in the inter-cell asynchronous W-CDMA systems as well [10]. While its main use is in tracking the incoming signal and estimating the channel gain, it also accompanies new challenges to fast and efficient cell search. Note that the common pilot has been widely used for scrambling sequence acquisition in the inter-cell synchronous systems.

As a potential challenge to using the CPICH for cell search in the inter-cell asynchronous IMT-2000 W-CDMA system, we are going to present in this paper a novel approach called *correlation-aided distributed sample acquisition* (CDSA). Distributed sample acquisition (DSA) is a recently introduced fast long-sequence acquisition technique that employs a short sequence called *igniter sequence* to modulate the CPICH for broadcasting of the *state samples* of the transmitter's long-sequence generator and employs comparison-correction technique for the synchronization of receiver's long-sequence generator [11]–[15]. The CDSA incorporates a *state symbol correlation process* into the *comparison-correction based synchronization* process of the DSA to yield a fast and robust two-stage

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cell search scheme for the IMT-2000 W-CDMA systems. As will become clear through extensive performance comparisons in later sections, the CDSA substantially outperforms the 3GPP three-step approach in terms of code acquisition time and system power consumption.

The paper is organized as follows: In Section II we describe the organization and operation of the CDSA based inter-cell asynchronous IMT-2000 W-CDMA systems. We consider the case of employing differential quadrature phase shift keying (DQPSK) as the target modulation scheme. Then, in Section III, we evaluate the mean acquisition time performance of the CDSA approach in Rayleigh fading channels through computer simulations, comparing it with the 3GPP three-step case. We also examine and compare the system implementation complexity between two approaches.

II. CELL SEARCH THROUGH CDSA IN IMT-2000 W-CDMA SYSTEMS

In the IMT-2000 W-CDMA systems, a cell (or sector) may use multiple scrambling codes to enhance the downlink code capacity [7]. Included among them is the primary scrambling code which is uniquely determined by the cell-number and used to scramble the primary CPICH and the primary CCPCH. In the initial cell search process an MS identifies and synchronizes the primary scrambling code of the cell currently located. The primary scrambling code allocated to each BS is a segmented *complex* Gold sequence of length 38,400. In fact, the I-phase primary scrambling sequence is this segmented Gold sequence which is obtained by binary-adding two sets of the first 38,400 m-sequence segments respectively generated by two different shift register generators (SRG) having the characteristic polynomials $\Psi_1(x) = x^{18}+x^7+1$ and $\Psi_2(x) = x^{18}+x^{10}+x^7+x^5+1$ respectively. We assume that the cellular system is composed of 512 cells numbered from 1 to 512 and that the first m-sequence generator (or, main SRG-1) of each BS is initially loaded with the cell-number and the second m-sequence generator (or, main SRG-2) with all-1 string. We decimate the two segmented m-sequences by the decimation period of 256 chips to get two *state sample sequences* of period 150 each, with each sequence corresponding to a different segment of the original m-sequences. Then we get 512 different sequences of period 150, $\{z_{i,\,k}^{(1)} : i = 0, 1, \cdots, 149, \cdots\}$, $k = 1, 2, \cdots, 512$, for the first m-sequences of 512 BS's, and one sequence $\{z_i^{(2)} : i = 0, 1, \cdots, 149, \cdots\}$ for the second m-sequences. These 513 available sample sequences of length 150 each are stored in advance in the ROM of each MS. On the other hand, the Q-phase primary scrambling sequence is obtained by taking the first 38,400 sequence values of the time-lagged version (lagged by 131,072 chips [7]) of the Gold sequence used for I-phase primary scrambling code generation. According to the shift-and-add property of the constituent m-sequences, the Q-phase sequence can be easily generated from the main SRG-1 and main SRG-2 by employing the corresponding *sequence generating vectors* [16]. Since the system chip rate is 3.84 Mcps [10], the period of the primary scrambling sequence is commensurate with 10 ms, which corresponds to the frame time of the transmitted signals. The frame is composed of 15 slots of length 2,560 chips each.

In the following we detail the CDSA scheme for the DQPSK modulation system.

Fig. 1 depicts the functional block diagram of the BS and MS in the kth cell ($k = 1, 2, \cdots, 512$) of the cellular system that employs the DQPSK-based CDSA scheme. The time-advanced sampling block of the BS takes the *state samples* $z_{r+i,\,k}^{(1)}$ and $z_{r+i}^{(2)}$ out of the main SRG-1 and the main SRG-2 at time $(r+i-1) \times 256T_c$, for a reference value r, and supplies them to the DQPSK modulator. The main SRG-1 and the main SRG-2 are the m-sequence generators that respectively generate the first and the second segmented m-sequences of length 38,400. The DQPSK modulator first maps the two state samples to the I-phase and the Q-phase of the QPSK constellation to generate the *state symbol* $x_{r+i,\,k}$, and then produces the differentially encoded symbol $f_{r+i,\,k}$ by adding the phase of $x_{r+i,\,k}$ to the phase accumulated up to the previous symbol time. As the period of the primary scrambling code (38,400 chips) is a multiple of the sampling period (256 chips), the resulting state symbol sequence $\{x_{r+i,\,k}\}$ also becomes periodic, with the period being 150 symbols. The differentially encoded symbol $f_{r+i,\,k}$ is broadcast through the primary CPICH channel in the time interval $[(r+i-1) \times 256T_c, (r+i) \times 256T_c)$.

The spreading sequence of the primary CPICH channel $\{c_{m,\,k}\}$, which we call the *igniter sequence* of the cell, is one of the 16 short sequences of length 256. The short sequences used in this paper are the complex orthogonal Gold sequences [2] but may be changed into another set of sequences for improved performances (For example, the set of 16 Hadamard-modulated Golay codes used for secondary SCH of the 3GPP three-step approach [7] may be used as the igniter sequence set.). The multiple short sequences are necessary for the spatial separation of co-code cells, each of which has a one-to-one correspondence with each cell group composed of 32 cells.

In parallel with the primary CPICH transmission, the PSC symbols spread by the GHG code of length 256 are broadcast through the SCH at the beginning of each slot for fast synchronization of the slot boundary. During the period when the PSC symbols are not transmitted, the broadcast channel (BCH) symbols are transmitted through the primary CCPCH. However, the SSC is not transmitted in the proposed CDSA scheme, thereby making all the SCH power be used for slot boundary acquisition only, without being divided into two for slot boundary acquisition and frame/group identification as is done in the 3GPP 3-step scheme case. On the other hand, each user's M-ary PSK data $\{a_{r+i,\,k}^{[l]}\}$ is spread by an orthogonal Walsh sequence $\{w_m^{[l]}\}$ and scrambled by the primary or one of the secondary scrambling sequences of the cell, and then transmitted as the data signal.

Fig. 2 depicts the timing relations among the synch-related common signals transmitted from the BS. The primary CPICH, the SCH, the primary CCPCH, and the other data and control signals go through the same channel to the MS. We assume the single path Rayleigh fading channel in the paper, which is the worst-case channel model as far as the initial synchronization process is concerned [6].

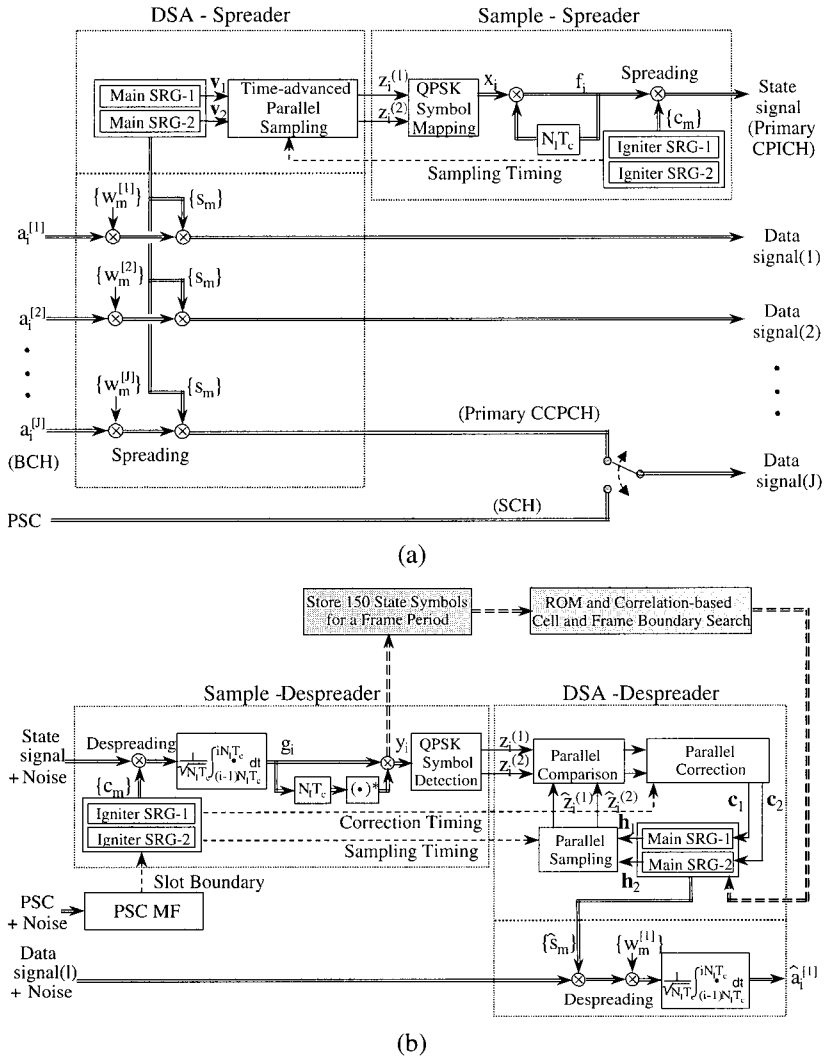

Fig. 1. Functional block diagram of the acquisition-related part of the IMT-2000 W-CDMA system employing the DQPSK-based CDSA scheme: (a) base-station (transmitter), (b) Mobile-station (receiver).

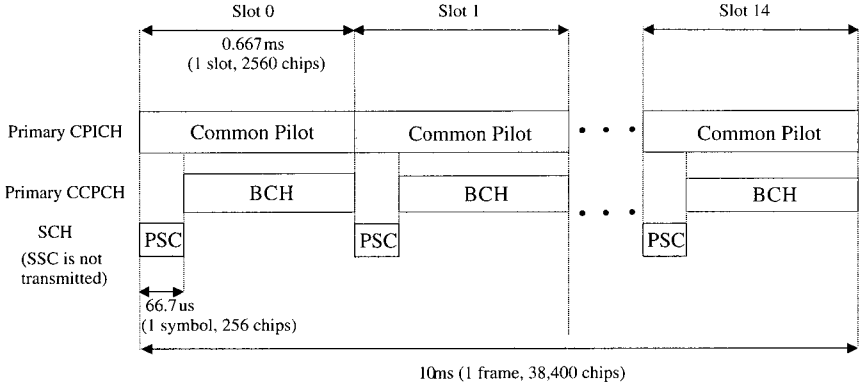

Fig. 2. Timing relations among the primary CPICH, SCH, and primary CCPCH.

A. (First Stage) Slot Boundary Acquisition and Igniter Sequence Identification Process

The MS first acquires the slot boundary by using the PSC, for which we take the first step of the 3GPP three-step approach, i.e., the matched filtering with the Golay correlator. More specifically, the MS first takes a discrete sample stream by sampling the incoming analog signal at every half chip interval. Then, it stores 5,120 correlation values per slot obtained by correlating the sample stream with the PSC by employing the Golay correlator of length 256 [5]. Finally, it acquires the slot boundary by taking the sample position that produces the maximum correlation energy out of the 5,120 candidate positions. For an improved acquisition performance in the fading channel,

we usually take the slot-wise energy accumulation throughout S slots before taking the sample position having the maximum correlation energy [6].

After acquiring the slot boundary, the MS identifies the igniter sequence broadcast in the current cell by correlating the incoming primary CPICH signal with 16 candidate igniter sequences in parallel and then determining the sequence having the maximum correlation energy. We take the symbol-wise energy accumulation throughout V_I primary CPICH symbols for an improved identification performance. By verifying whether or not the square-rooted maximum correlation energy overtakes a pre-specified threshold value R_I, we can also confirm whether or not the slot boundary is truly synchronized. If the square-rooted maximum energy turns out to overtake R_I, the first step terminates, but otherwise, the slot boundary acquisition step resumes. Once one of the 16 igniter sequences is determined, the cell uncertainty reduces from 512 to 32, according to the mapping relation between the igniter sequences and the co-code cells.

B. *(Second Stage) Main SRG Synchronization and State Symbol Correlation Process*

B.1 Comparison-correction based main SRG synchronization

Once the slot boundary is acquired, the MS then acquires the primary scrambling code through the *comparison-correction based main SRG synchronization* process. For this, the MS first despreads the received primary CPICH signal $r(t)$ using the acquired igniter sequence to get the *soft CPICH symbol* g_{r+i} and then multiplies it to the conjugate of the previously obtained symbol g^*_{r+i-1} to get the *soft state symbol* y_{r+i}. More specifically, if we denote by P_s the primary CPICH signal power, by $f_{n,\,k} \equiv e^{j\theta_{n,\,k}}$ the nth DQPSK symbol, by $c_k(t) \triangleq \sum_{m=0}^{255} c_{m,\,k} p_{T_c}(t - mT_c)$ the igniter sequence of the kth BS,[1] by $N(t)$ the channel noise, by H the channel gain, by ω_o the frequency alignment offset, by ϕ the carrier phase, and by ηT_c the fractional chip alignment offset, then we get the expressions

$$r(t) = \sum_{n=-\infty}^{\infty} \sqrt{P_s} H e^{j(\omega_o t + \phi + \theta_{n,\,k})} \times c_k(t + \eta T_c - [n-1] \times 256T_c) + N(t), \quad (1)$$

$$g_{r+i} = \frac{1}{\sqrt{256T_c}} \times \int_{256(r+i-1)T_c}^{256(r+i)T_c} r(t) c_k^*(t - [r+i-1] \times 256T_c) dt, \quad (2)$$

and

$$y_{r+i} = g_{r+i} g^*_{r+i-1}. \quad (3)$$

The channel noise is assumed complex white Gaussian distributed, with its I-phase and Q-phase components both having the power spectral density of $N_0/2$.

[1] We define $p_w(t)$ to be the pulse shaping function which is 1 in $[0, w]$ and 0 elsewhere.

The DPSK symbol detection block then determines the conveyed state samples $z^{(1)}_{r+i,\,k}$ and $z^{(2)}_{r+i}$, which are then passed to the DSA-despreader at time $(r+i) \times 256T_c$. On the other hand, the DSA-despreader generates its own state samples $\hat{z}^{(1)}_{r+i}$ and $\hat{z}^{(2)}_{r+i}$ at time $(r+i) \times 256T_c$ from the MS main SRG-1 and main SRG-2, and compares them with the conveyed counterparts $z^{(1)}_{r+i,\,k}$ and $z^{(2)}_{r+i}$. If $\hat{z}^{(1)}_{r+i}$ and/or $\hat{z}^{(2)}_{r+i}$ do not coincide with $z^{(1)}_{r+i,\,k}$ and/or $z^{(2)}_{r+i}$ respectively, the corresponding jth $(j = 1, 2)$ correction circuit $\mathbf{c}_j$ is triggered to correct the state of the main SRG-j at time $(r+i) \times 256T_c + D_c T_c$, with D_c chosen such that $0 < D_c \leq 256$. Otherwise, no action takes place. If we employ a pair of sampling and correction circuits independently designed for main SRG-1 and main SRG-2 according to the theorems in [11], the MS main SRGs will get synchronized to the BS main SRGs whenever 18 successive state symbols are conveyed without any detection errors.

For fear that there may occur one or more detection errors while detecting the 18 symbols, we observe $V = 7$ additional symbols to verify the synchronization. Since the main SRGs in the BS and the MS generate the same sequence samples after the true synchronization, we can verify the synchronization by comparing the observed samples with the MS generating samples. If the conveyed and receiver-generated symbols indeed coincide for all V symbol pairs, then the MS declares completion of synchronization of the primary scrambling sequence, beginning to track and estimate the channel gain and carrier phase. If less than V symbol-pairs coincide, the MS restarts the comparison-correction based main SRG synchronization using another set of 18 successive state symbols. Therefore, it nominally takes 25 state symbol periods (i.e., 1.66 ms) to complete a run of this main SRG synchronization process of the CDSA, but it could take multiple runs in poor channel environments as detection errors would occur more frequently.

B.2 State symbol correlation

To prevent unbounded runs going in the main SRG synchronization process, we initiate a synch-termination process after detecting 150 soft state symbols, by correlating them with the pre-stored state sample sequences. This state symbol correlation process is composed of two phases—frame boundary detection and cell number detection. For frame boundary detection, we first correlate the soft state symbol sequence $\{y_{10\tilde{r}+i} : i = 0, 1, \cdots, 149\}$, for an arbitrary integer $\tilde{r}$, with the 15 shifted versions of the pre-stored second state sample sequence $\{w^{(2)}_{10n+i} : i = 0, 1, \cdots, 149\}$, $n = 0, 1, \cdots, 14$, where $w^{(2)}_i \triangleq (-1)^{z^{(2)}_i}$. Note that the timing reference r is set to $10\tilde{r}$, which indicates that the soft state symbol collection begins at the start of a slot, taking advantage that the slot boundaries are readily acquired in the slot identification step. Then we compare the resulting 15 correlation energy values

$$E_{n,\,frame} = \left| \frac{1}{\sqrt{150}} \sum_{i=0}^{149} y_{10\tilde{r}+i} w^{(2)}_{10n+i} \right|^2, \quad n = 0, 1, \cdots, 14, \quad (4)$$

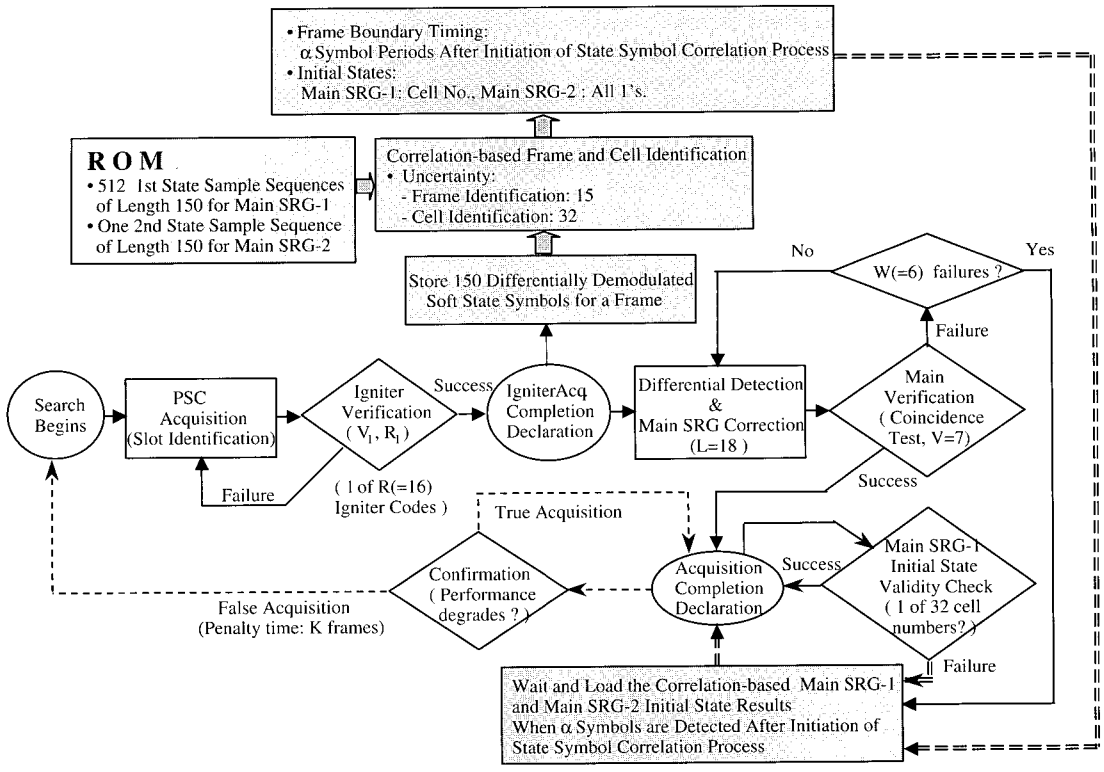

Fig. 3. Block diagram outlining the CDSA-based cell-search process for IMT-2000 W-CDMA systems. (The blocks in shade are those related to state symbol correlation process.)

and determine the time shift number $n = n_0$ at which the correlation energy becomes maximum as the frame boundary. For cell number detection, we correlate the soft state symbol sequence $\{y_{10\tilde{r}+i} : i = 0, 1, \cdots, 149\}$ with the 32 candidate (first state sample) sequences obtained at the end of the igniter sequence identification process. More specifically, if the acquired igniter sequence $\{c_k(t)\}$ is mapped to the 32 co-code cells using the first state sample sequences $\{z^{(1)}_{i,\,q}\}$, $q = 1, 2, \cdots, 32$, we compare the 32 correlation energy values

$$E_{q,\,cell} = |\frac{1}{\sqrt{150}} \sum_{i=0}^{149} y_{10\tilde{r}+i} w^{(1)}_{10n_0+i,\,q}|^2, \quad q = 1, 2, \cdots, 32, \tag{5}$$

where $w^{(1)}_{i,\,q} \triangleq (-1)^{z^{(1)}_{i,\,q}}$, and determine the cell number $q = q_0$ at which the correlation energy becomes maximum. Now that the frame boundary information n_0 and the cell number information q_0 are both available, we can complete the cell search by loading the corresponding initial state values (or, the cell number information) to the first main-SRG and loading the all-1 string to the second main-SRG at the moment the next frame boundary begins. This completes the second stage synchronization process.

In the state symbol correlation process, we deliberately use the *differentially demodulated* state symbols to enhance the robustness of the scheme in the frequency offset environment. If there were no frequency offset at all, the CPICH symbols $\{g_i\}$ would yield better correlation performance than the state symbols $\{y_i\}$ does, as the state symbols accompany higher noise variances due to the differential demodulation process. In reality, however, frequency offset is unavoidable in any initial synchronization process, and CPICH symbol based correlation degenerates even at a small amount of frequency offset because the symbols are collected over relatively long period (i.e., a frame time, 10 ms). By using differentially demodulated symbols for the correlation, we can maintain normal correlation performances unless the frequency offset becomes exceedingly high to cause a considerable phase angle rotation during the symbol interval.

C. Supplemental Processings

Once the cell search is completed by way of the comparison-correction based SRG synchronization process, we declare synchronization, but at the same time we carry out a validity test by checking whether or not the state of the first m-sequence generator takes one of the 32 valid cell numbers when the state of the second m-sequence generator takes all-1 string. This test can be done within a frame time. If this validity test fails, we recall the synchronization declaration and load the main SRGs with the initial state values determined through the state symbol correlation process.[2] Fig. 3 depicts the resulting overall cell search

[2]If the all-1 state does not appear in the main SRG-2 by the frame boundary time determined by the state symbol correlation process, the synchronization declaration is regarded as a false alarm, and the initial states obtained in the state symbol correlation process are loaded. The state validity check can be done even before the all-1 state appears in the main SRG-2 at the cost of increased memory use by pre-storing more state mapping data between the two main SRGs of the 512 cells.

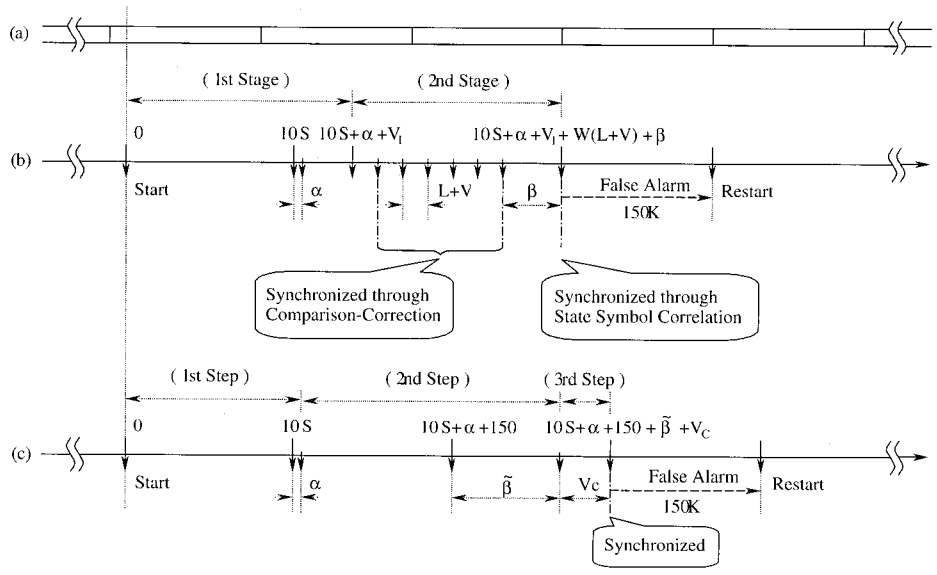

Fig. 4. Synchronization timing diagram of CDSA and 3GPP 3-step schemes: (a) primary CPICH frames, (b) CDSA scheme, and (c) 3GPP 3-step scheme (see Section II-C for the definition of parameters).

process (see the solid line part). Despite these verification and validity tests, there still exists a small probability of false acquisition, no matter how small it may be. Thus we keep monitoring the data decoding performance even after the acquisition completion declaration. If a false acquisition is really detected in this stage, the MS recalls the declaration of the synch-completion and restarts the slot boundary search stage, which may be modeled by a delay of K frame times, i.e., $K \times 10$ ms (see the dashed line part).

Once the synchronization process is done, with the MS igniter and main SRGs synchronized to those in the BS, the MS first despreads the data signal by multiplying the conjugate of the corresponding primary (or secondary) scrambling sequence and the corresponding Walsh sequence. It then regenerates the broadcasted primary CPICH signal (only with an initial phase difference involved in the DQPSK modulator), and estimates the channel characteristics in a way similar to that of the conventional DS/CDMA cellular systems employing the unmodulated pilot sequences [18]. Finally it coherently demodulates the despread data using the channel estimation results. Detailed discussions on the channel estimation, including solutions to the phase ambiguity problem that happens when using a DQPSK-modulated pilot, can be found in the reference [14].

The potential disadvantage of introducing short codes in spreading the primary CPICH is that the capacity may reduce due to the non-orthogonality between the pilot and the traffic/control channels. However, the non-orthogonality problem can be effectively resolved by employing the pilot cancellation technique [17], [19], which can be easily implemented as the necessary parameters such as signal delay and gain information are readily estimated to coherently demodulate and maximally combine the data in the RAKE detector. Moreover, the probable introduction of the multiple scrambling codes in a cell [7] would break the orthogonality and thus require the pilot cancellation technique inevitably. The phase ambiguity problem of the CPICH introduced by employing the differential encoding technique can be resolved by observing the phase of the *dedicated* pilot symbols transmitted in the traffic/control channels or by employing the data constellation pre-rotation technique introduced in [14].

Fig. 4 depicts the synchronization timing diagram of the DQPSK-based CDSA scheme in comparison with that of the 3GPP 3-step scheme: Fig. 4(a) shows the frame boundaries of the primary CPICH signal arriving at the MS, with each block indicating 38,400 chip time (10 ms). Fig. 4(b) and (c) respectively show the overall synchronization timing of the CDSA scheme and the 3GPP 3-step scheme, with unit time indicating 256 chips (66.7 μs). It is assumed in calculating both synchronization times that the data processing time is negligibly small (by dint of high-speed processors) when compared with the data collection time. The parameters α and β (or $\tilde{\beta}$) in Fig. 4(b) and (c) are the random variables that denote the time interval between the slot boundary determination and the slot boundary appearance and the time interval between the frame boundary determination and the frame boundary appearance for the CDSA scheme (or the 3GPP 3-step scheme) respectively. Both random parameters are uniformly distributed, with α being in $[0, 10)$ and β (or $\tilde{\beta}$) being in $[0, 150)$. In addition, we denote by S (=15) the number of slots accumulated for the slot boundary acquisition, V_I (=50) the number of accumulated symbols for the igniter sequence identification, $L + V$ (=25) the number of symbols used for a run of the comparison-correction, W (=6) the number of comparison-correction based synchronization processes tried before the initiation of the state symbol correlation process, K (=1) the number of frames lost by the false acquisition declaration, and V_c (=50) the number of accumulated symbols for the cell-specific scrambling sequence identification. We observe that the expectation of the nominal cell search time is 430 symbol time (28.66 ms) for both schemes if the CDSA synchronization is completed after the state symbol correlation process. However, in the CDSA case, it reduces to 205 symbol time (13.66 ms) in high-SNR environments where

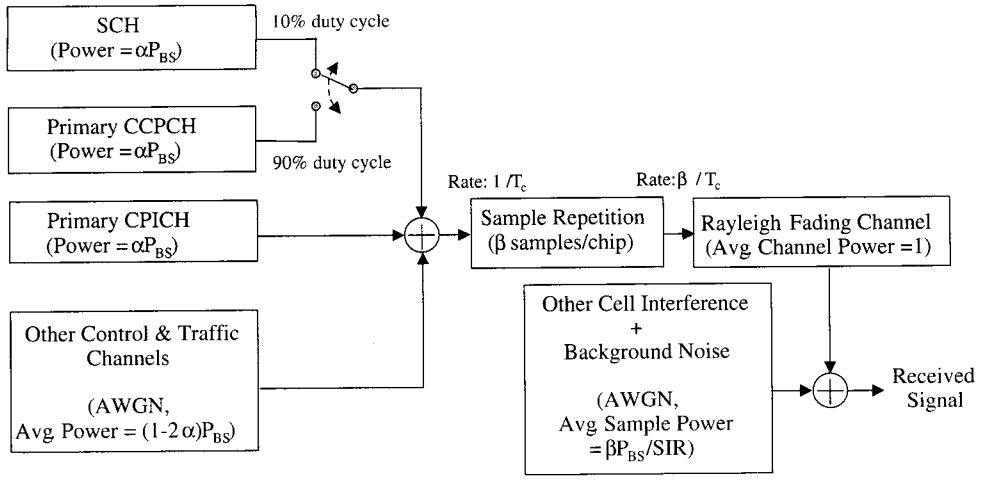

Fig. 5. Power allocation and interference generation employed in performance simulations ($\alpha = 0.1$ or 0.05, $\beta = 2$).

the comparison-correction process satiates the synchronization. Note that in the comparison-correction based synchronization, six possible chances are given to acquire the synchronization in a frame time of 10 ms long,[3] and the state symbol correlation process is initiated only when the six chances are all missed.

III. MEAN ACQUISITION TIME AND COMPLEXITY EVALUATIONS

We examine the performances of the CDSA scheme within the IMT-2000 W-CDMA system, in terms of mean acquisition time and system complexity, and compare them with the 3GPP 3-step synchronization case.

A. Mean Acquisition Time

For the simulations, we take the single-path Rayleigh fading channel, which is the worst-case channel model in regard to code acquisition process [6]. We take the JTC flat and classic (U-shape) spectra of maximum Doppler frequencies 5 Hz and 200 Hz to generate the Rayleigh fading channels for the low-speed and high-speed mobile users respectively. We take the coefficients of the IIR spectral filters of order 32 that are normalized to make the average power of the output samples unity [20]. We set the false alarm penalty factor K to 1 (i.e., 10 ms penalty time) as we can easily confirm the synchronization by observing one frame of the primary CCPCH signal. In calculating the total acquisition time, we do not take into account the MS processing capability dependent factors such as the processing time for determining the maximally correlated code or timing in each step. We set the chip rate to 3.84 Mcps [10] and process two samples per chip for baseband simulations.

Fig. 5 shows how the power allocation and interference generation are arranged for the performance simulations. Note that both the PSC and the SSC are broadcast through the SCH in the 3GPP 3-step approach while only the PSC is broadcast in the CDSA approach. In the 3GPP 3-step case, the SCH (PSC and SSC)/primary CCPCH and the primary CPICH respectively use 10%, of the total BS power, with the remaining 80% being devoted to the other control and traffic channels (i.e., $\alpha = 0.1$).[4] In the CDSA case, we consider two different power allocations—one when the SCH (PSC)/primary CCPCH and the primary CPICH respectively use 10% (i.e., $\alpha = 0.1$) of the BS total power and the other when they use only 5% (i.e., $\alpha = 0.05$): The former is for a fair comparison of cell search performance with the 3GPP 3-step synchronization case and the latter for investigation of possible reduction of the BS power portion for cell search. Other cell interference signals including the background noise are added to the intra-cell signal after the Rayleigh channel multiplication. The intra-cell control/traffic signals which are not related to the acquisition and other cell interferences are approximated to complex white Gaussian random processes in the simulation.

For data processing in the MS, we take the following arrangements: In the 3GPP 3-step case we noncoherently accumulate 15 PSC slots(or, 1 frame) for the first step synchronization, 15 SSC slots for the second step synchronization, and 50 primary CPICH symbols(or, 5 slots) for the third step synchronization.[5] When grouping the 512 cells we consider the case of 32 cell-groups having 16 cells each and the case of 64 cell-groups having 8 cells each [2], [7]. In the CDSA case, we accumulate 15 PSC slots for slot boundary identification (i.e., $S = 15$) and 50 CPICH symbols (or, 5 slots) for igniter sequence identification and verification (i.e., $V_I = 50$) in the first stage; and maximally 150 CPICH symbols (or, 1 frame) for the comparison-correction based main SRG synchronization and state symbol correlation processes in the second stage. In support of the igniter sequence identification process, we carry out a slot boundary verification test with respect to the threshold R_I set such that the false alarm probability in the verification stage becomes 0.01.

The simulation results thus carried out are shown in Fig. 6 through Fig. 8. Fig. 6 plots the mean acquisition times of the

[3] Only five out of six chances are normally available unless the comparison-correction process begins at the frame boundary. Refer to [17] for details.

[4] We assume that the BS power allocated to the SCH is equally divided for PSC and SSC transmissions in the 3GPP scheme.

[5] After the introduction of the CPICH within the IMT-2000 W-CDMA system, the primary CPICH has been considered as a possible means for the third step synchronization. In real implementations, however, we may use either the primary CPICH or the primary CCPCH for the third step.

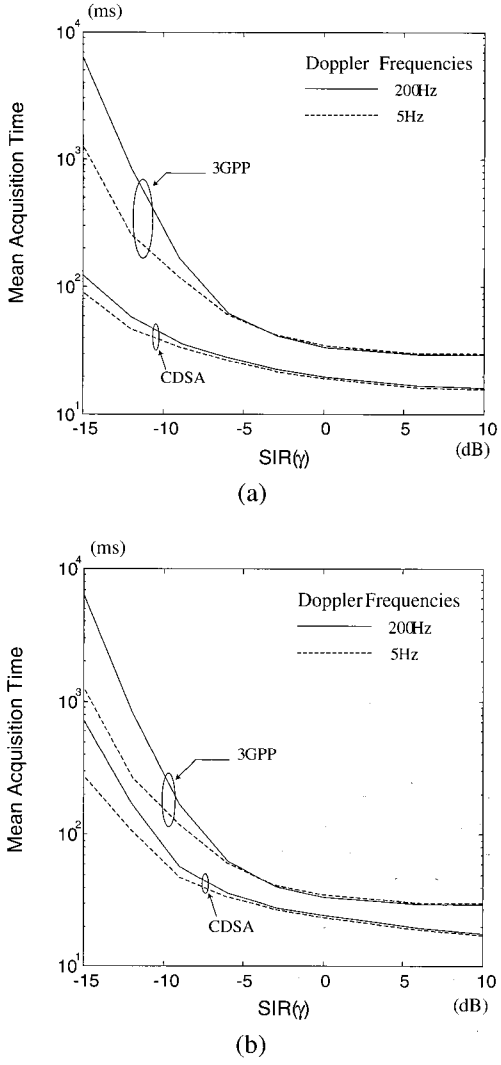

Fig. 6. Overall mean acquisition time performances with respect to SIR(γ) change in Rayleigh fading channel: (a) $\alpha = 0.1$ for both schemes, (b) $\alpha = 0.05$ for CDSA scheme and 0.1 for 3GPP 3-step scheme.

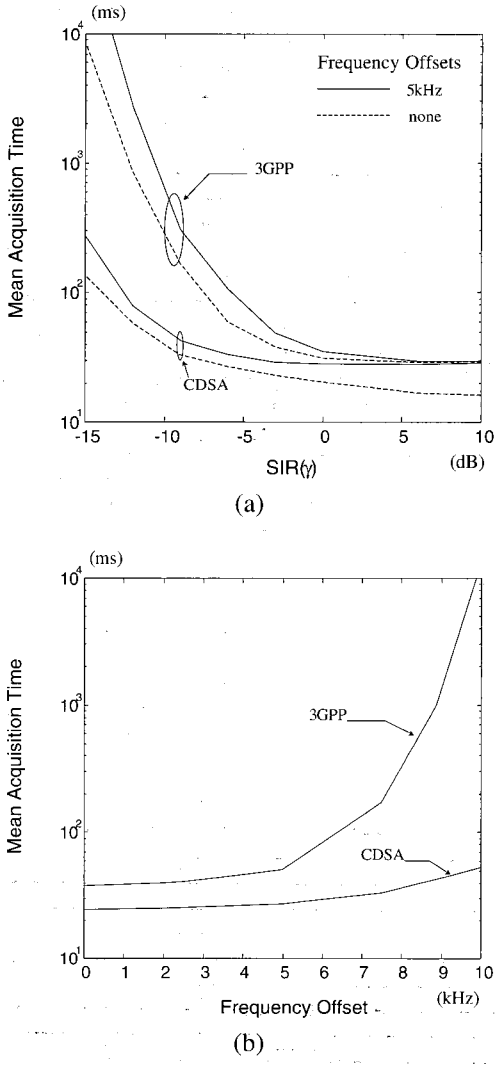

Fig. 7. Mean acquisition time degradation due to frequency offset in Rayleigh fading channel: (a) overall mean acquisition times vs. SIR(γ) for 5 kHz frequency offset and no-offset, (b) overall mean acquisition times vs. frequency offset for -3 dB SIR.

CDSA and the 3GPP 3-step schemes with respect to the signal-to-interference ratio(SIR, defined by the ratio of the average intra-cell total signal energy per chip to the other cell interference spectral density) varying from -15 dB to +10 dB. Fig. 6(a) is the case when 10% of the BS power is allocated to both SCH and primary CPICH channels in both the CDSA and 3GPP 3-step schemes, and Fig. 6(b) is the case when the power allocation drops to 5% in the CDSA scheme and is kept at 10% in the 3GPP 3-step scheme. We observe that in the low-SIR range the CDSA scheme has an SIR gain of about 7 dB over the 3GPP 3-step scheme in the Fig. 6(a) case of equal power allocation. The CDSA scheme yields much shorter acquisition time than the 3GPP 3-step scheme even in the Fig. 6(b) case. In the high-SIR range, the mean acquisition time reduces to less than 20 ms in the CDSA case, while it maintains the nominal acquisition time of 28.6 ms in the 3GPP 3-step case. In terms of Doppler frequency, we observe that the acquisition time performance exhibits similar trends in both schemes with the slowly varying indoor channel (5 Hz, flat spectrum) outperforming the fast varying outdoor channel (200 Hz, classic spectrum) in the low SIR range, but comparable in the high SNR range.

Fig. 7 plots the mean acquisition time degradations caused by frequency offset between the BS and the MS. In normal operation, code acquisition is done before the frequency discrepancy between BS and MS reduces (through phase-locked loop (PLL) operation) to a satisfactory level, so the robustness to frequency offset is critically important in acquisition. Shown in the figure is the case of the outdoor channel of Doppler frequency of 200 Hz, but a similar performance degradation was observed for the indoor channel of 5 Hz Doppler frequency. The case of 10% power allocation is considered for both CDSA and 3GPP 3-step schemes. Fig. 7(a) shows the performance degradation due to the frequency offset of 5 kHz (or, 2.5 ppm for 2 GHz carrier frequency) with reference to the no-offset case. We find that at the SIR of -6 dB, mean acquisition time is about 30 ms for the CDSA scheme (i.e., little degradation) but increases above 100

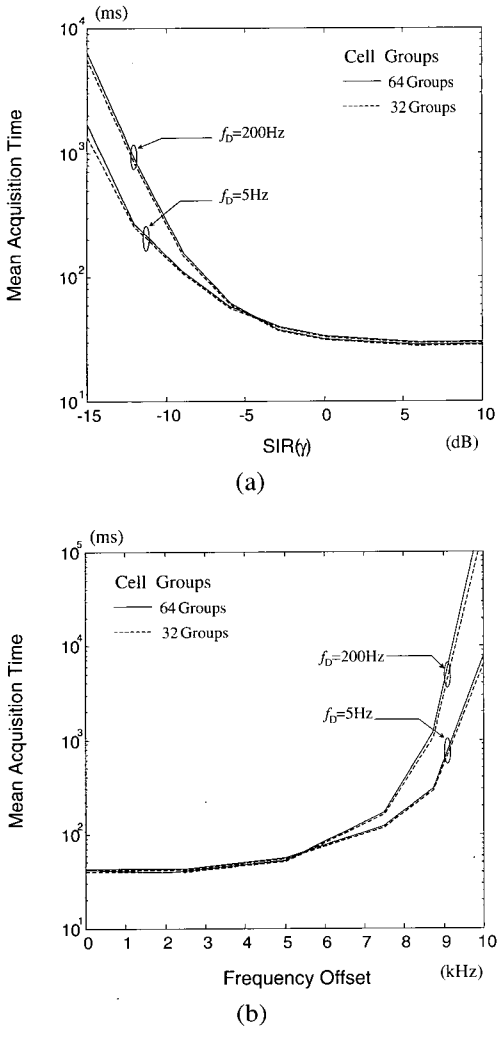

Fig. 8. Overall mean acquisition times for the 3GPP 3-step schemes in Rayleigh fading channel: (a) mean acquisition times vs. SIR(γ) for 0 frequency offset, (b) mean acquisition times vs. frequency offset for -3 dB SIR.

ms for the 3GPP 3-step scheme, which is twice as long as that for the no-offset case. We also observe in the CDSA case that the mean acquisition time is under-bounded by 28.6 ms even in the high SIR range, which implies that acquisition is mostly completed through the state symbol correlation process when the frequency offset is large. Fig. 7(b) shows the performance degradation with respect to the frequency offset that varies from 0 to 10 kHz (5 ppm) for a fixed value of SIR of -3 dB. We observe that acquisition time increases exceedingly rapidly as the frequency offset increases, which warns that the 3GPP 3-step synchronization scheme may malfunction even in the moderate SIR range. In contrast, the CDSA scheme maintains short acquisition time in stable and gradual manner. Notice that the acquisition time performance degradation due to the frequency offset becomes a serious problem in critical regions such as shadowed areas or cell boundaries, where SIR becomes very low and thus acquisition time increases rapidly.

Fig. 8 compares the mean acquisition time performance of the 3GPP scheme for different cell groups. We consider the numbers 32 [2] and 64 [7] for this as they have been proposed as the candidate group numbers of the 3GPP 3-step scheme. Fig. 8(a) shows the mean acquisition time performances with respect to the SIR that varies from -15 dB to +10 dB at no frequency offset, and Fig. 8(b) with respect to the frequency offset that varies from 0 to 10 kHz for the SIR of -3 dB. We observe that both cell groups exhibit almost the same acquisition time performances. This signifies that the performance comparisons given in Figs. 6 and 7 also apply to the 3GPP 3-step scheme having 64 cell groups.

B. System Complexity

As an extension of performance comparison between the CDSA and the 3GPP 3-step schemes, we now consider the system complexity. For this, we consider the hardware complexity and operation complexity, as the former is related to the MS chip-set size and the latter to the MS power consumption. Note that the energy consumption during the cell search process is proportional to the product of the acquisition time and the operation complexity.

For the slot boundary acquisition, both schemes employ the same GHG correlator and the same matched filtering operation. So the hardware and operation complexities required for the slot boundary search are the same in both schemes.

In relation to the CPICH spreading, the CDSA scheme employs 16 parallel *short* Gold sequence correlators to identify the igniter code used for the spreading, while the 3GPP 3-step scheme employs 16 parallel *long* Gold sequence correlators to identify the primary scrambling code used for the spreading. Since both schemes use 16 parallel correlators of complex Gold codes and the number of slots used in the CDSA igniter identification process is the same as that of the 3GPP primary scrambling code identification process (i.e., 5 slots), the hardware and operation complexities for the CDSA igniter identification turn out identical to those for the primary scrambling code identification (i.e., the third step) of the 3GPP 3-step scheme, but the CDSA additionally requires a short Gold sequence generator. On the other hand the 3GPP 3-step scheme necessitates the hardware for 16 Golay-Hadamard correlators for the group and frame boundary identification purpose (i.e., the second step). Therefore the overall hardware complexity of the CDSA scheme becomes slightly less than or equal to that of the 3GPP three-step scheme.

Finally, we compare the operation complexity of the remaining operations—the comparison-correction based synchronization and the state symbol correlation operations of the CDSA scheme in contrast to the group and frame boundary identification operation of the 3GPP 3-step scheme. To collect the state symbol streams for the comparison-correction and the state symbol correlation processes, a single correlation operation is required for the duration of a frame time, and the identified igniter correlator keeps operating to obtain the state symbols. On the contrary, in the 3GPP 3-step case, 16 parallel matched filtering is required for the duration of a frame time to collect the SSC sufficient statistics, with the filtering operation periodically activated (with 10% duty cycle) and performed by a Fast-Hadamard transformer. Once the state symbols are obtained, (15 + 32) off-

line correlations of length 150 and magnitude comparisons are required, *occasionally* (when the state symbol correlation process is triggered), in the CDSA case to determine the cell and frame boundary. In contrast, (15×32) off-line correlations of length 15 and magnitude comparisons are required, *always*, in the 3GPP 3-step case to determine the group and frame boundary using the SSC sufficient statistics. It is not difficult to show that the number of arithmetic operations of those off-line processes is of the same order for both schemes, but the number of relevant memory access is smaller for the CDSA case. Note that the operation complexity as well as system complexity for the comparison-correction based synchronization process of the CDSA scheme is negligible [11]. Overall, we may conclude that the operation complexity for the above remaining processes is comparable for the two schemes or slightly less for the CDSA scheme.

IV. CONCLUDING REMARKS

So far we have introduced the CDSA scheme for fast cell search in the IMT-2000 inter-cell asynchronous DS/CDMA system. By incorporating the state symbol correlation process in the comparison-correction based synchronization process of the existing DSA, we could significantly improve the worst-case acquisition time performance of the DSA scheme. The resulting CDSA scheme maintains short acquisition time even in extremely low SIR regions as well as in high frequency offset environment. We have confirmed through computer simulations that the CDSA scheme, when realized along with the DQPSK modulation scheme in the IMT-2000 W-CDMA system, substantially outperforms the 3GPP 3-step synchronization scheme, and the system complexity is comparable or slightly less. The CDSA scheme is much superior to the 3GPP 3-step scheme in view of average energy consumption in cell search as well, which is directly related to the battery life of the MS.

The two-stage CDSA scheme distinguishes itself from the 3GPP 3-step scheme in the cell search methodology. The 3GPP 3-step scheme applies a hierarchical uncertainty reduction method through the three steps—symbol and slot boundary identification, frame boundary and cell group identification, and cell identification. In order to realize such hierarchical reduction, it necessitates synch-dedicated signals such as PSC and SSC. On the contrary, the CDSA scheme takes advantage of the fundamental relations between the cell-specific scrambling codes and the sequence generator states. It acquires synchronization in two stages, first by acquiring the slot boundary and short auxiliary sequence, and secondly by synchronizing the long main sequence. This synchronization process is done efficiently by conveying the cell-specific state symbols of the main sequence generator through the pilot channel. The correlation process among the conveyed state symbols contributes to enhancing the robustness of synchronization in poor channel environment.

In the second stage of the CDSA-based IMT-2000 W-CDMA system, the MS gets an opportunity to complete the cell search by employing the comparison-correction based synchronization process at every detection of 25 successive state symbols. If this process fails six consecutive times, until 150 detected state symbols are utilized, the MS activates the state symbol correlation process. In this process, the MS correlates the received soft state symbol sequence of length 150, first with the 15 candidate shifts of the second state sample sequence (to identify the frame boundary), and then with the 32 first state sample sequences (to identify the cell number). In practical implementations, we may use some optimized values for the number of igniter sequences and the length of the state symbol sequence for the correlation process such that the performances in acquisition time as well as in system complexity get maximized.

According to the performance evaluation conducted through computer simulations under single-path Rayleigh fading channels, the CDSA scheme turned out to outperform the 3GPP 3-step synchronization scheme, requiring significantly less signal power (as much as 7 dB) to achieve the same acquisition time performance in low SIR environment. Furthermore, acquisition time of the 3GPP 3-step scheme turned out to increase very rapidly as the frequency offset increases, which warns that the 3GPP 3-step synchronization scheme may malfunction even in the moderate SIR range. In contrast, the CDSA scheme maintained short acquisition time with the change being made gradually even in the frequency offset environment.

Another noteworthy point observed through simulation is that the CDSA scheme outperforms the 3GPP 3-step scheme even when the power allocated to the synchronization related channels (i.e., the SCH, the CPICH, and the CCPCH) is cut to half. In practice, the power budget for these channels should be carefully determined considering various other factors such as channel estimation performance and broadcast channel data error rate also. Nevertheless, it is a promising indication that the power consumption in the common channels can be reduced to half, as it directly contributes to channel capacity increase.

While we have discussed the CDSA scheme in the capacity of the inter-cell asynchronous IMT-2000 system in this paper, it can also be successfully applied to the inter-cell synchronous DS/CDMA systems, thereby expediting the acquisition process and enhancing the robustness in poor channel environments. Efficient realization of the CDSA-based inter-cell synchronous DS/CDMA systems is an issue for further study.

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