4-레벨 인버터 및 컨버터를 위한 새로운 스너버회로

論 文
49B-9-6

A New Snubber Circuit for Four-Level Inverter and Converter

金 仁 東* · 魯 義 哲*
(In-Dong Kim · Eui-Cheol Nho)

Abstract - This paper proposes a new snubber circuit for 4-level inverter and converter. The snubber circuit makes use of Undeland snubber and McMurray efficient snubber as basic snubber unit, and can be regarded as a generalized combined Undeland and McMurray efficient snubber. The proposed snubber keeps such good features as fewer number of components, improved efficiency due to low snubber loss, capability of clamping overvoltage across main switching devices, and no unbalance problem of blocking voltage. Furthermore, the proposed concept of constructing a snubber circuit for 4-level inverter and converter can apply to any level of converter and inverter.

Key Words : 4-level inverter, Multilevel inverter, Multilevel converter, Snubber

1. Introduction

Recently the multilevel inverter and converter have drawn tremendous interest for high voltage and high power applications [1-7]. The general structure of the multilevel inverter and converter is to synthesize sinusoidal voltage waveforms from several levels of voltages typically obtained from capacitor voltage sources. As the number of levels increase, the synthesized output waveform adds more steps, producing staircase waveform which approaches the sinusoidal wave with minimum harmonic distortion. More levels also mean that higher DC link voltage than voltage rating of device itself can be handled by series device without device voltage sharing problem and without the use of bulky and heavy transformer for multiple connections. Until now, for multilevel inverter and converter, conventional RCD and RLD snubber as turn-off snubber and turn-on snubber, respectively, have been used widely and exclusively because it is easy to apply to multilevel inverter and converter as shown in Fig. 1 [6-7]. But this kind of

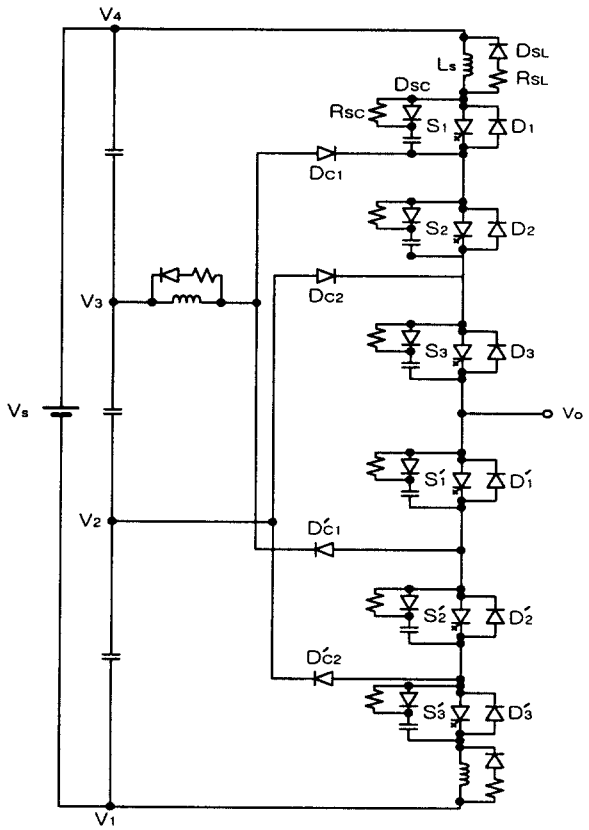


Fig. 1 4-level GTO inverter with conventional RCD and RLD snubber.

* 正 會 員 : 釜慶大 電氣 · 制御計測工學部 助教授 · 工博
接受日字 : 2000年 4月 21日
最終完了 : 2000年 8月 18日

snubbers need separate snubber circuit unit for each GTO which is composed of turn-off capacitor, turn-on inductor, resistors, and diodes. Thus the total number of snubber components become considerably high and the circuit becomes complex, thus resulting in high costly multilevel inverter and converter. And since the large amount of snubber energy is fully dissipated in snubber resistor, system power loss become high, which causes low system efficiency. Furthermore, during turn-off process, the overvoltage of GTO can be very high, usually about 1.8 times higher than DC link voltage because the turn-off capacitor is not large enough to absorb the stored inductor energy. In addition, unbalance problem of the overvoltage, which results from combination of multilevel structure and RCD/RLD snubbers, makes voltage stresses of the switching devices worse [7].

To overcome the above-mentioned disadvantages of RCD/RLD snubber for multilevel inverter and converter, a new snubber topology suitable for multilevel inverter and converter, especially for 4-level inverter and converter, are proposed. The proposed snubber utilizes Undeland snubber and McMurray efficient snubber as basic snubber unit and can be regarded as a generalized combined Undeland and McMurray snubber for 4-level structure converter. Its good features include fewer number of component, improved efficiency due to low snubber loss, capability of clamping overvoltage across main switching device, and no unbalance problem of blocking voltage. This paper also explains in detail how to construct a snubber circuit for 4-level inverter and converter.

2. Review of Undeland Snubber and McMurray Snubber as Basic Snubber Unit

Fig. 2(a) shows one inverter pole with the conventional Undeland snubber. In this paper, the Undeland snubber is to be utilized as one of the basic snubber unit for 4-level inverter and converter [8]. The modified Undeland snubber, that is, the complementary snubber of the original Undeland snubber can be derived as shown in Fig 2(b) and its principle of operation is the same as that of the original Undeland snubber. The complementary snubber will also be used as a basic snubber unit for negative arms of multilevel inverter and converter poles. As shown in Fig. 2(a) and (b), the snubber circuit consists of fewer components, which includes turn-off capacitor C_S for dv/dt limitation, turn-on inductor L_S for di/dt limitation, capacitor C_O for overvoltage clamping and snubber energy recovery normally about ten times larger than C_S, resistor R_S for resetting snubber inductor and capacitor, and diodes

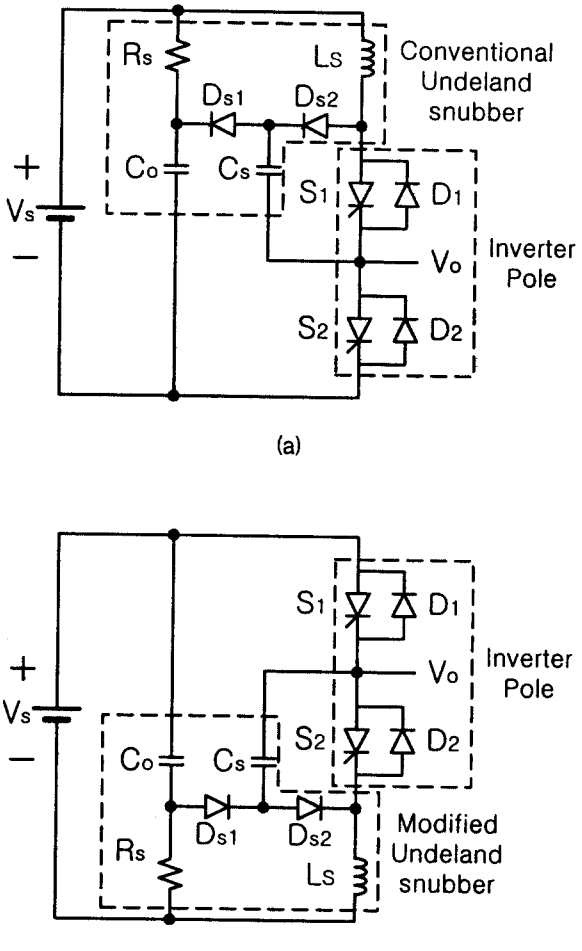


Fig. 2 (a) Conventional Undeland snubber circuit, (b) Modified Undeland snubber, (c)McMurray efficient snubber.

D_{S1}, D_{S2}. Such a simple circuit topology of Undeland snubber make itself good candidate for multilevel inverter

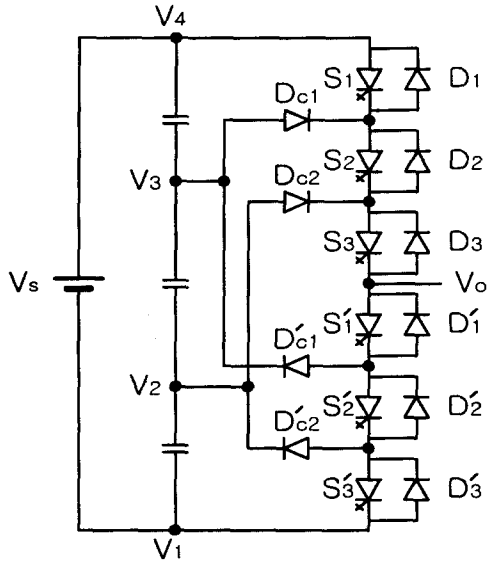


Fig. 3 4-level inverter with no snubber.

and converter which essentially include a number of main switching devices. In addition, since the resistor R_S is not directly involved in snubbing action unlike RCD and RLD snubber, mechanical arrangement of components and cooling system are much easier and simpler. In particular, thanks to capability of clamping overvoltage at turn-off and no unbalance problem of overvoltage, the Undeland snubber is selected as the best basic snubber unit for multilevel inverter and converter.

The McMurray snubber arrangement resulted from the modification of the RCD snubber circuit, as shown in Fig. 2(c) [9]. The two series snubbers, each having a self-inductance L_{self} are magnetically coupled with mutual coefficient k to provide a total series inductance $L_s=2L_{self}(1+k)$, which is effective in limiting the di/dt through either S_1 or S_2 to E_d/L_s. In particular, this di/dt limit applies to the discharge of the shunt snubber capacitors C_s because of the steering action by the snubber diodes D_{S1} and D_{S2}. Therefore, the value of resistance R_S can be low, as determined by the need to limit the overvoltage during discharge of the series snubber, but to dissipate the energy in a reasonable time, preferably before the next switching occurs. Because the resistance R_S is low, the two shunt snubber capacitors C_S are able to render each other mutual assistance in limiting the dv/dt when turning off either S_1 or S_2, thus allowing a reduction in their capacitance values by a factor up to two. The associated losses can be reduced by the same factor.

Table 1 4-level inverter voltage levels and corresponding switch states(1 : On , 0 : Off)

Output Vo	Switch State					
	S_1	S_2	S_3	S'_1	S'_2	S'_3
$V_4(=V_S)$	1	1	1	0	0	0
$V_3(=2V_S/3)$	0	1	1	1	0	0
$V_2(=V_S/3)$	0	0	1	1	1	0
$V_1(=0)$	0	0	0	1	1	1

3. Proposed Snubber for 4-level Inverter and Converter

An n-level multilevel inverter typically consists of n-1 capacitors on the DC bus and produces n-levels of the phase voltage. Fig. 3 shows one pole of four-level inverter in which the DC bus consists of three capacitors, C_1, C_2, and C_3. For a DC bus voltage V_S, the voltage across each capacitor is $V_S/3$ and each device voltage stress will be limited to one capacitor voltage level, $V_S/3$, through clamping diodes. Table 1 lists the voltage levels and their corresponding states. State condition 1 means the switch is on, and 0 is off. There exists three complementary switch pairs in each phase. The complementary switch pair is defined such that turning on one of the pair switches excludes the other from being turned on. In case of four-level inverter, the three complementary pairs are (S_1, S'_1), (S_2, S'_2), and (S_3, S'_3) which, respectively, correspond to each level change, that is, between V_4 and V_3, V_3 and V_2, and V_2 and V_1. Notice that the level changes occur only between adjacent levels. When investigating all level changes, we can find the operating part of circuit during each level change to converge to equivalent two level inverter, which is composed of complementary pair switches and corresponding clamping diodes.

Consider level changes between V_3 and V_2, as an example, shown in Fig. 4. The corresponding complementary pair is (S_2, S'_2). If S_2 is on and S'_2 is off, output level is V_3. Conversely, If S_2 is off and S'_2 is on, output level is V_2. During these level changes the operating components of four-level inverter can be drawn with thick line as shown in Fig. 4(a). The thick-lined part of the circuit can be transformed into Fig. 4(b) and can also be redrawn as Fig. 4(c) since switches S_3 and S'_1 are always turned on irrespective of on/off condition of S_2 and S'_2. Fig. 4(c) shows that the operating part

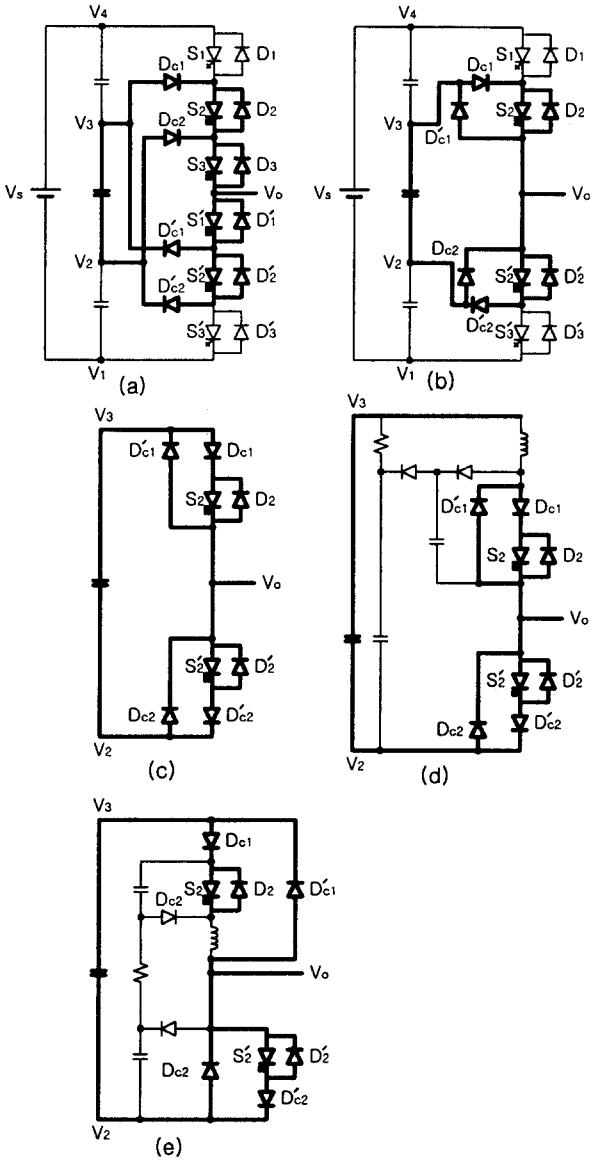


Fig. 4 Derivation of the proposed snubber for 4-level inverter (a)the operating part of circuit (thick line) during level changes between V3 and V2 , (b) Redrawn circuit of (a), (c)Equivalent two-level inverter, (d)Equivalent circuit with Undeland basic snubber unit, (e)with McMurray basic snubber unit.

of circuit is equivalent to the conventional two-level voltage source inverter. It follows that for the equivalent two-level inverter related to switching devices (S_2, S'_2), the basic snubber unit which have been used in two-level inverter can be applied as shown in Fig. 4(d) and 4(e) in case of Undeland snubber and McMurray snubber as a basic snubber, respectively.

In the same way, all the equivalent two-level inverter corresponding to each level change, that is, each complementary pair in multilevel inverter can be derived,

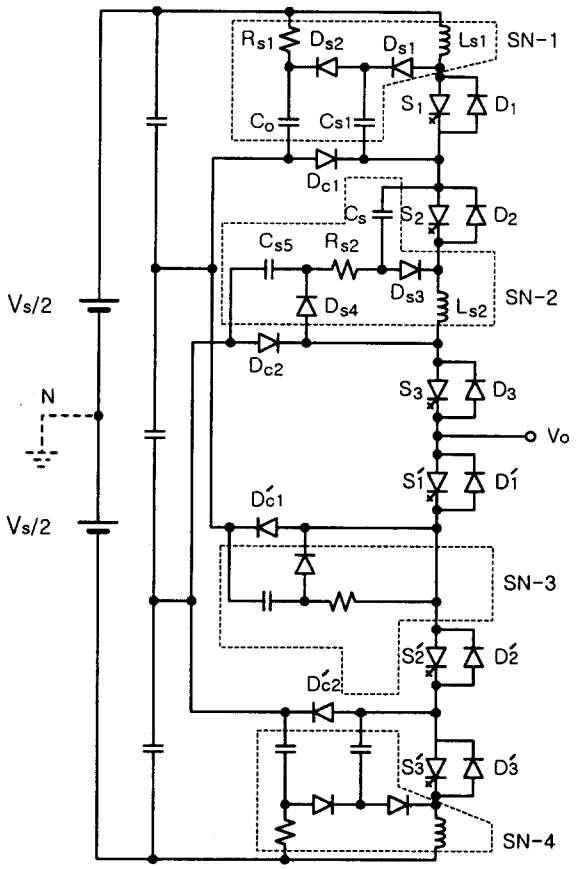


Fig. 5 4-level inverter with the proposed snubber(within the dotted line).

and the same basic snubber units can apply to them. So, we can obtain the proposed snubber circuit for four-level inverter as shown in Fig. 5. Using the proposed principle, a generalized snubber circuit for any multilevel inverter and converter can be achieved. The generalized snubber has the same good features as the basic snubber unit. In this paper since we use the Undeland snubber and McMurray efficient snubber as the basic snubber unit, the characteristics of the generalized snubber are such as fewer number of component, improved efficiency due to low snubber loss , capability of clamping overvoltage across main switching device and easy arrangement and mounting of snubber circuit. Furthermore, thanks to the snubber structure, the generalized snubber has no unbalance problem of overvoltage unlike RCD/RLD snubber, thus resulting in equal voltage stress to all main switching devices except clamping diodes.

4. Simulation Results

In order to prove the effectiveness of the proposed snubber circuit, A simulation for 4-level inverter equipped

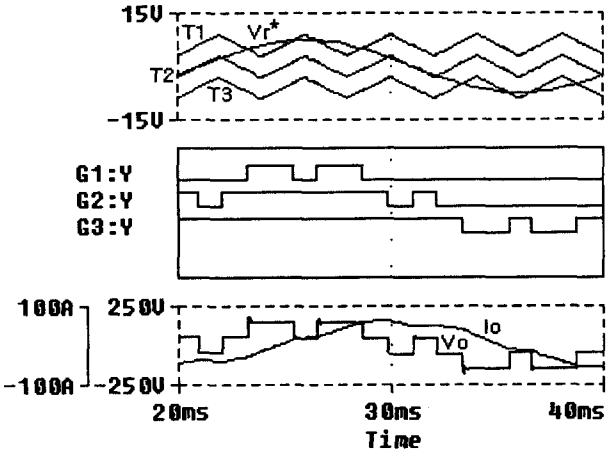


Fig. 6 simulated PWM generation-related signals(first plot and second plot) and overall output voltage Vo and current Io waveforms during one fundamental period(third plot).

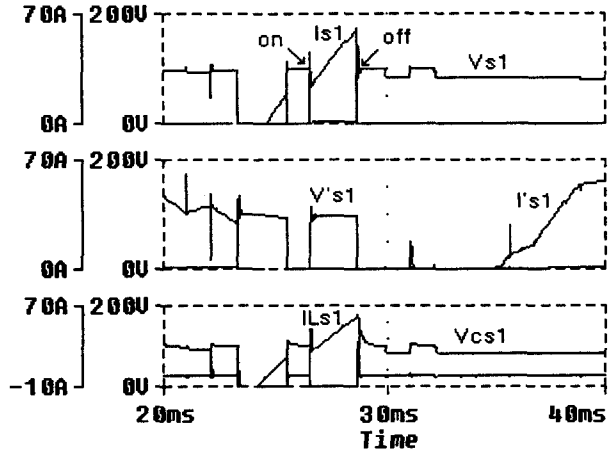
with the proposed snubber circuit is carried out. Only one pole of the 4-level inverter was simulated as shown in Fig. 5 with the output terminal V_O connected to the midpoint of input source voltage V_S through series-connected R-L load. The used simulation tool is PSPICE 8.0 version. The simulation conditions are as follows:

V_S = 300 [V] $I_{O.max}$ = 50 [A]
$L_{S1} = L_{S2}$ = 25 [μH] $C_{S1} = C_{S1}$ = 1 [μF]
C_O = 40 [μF] R_{S1} = 4.7 [Ω]
R_{S2} = 0.5 [Ω]

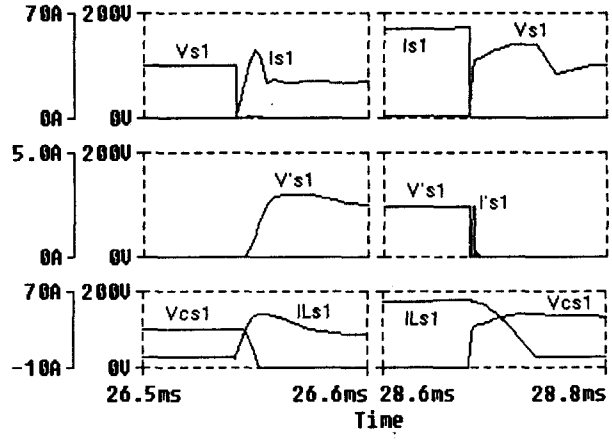
Since the proposed snubber utilizes Undeland snubber and McMurray snubber as basic snubber, the snubber circuit parameters are determined according to their conventional design method.

Fig. 6, 7, 8, and 9 show the simulation results under the same time base so that the overall operation of the proposed snubber can be understood easily. Fig. 6 shows PWM-related reference signal Vr* , triangular waveforms T_1 - T_3, and overall output voltage and current waveforms. The PWM gate signals G_1, G_2, and G_3 which are generated by comparing reference signal and triangular signals apply for switches S_1, S_2, and S_3 respectively, and their complemented signals also apply for switches S'_1, S'_2, and S'_3, respectively. The output voltage and current waveforms shown in the third plot have good waveforms with no adverse effects of the proposed snubber.

Fig. 7(a) shows the simulated voltage v_{S_1} and



(a)

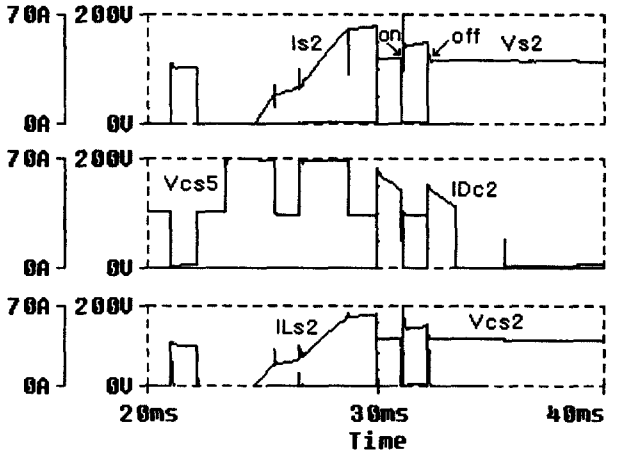


(b)

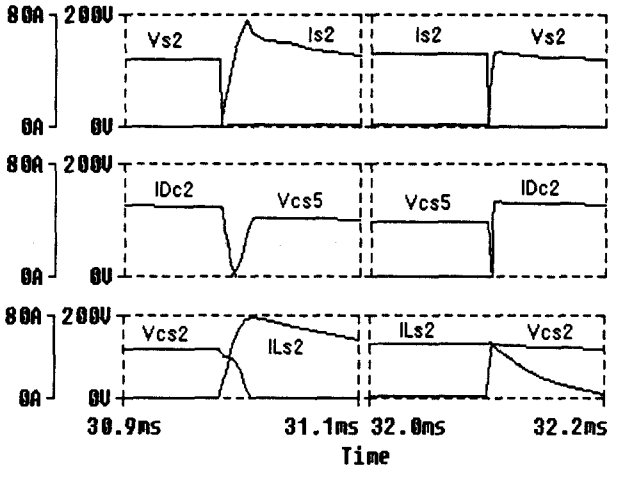
Fig. 7 (a) simulated voltage v_{S_1} and current i_{S_1} of switch S_1(first plot), v'_{S_1} and $i'_{S_1}$of switch S'_1 (second plot) and snubber inductor current i_{Ls1} and capacitor voltage v_{Cs1} of L_{S1} and C_{S1} (third plot) in snubber circuit SN-1, (b) their zoomed waveforms during turn-on(left) and turn-off(right) intervals.

current i_{S_1} of switches S_1(first plot), v'_{S_1} and $i'_{S_1}$of switches S'_1(second plot) and snubber inductor current i_{Ls1} and capacitor voltage v_{Cs1} of L_{S1} and C_{S1} (third plot) in snubber circuit SN-1. Fig. 7(b) also their detailed(zoomed) waveforms during turn-on(left) and turn-off(right) intervals, respectively. It proves that the proposed snubber circuit have good snubbing effects on main switches in terms of transient switching peak values, dissipative power and snubber losses.

Fig. 8 (a) shows the simulated voltage v_{S_2}, and current i_{S_2} of switches S_2 (first plot), snubber capacitor



(a)



(b)

Fig. 8 (a) simulated voltage v_{S_2}, and current i_{S_2} of switch S_2 (first plot), snubber capacitor voltage v_{Cs}, clamp diode current i_{Dc2}(second plot), and snubber inductor current i_{Ls2} and capacitor voltage v_{Cs2} of L_{s2} and C_{s2} in snubber circuit SN-2(third plot), (b) their zoomed waveforms during turn-on(left) and turn-off(right) intervals.

voltage v_{Cs}, clamp diode current i_{Dc2}(second plot), and snubber inductor current i_{Ls2} and capacitor voltage v_{Cs2} of L_{s2} and C_{s2} in snubber circuit SN-2(third plot). Fig. 8(b) shows their zoomed waveforms during turn-on (left) and turn-off (right) intervals, respectively. It proves that the proposed snubber provides switch S_2 and clamp diode D_{C2} good snubbing effects in terms of transient switching peak values and diode reverse recovery phenomena.

In order to compare characteristics of the proposed snubber with those of conventional RCD/RLD snubber,

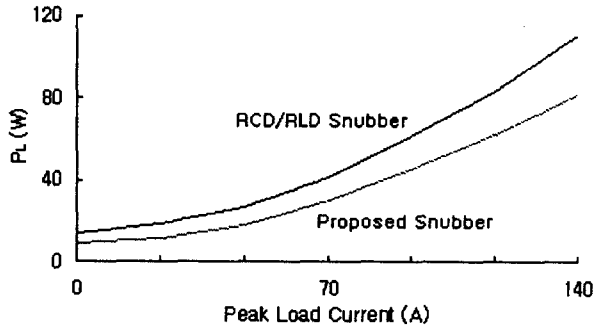


Fig. 9 Snubber losses of proposed snubber compared with that of conventional RCD/RLD snubber.

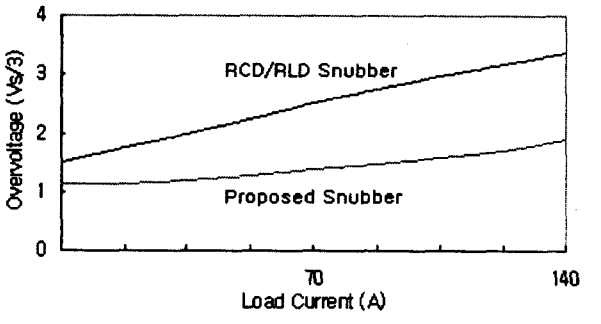
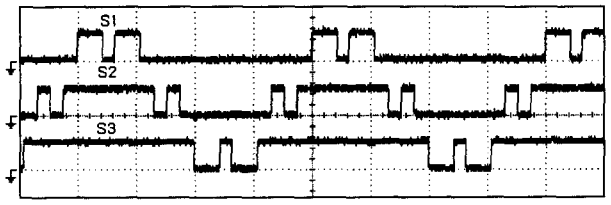


Fig. 10 Overvoltage across main switches during switching operations of proposed snubber.

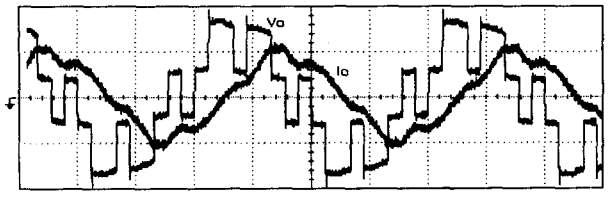
Table 2 Comparison of the number of snubber circuit components

Components	Resistor	Capacitor	Diode	Inductor	Total number
RCD/RLD snubber	9	6	9	3	27
Proposed snubber	4	7	7	3	21

both snubbers are simulated under comparison conditions of the same turn-on inductor value and turn-off capacitor value, which provide identical di/dt and dv/dt values to both snubbers. Fig. 9 shows the snubber loss of proposed snubber compared with that of conventional RCD/RLD snubber. It proves that the proposed snubber make system efficiency improved by about 30% at 70A load current level. If the DC link voltage is increased as in practical case, the system efficiency will be improved because of increase of the stored snubber energy at snubber capacitor C_S. Fig. 10 shows the overvoltage of main switches in both proposed and conventional snubber. As shown in Fig. 10, the overvoltage of main switches in proposed snubber is reduced as good as 1/2 or 1/3 of

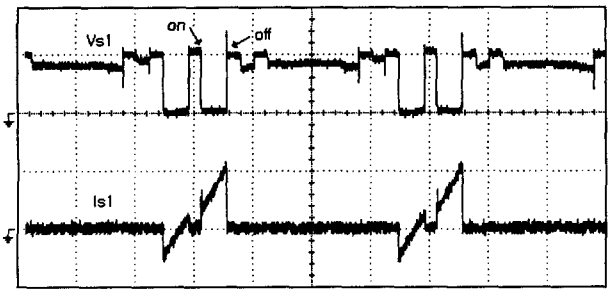


(a)

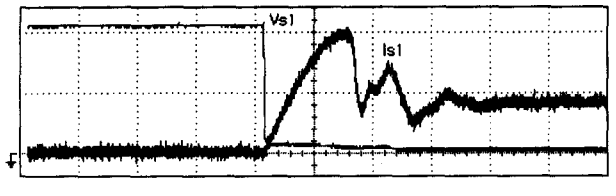


(b)

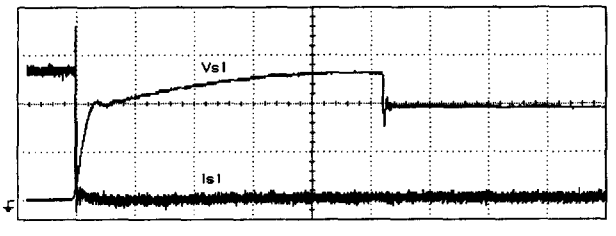
Fig. 11 (a) measured PWM gate signals of switches S_1, S_2 and S_3 and (b) overall output voltage v_o and current i_o waveforms [100V/div, 50A/div, 5msec/div].



(a)

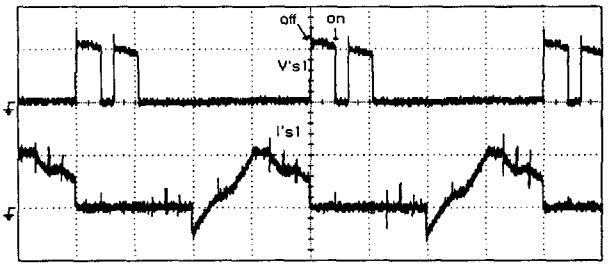


(b)

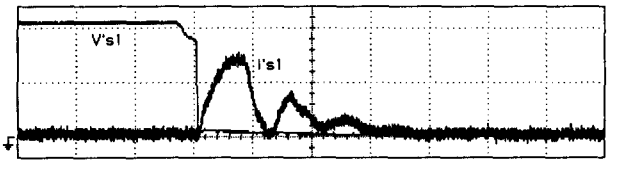


(c)

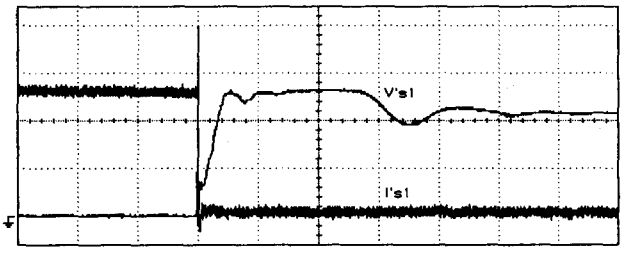
Fig. 12 (a) measured voltage v_{S_1} and current i_{S_1} of switch S_1[100V/div, 50A/div, 5msec/div] (b) their zoomed waveforms during turn-on interval and (c) during turn-off interval [50V/div, 20A/div, 10μ sec/div].



(a)



(b)



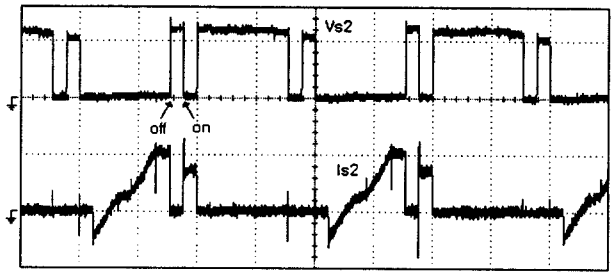
(c)

Fig. 13 (a) measured voltage v'_{S_1} and i'_{S_1} current of switch S'_1 [100V/div, 50A/div, 5msec/div] (b) their zoomed waveforms during turn-on interval [50V/div, 10A/div, 10sec/div] and (c) during turn-off interval [50V/div, 10A/div, 20sec/div].

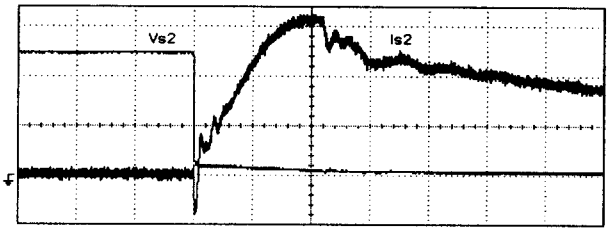
the overvoltage of main switches in conventional RCD/RLD snubber. This characteristics make it possible for the circuit designer to select lower rating of devices. Table 2 shows that the proposed snubber requires lower number of snubber circuit elements than that of conventional snubber.

5. Experimental Results

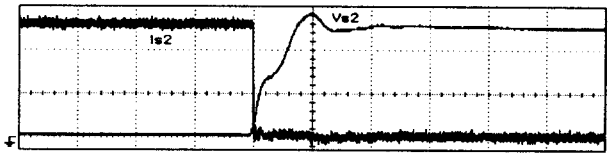
In order to verify the operation of the proposed snubber circuit, one pole of 4-level inverter was properly implemented with rated power 7.5[kw] and output current 50[A]. The prototype inverter is controlled through triangular waveform carrier-based PWM operation with carrier frequency 250[Hz]. The inverter with the proposed snubber circuit utilizes IXYS IGBT MII(MID, MDI)100-12A3 of current rating 135[A] for main switches S_1-S'_3 and clamp diodes D_{C1}-D'_{C2}, IXYS DSEI 2×61 for snubber diodes, ferrite core inductor of



(a)

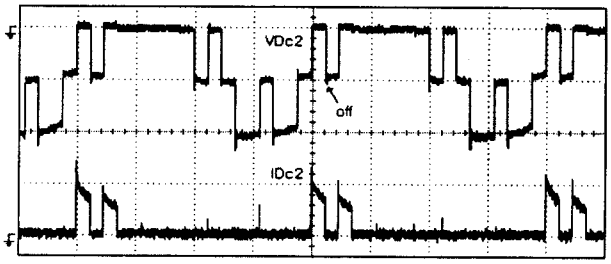


(b)

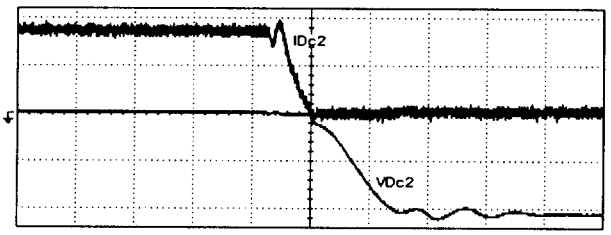


(c)

Fig. 14 (a) measured voltage v_{S_2}, and current i_{S_2} of switch S_2[100V/div, 50A/div, 5msec/div], (b) their zoomed waveforms during turn-on interval and (c) during turn-off interval[50V/div, 20A/div, 10 μ sec/div].

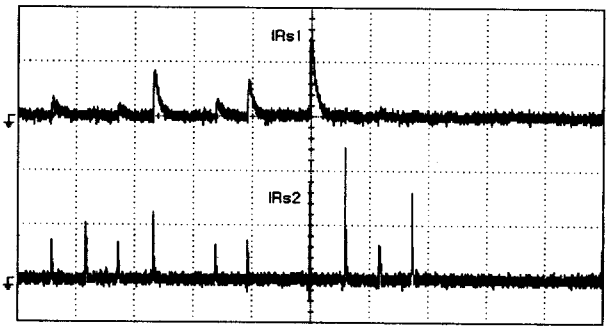


(a)

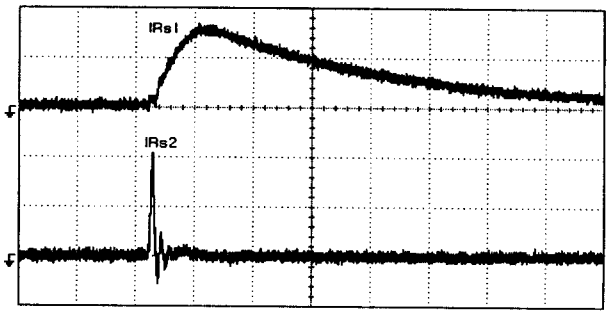


(b)

Fig. 15 (a) measured voltage $v_{D_{c2}}$, and current $i_{D_{c2}}$ of diode D_{c2}[100V/div, 50A/div, 5msec/div], (b) their zoomed waveforms during turn-off interval [50V/div, 50A/div, 10 μsec/div].



(a)



(b)

Fig. 16 (a) measured current waveforms i_{Rs1} [5A/div] and i_{Rs2} [20A/div] through snubber resistors R_{s1} and R_{s2}, (b) zoomed waveforms i_{Rs1} and i_{Rs2}.

25[μH] for snubber inductor L_S, and polypropylene capacitor of 1[μF], 400[v] for snubber capacitor C_S, polypropylene capacitor of 40[μF], 400[v] for snubber capacitor C_O, snubber resistors R_{S1} 4.7[Ω] and R_{S2} 0.5 [Ω]. The switching devices IGBT as main switches are used to check only the operation of the proposed snubber circuit.

Fig. 11 shows the measured PWM gate signals of switches S_1, S_2 and S_3 , and overall output voltage v_o with respect to neutral point N and current i_o waveforms. Fig. 12 shows the measured voltage v_{S_1} and current i_{S_1} of switches S_1, their zoomed waveforms during turn-on interval and turn-off interval. Fig. 13 shows the measured voltage v'_{S_1} and i'_{S_1} current of switches S'_1 and their zoomed waveforms during turn-on and turn-off intervals. It shows that the proposed snubber results in the good waveforms around the main switches S_1 and S'_1 in terms of limiting the di/dt and dv/dt values and reducing switching losses. Since the snubber for the main switches S_1 and S'_1 is similar to Undeland snubber, the measured results are as good as those of Undeland snubber.

Fig. 14 shows the measured voltage v_{S_2} and

current i_{S_2} of switches S_2, and their zoomed waveforms during turn-on and turn-off intervals. Fig. 15 shows the measured voltage $v_{D_{C2}}$, and current $i_{D_{C2}}$ of diode D_{C2}, and their zoomed waveforms during turn-off interval. It proves that the proposed snubber provides S_2 and D_{C2} the good di/dt and dv/dt protections, reducing switching losses. Since the snubber for the main switches S_1 and S'_1 is similar to McMurray snubber, the measured results are as good as those of McMurray snubber.

Fig. 16 shows the measured current waveforms i_{Rs1} and i_{R2} through snubber resistor R_{S1} and R_{S2}, and zoomed waveforms i_{Rs1} and i_{R2}. As shown in Fig. 16, the proposed snubber results in lower snubber losses.

6. Conclusions

This paper proposes a new efficient snubber circuit for 4-level inverter and converter. The snubber circuit makes use of Undeland snubber and McMurray snubber as basic snubber unit and can be regarded as a generalized combined Undeland snubber and McMurray snubber. The proposed snubber keeps such good features as fewer number of components, improved efficiency due to low snubber loss, capability of clamping overvoltage across main switching device and no unbalance problem of blocking voltage. Furthermore, the proposed concept of constructing a snubber circuit for 4-level inverter and converter can apply to any level of multilevel converters easily.

References

[1] Nam S. Choi, Jung G. Cho and Gyu H. Cho, "A General Circuit Topology of Multilevel Inverter," IEEE PESC, pp96-103, 1991.

[2] C. Hochgraf, R. Lasseter, D. Divan and T. A. Lipo, "Comparison of Multilevel Inverter for Static Var Compensation," IEEE IAS Annual Meeting Conf. Record, pp. 921-928, 1994.

[3] J.-S. Lai and F. Z. Peng, "Multilevel Converters-A New Breed Power Converters," IEEE IAS Annual Meeting Conf. Record, pp. 2348-2356, 1995.

[4] Nam S. Choi, Cuk C. Cho and Gyu H. Cho, "Modeling and Analysis of a Static Var Compensator using Multilevel Voltage Source Inverter," IEEE IAS Annual Meeting Conf. Record, pp. 356-365, 1993.

[5] F. Z. Peng, J.-S. Lai, J. Mckeever and J. VanCoevering, "A Multilevel Voltage-Source Inverter with Separate DC source for Static Var Generation," IEEE IAS Annual Meeting Conf. Record, pp. 2541-2548, 1995.

[6] G. Sinha, C. Hochgraf, R.H. Lasseter, D.M. Divan T.A. Lipo, "Fault Protection in a Multilevel Inverter Implementation of a Static Condenser," IEEE IAS Annual Meeting Conf. Record, pp. 2557-2564, 1995.

[7] B. S. Suh, D. S. Hyun and H. K. Choi, "A Circuit Design for Clamping an Overvoltage in Three-level GTO Inverters," IEEE IECON, pp651-656, 1994.

[8] T. Undeland, F. Jenset, A. Steinbakk, T. Rogne and H. Hernes, "A Snubber Configuration for Both Power Transistor and GTO PWM Inverters," IEEE PESC, pp42-53, 1984.

[9] W. McMurray, "Efficient Snubbers for Voltage-Source GTO Inverters," IEEE Trans. Pow. Elec., vol. PE-2, No. 3, pp. 264-272, July 1987.

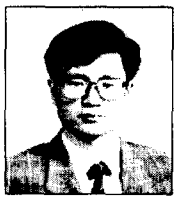
저 자 소 개

김 인 동 (金 仁 東)

1960년 8월 27일생. 1984년 서울대 공대 전기공학과 졸업. 1987년 한국과학기술원 전기 및 전자공학과 졸업(석사). 1991년 동 대학원 졸업(공박). 1991년~1996년 대우중공업 철도차량연구소 책임연구원. 1997년~1998년 미국 Univ. of Tennessee 방문교수. 1996년~현재 부경대학교 공대 전기제어계측공학부 조교수

Tel : 051-620-1429

E-mail : idkim@dolphin.pknu.ac.kr



노 의 철 (魯 義 哲)

1960년 8월 2일생. 1984년 서울대 공대 전기공학과 졸업. 1986년 한국과학기술원 전기 및 전자공학과 졸업(석사). 1991년 동 대학원 졸업(공박). 1997년~1998년 미국 Univ. of Wisconsin-Madison 방문교수. 1995년~현재 부경대학교 공대 전기제어계측공학부 조교수

Tel : 051-620-1439

E-mail : nhoec@dolphin.pknu.ac.kr