대용량 인버터 시스템을 위한 공간벡터 PWM 인버터의 병렬운전

Parallel Operation of Space Vector PWM Inverters for Large Capacity Inverter System

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Abstract – This paper deals with the parallel operation of space vector PWM for large capacity inverter system. To enlarge the capacity of inverter system and to reduce the current ripples on inverter output side, two or more inverters are operated in parallel. In this paper, a new parallel operation strategy which minimizes the harmonic distortion of the output stage is described. The proposed method is developed on the basis of the space-vector PWM in order to increase the linearly controllable voltage range. With the help of the proposed voltage synthesis method, the total harmonic distortion of the output stage can be greatly reduced in compared with that of conventional method with sinusoidal PWM or that of the single inverter operation case. The experimental results with reduced scale test show the feasibility of the proposed voltage synthesis method.

Key Words : parallel operation, space vector PWM inverters, Large capacity inverter system

1. Introduction

Up to date, the high power inverter system draws the increasing popularity because of the increasing demands for the high power capacity in many application fields such as power plant, traction drives and rolling mill drives etc. However, as widely known, the voltage and current ratings of the power devices limits the capacity of the inverter. To increase the capacity of inverter system, a switching bank which consists of several power semi-conductor switching devices connected in series or parallel is used as a single switch of the inverter. However, because of the different characteristics of the each power switching devices, a particular switching device may get higher switching stress, which results in additional cost and reduced reliability. On the other hand, there have been many researches about series or parallel operation scheme with multiple inverter unit in order to increase the whole capacity of inverter systems[1],[2]. Using the parallel operation scheme, the parallel operation of inverters can be cost effective owing to the mass production through standardization. In addition, when several unit inverters are operated in parallel, the harmonic contents of the output stage can be reduced in compared with the case of single inverter

scheme [1],[2]. In the high power application fields, only the switching devices such as GTO or thyristor with low frequency switching characteristics are available, therefore the harmonic problem of the output stage becomes very serious. In the conventional inverter scheme with parallel operation, this problem could be overcome to some degree by shifting the carrier-waves which are injected to each unit inverter to generate the actual gating pattern[1].

In recent years, a new switching pattern generation technique named as Space-Vector based PWM(SV-PWM) has been deeply studied since the linearly controllable output voltage of the SV-PWM can be greatly extended compared with that of the conventional sinusoidal PWM[3]~[6]. When SV-PWM is adopted for a unit inverter in parallel operation system instead of the sinusoidal PWM, the each output voltage generated by unit inverter can be independently controlled to compound the reference voltages. Therefore, it is possible to greatly reduce the harmonic contents of the output side current by introducing SV-PWM to the parallel connected inverter system.

In this paper, a new parallel operation strategy which minimize the harmonic distortion of the output stage is described. The proposed method is developed on the basis of the SV-PWM in order to increase the linearly controllable voltage range. With the help of the proposed voltage synthesis method, the total harmonic distortion(THD) of the output stage can be greatly reduced in compared with that of the conventional method with sinusoidal PWM or that of the single inverter operation case. The

experimental results with reduced scale test show the feasibility of the proposed voltage synthesis method in any operating condition with the variable voltage and variable frequency (VVVF).
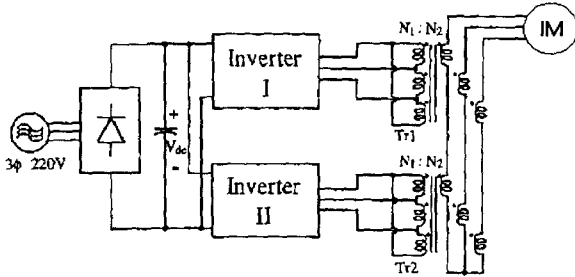
2. System Description

Fig. 1 Schematic of parallel operation system

Fig. 1 shows the schematic of parallel operation system using two inverter systems. In order to increase the whole power capacity of the inverter system, each output stage of the two unit inverters are connected in series through output transformers. It is assumed that two unit inverter systems with output transformer are identical and a unit inverter consists of six GTO devices with reversely connected diodes. It is noticeable that the output transformer is connected in $\triangle$-Y. Therefore, the phase voltage in the induction motor is in-phase with the summation voltage of the line-to-line voltages of the each unit inverter.

3. New Harmonic Reduction Scheme

3.1 Harmonic Reduction Technique

If the harmonic contents of the output stage are not interested in the parallel operation, a simple voltage synthesis technique can be considered using the SV-PWM operating concept, i.e. each inverter works independently with a same reference voltage at the same sampling instance. However, in this case, the same voltage vector is generated in each inverter at the same instance which results in the same THD value of the single inverter case. Therefore, there is no merit in the view of the harmonics.

Considering the stator current ripple of the motor connected to the output stage of the inverter, it is desired that the harmonic components of the inverter output stage should be effectively reduced with minimum effort. In the parallel operation with sinusoidal PWM, the current ripple is reduced by shifting the carrier-waves. This concept can be also applied to the parallel operation with SV-PWM. In this case, the sampling points of inverter I (1,3 in Fig. 2) alternate with the sampling points of

inverter II (2,4 in Fig. 2). By doing so, the current ripple can be reduced to some degree as above method in the parallel operation with sinusoidal PWM.

In Fig. 2, Flag 1 and 2 denote the switching mode of inverter I and II, respectively. If the switching mode is high(low), the upper(lower) switches of the inverter arms are activated and pole voltages go high(low) at appropriate instant. As shown in Fig. 2, the reference voltage of inverter I ($V_I^*(k)$) is sampled from $V^*(K)$ at the time point "1", "3", and that of inverter II ($V_{II}^*(k)$) is sampled from V*(k) at the time point "2", "4".
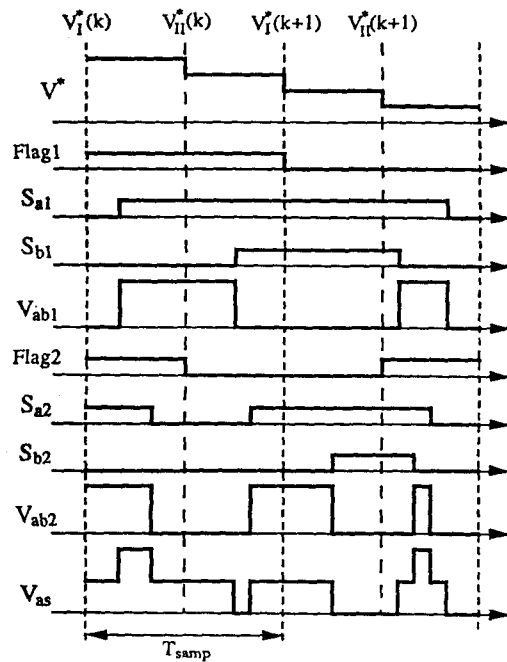

Fig. 2 Switching states and voltages

Eqs. (1), (2) are the time of effective voltage vector in the inverter I and Eq. (3) is the time of zero voltage vector in the inverter I. Also, Eqs. (4), (5) are the time of effective voltage vector in the inverter II and Eq. (6) is the time of zero voltage vector in the inverter II.

$$T_{11} = \frac{\sqrt{3}\left|V^*(k)\right|}{2V_{dc}} T_{samp} \ sin(\frac{\pi}{3} - \gamma(k)) \tag{1}$$

$$T_{12} = \frac{\sqrt{3}\left|V^*(k)\right|}{2V_{dc}} T_{samp} \ sin(\gamma(k)) \tag{2}$$

$$T_{10} = T_{samp} - T_{11} - T_{12} \tag{3}$$

$$T_{21} = \frac{\sqrt{3}\left|V^*(k+1)\right|}{2V_{dc}} T_{samp} \ sin(\frac{\pi}{3} - \gamma(k+1)) \tag{4}$$

$$T_{22} = \frac{\sqrt{3}\left|V^*(k+1)\right|}{2V_{dc}} T_{samp} \ sin(\gamma(k+1)) \tag{5}$$

$$T_{20} = T_{samp} - T_{21} - T_{22} \tag{6}$$

For sufficiently high switching frequency compared to the out put frequency, these scheme produces low current ripples. However, in most high power applications, the switching frequency is not sufficiently high. In that case, therefore, the assumption of the constant reference voltage is no longer valid in high output frequency region. In these situation, as shown in Fig. 2, the unexpected voltages is produced.

3.2 Proposed Harmonic Reduction Technique

The solution for the inappropriate voltage composition as mentioned above is suggested in this section. Since, in general, the dynamics of the high power machine drives is very slow, the trajectory of the reference voltage vectors can be exactly known in steady state. In the proposed system, the reference voltages for two unit inverters are sampled at the same time. However, as shown in Fig. 3, the reference voltage for a unit inverter is composed of the current reference voltage and the predicted reference voltage. Note that the flags of two inverters alternate with logically complement relation. As shown in Fig. 3, at the time point "1", the current reference voltage is sampled for inverter I while a predicted reference by 1/2 sampling time is selected for the inverter II.
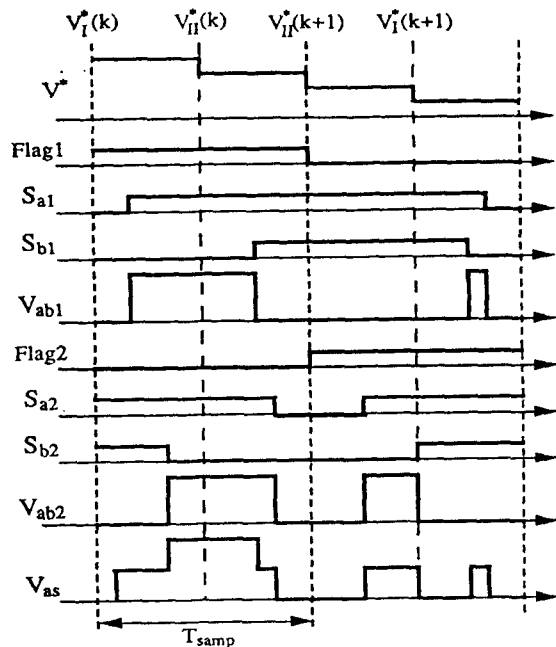

Fig. 3 Switching states and voltages using proposed method

Eqs. (7), (8) are the time of effective voltage vector in the inverter I and Eq. (9) is the time of zero voltage

vector in the inverter I. Also, Eqs. (10), (11) are the time of effective voltage vector in the inverter II and Eq. (12) is the time of zero voltage vector in the inverter II.

$$T_{11} = \frac{\sqrt{3}|V^*(k)|}{2V_{dc}} T_{samp} \ sin(\frac{\pi}{3} - \gamma(k)) \tag{7}$$

$$T_{12} = \frac{\sqrt{3}|V^*(k)|}{2V_{dc}} T_{samp} \ sin(\gamma(k)) \tag{8}$$

$$T_{10} = T_{samp} - T_{11} - T_{12} \tag{9}$$

$$T_{21} = \frac{\sqrt{3}|V^*_{cal}(k+1)|}{2V_{dc}} T_{samp} sin(\frac{\pi}{3} - \gamma_{cal}(k+1)) \tag{10}$$

$$T_{22} = \frac{\sqrt{3}|V^*_{cal}(k+1)|}{2V_{dc}} T_{samp} \ sin(\gamma_{cal}(k+1)) \tag{11}$$

$$T_{20} = T_{samp} - T_{21} - T_{22} \tag{12}$$

In Fig. 3, the inverter II produces a voltage pulse in the time period "3" ~ "5" and the inverter I produces a voltage pulse in the same time period. But, the voltage pulse produced in the inverter II is located in the time period "3" ~ "4", while the voltage pulse produced in the inverter I is located in the time period "4" ~ "5". Consequently, during the time period "3" ~ "5", the voltage pulses of the added voltage V_{as} are distributed sinusoidally. Compared to the method described in the previous section(Fig. 2), the proposed method gives a remarkable improvement in the output voltage synthesis.

4. Experimental Results

In order to verify the feasibility of the proposed scheme, the laboratorial tests are conducted in reduced scale. Two 10kVA inverters and a 3-phase, 220V, 10Hp induction motor are used for experiments. The unit inverter switching frequency is 540Hz to simulate the high power GTO inverter. The TMS320C31 DSP(Digital Signal Processor), which operates at 33.33MHz clock and is capable of 32 bits floating-point operation, is used for implementing two SV-PWM in real time.

Fig. 4 shows the input line-to-line voltage(V_{ab}) and input current(I_{as}) of the induction motor when the same reference voltage is applied to each unit inverter. The considerable amount of harmonics is included in stator current(I_{as}) current of the motor as shown Fig. 4(b). In Fig. 5 and 7, the output voltages(V_{ab1}, V_{ab2}) of inverter I , II, the stator current(I_{as}) and the phase voltage(V_{as}) of the motor are shown. The experimental results using the conventional method are hown in Fig. 5 and 6.
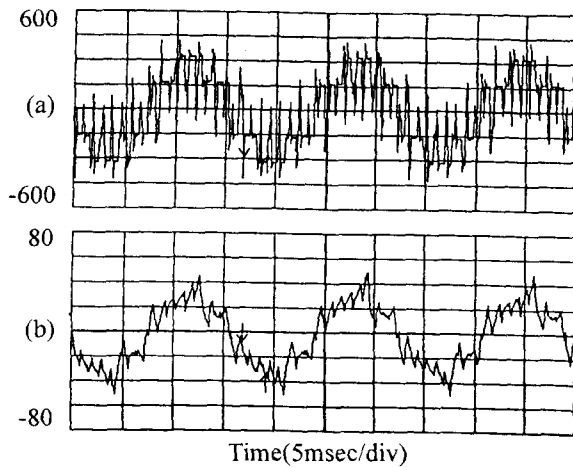
Fig. 4 Output waveforms using same reference voltage
(0.6 p.u. load, 60Hz based)
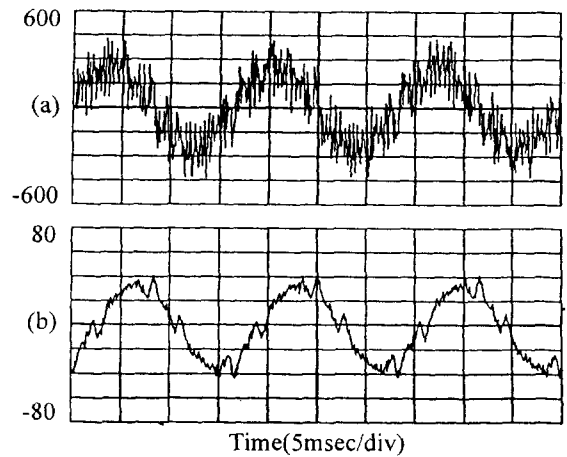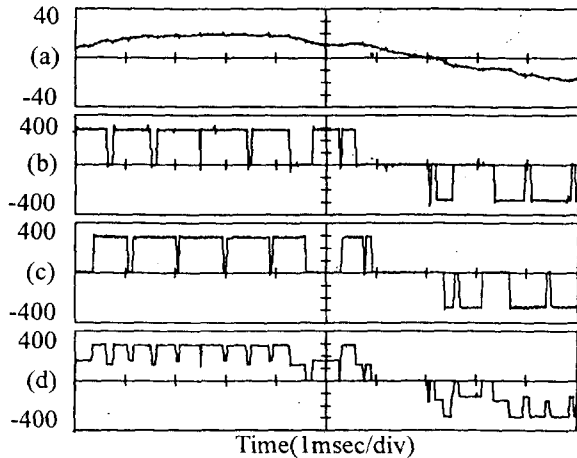(a) line-to-line voltage (b) stator current

Fig. 5 Output waveforms using conventional method
(No Load)
(a) input current (b) output voltage of inverter Ⅰ
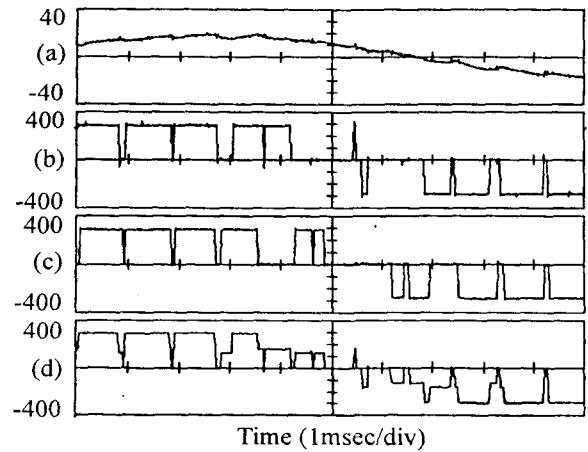(c) output voltage of inverter Ⅱ (d) phase voltage

In Fig. 5(d), the inappropriate voltage is shown and it results in the current distortion as shown in Fig. 6(b). The experimental results using the proposed method are shown in Fig. 7 and 8. In Fig. 7(d), the composed voltage pulses are distributed more sinusoidally than those of conventional method. Also the motor stator current (Fig. 8(b)) has lower harmonic components and current ripples than those of the conventional method (Fig. 6(b)).

To compare the actual THD of stator currents, FFT results are presented in Fig. 9. As shown Fig. 9(a), the low order harmonics (5th, 7th, 11th, 13th,...) are contained in the stator current. On the other hand, in Fig. 9(b), there are no low order harmonics, but the high order harmonics exist in the neighbor of switching frequency.
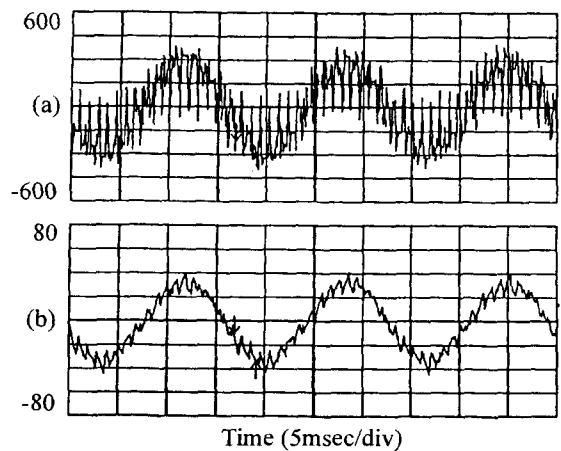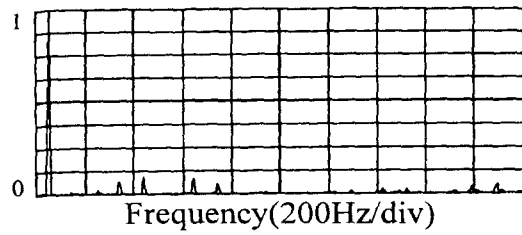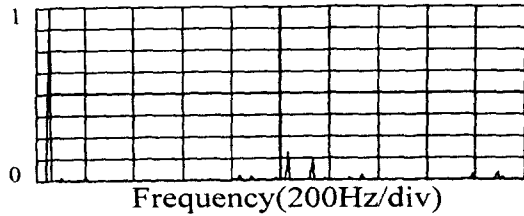

Fig. 6 Output waveforms using conventional method
(0.6 p.u. load, 60Hz based)
(a) line-to-line voltage (b) stator current

Fig. 7 Output waveforms using proposed method
(No Load)
(a) stator current (b) output voltage of inverter Ⅰ
(c) output voltage of inverter Ⅱ (d) phase voltage

Fig. 8 Output waveforms using proposed method
(0.6 p.u. load, 60Hz based)
(a) line-to-line voltage (b) stator current

(a)

(b)

Fig. 9 FFT analysis of stator current for
(a) conventional method (b) proposed method

5. Conclusions

In this paper, a new parallel operation strategy with the reduction of the harmonic distortion of the output current is proposed. With the help of the proposed voltage composition method, the total harmonic distortion(THD) of the output current can be greatly reduced in compared with that of the conventional method with sinusoidal PWM or that of the single inverter operation case. The experimental results with reduced scale test show the feasibility of the proposed voltage composition method.

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