논문 99-01-10

Design of Fractional-N Frequency Synthesizer with Delta-Sigma Modulator for Wireless Mobile Communications

Delta-Sigma Modulator를 이용한 무선이동통신용 Fractional-N 주파수합성기 설계

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Abstract

This paper describes a 1 GHz, low-phase-noise CMOS fractional-N frequency synthesizer with an integrated LC VCO. The proposed frequency synthesizer, which uses a high-order delta-sigma modulator to suppress the fractional spurious tones at all multiples of the fractional frequency resolution offset, has 64 programmable frequency channels with frequency resolution of $f_{ref}/64$.

The measured phase noise is as low as -110 dBc/Hz at a 200 KHz offset frequency from a carrier frequency of 980 MHz. The reference sideband spurs are -73.5 dBc. The prototype is implemented in a 0.5 μ m CMOS process with triple metal layers. The active chip area is about 4 mm^2 and the prototype consumes 43 mW, including the VCO buffer power consumption, from a 3.3 V supply voltage.

Keyword: Frequency synthesizer, fractional-N synthesis, phase noise, phase-locked loop, voltage-controlled oscillator, delta-sigma modulator, noise shaping technique

I. Introduction

The recent rapid growth in demand for wireless mobile communications services has provided a strong motivation for designing more highly integrated RFICs with low operating voltage, power, and cost, while meeting performance requirements for wireless communications systems. Scaled CMOS technologies could be more effectively utilized to improve the integration level of the RF transceivers and synthesizers, with resulting further improvements in power dissipation and cost.

A frequency synthesizer, used to generate a local oscillator (LO) frequency for frequency translation in a communication system, is one of the major building blocks for wireless communications devices. Since the synthesizer influences the performance of the overall wireless systems, it should have high performance, specifically low phase noise and low sideband spurs.

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接受日: 1999年3月9日, 修正完了日: 1999年6月1日

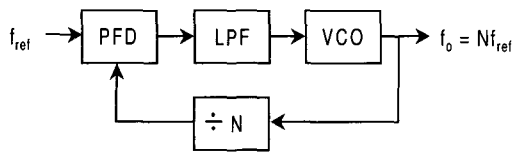


Fig. 1. A PLL-based integer-N frequency synthesizer

A single-loop PLL-based frequency synthesis technique offers high integration level, low power dissipation, small chip area, high reliability, and predictable performance. Typically, a single-loop integer-N frequency synthesis is implemented by a phase-locked loop (PLL) as indicated in Fig. 1.[1-3] When the PLL is in lock state, the frequency of the feedback signal equals the input reference frequency f_{ref}, which results in the output frequency of $f_o = N \cdot f_{ref}$. For a fixed f_{ref}, the desired output frequency f_o is generated by selecting the proper integer N. This means the frequency resolution or frequency step size is f_{ref}. Since the frequency step size is equal to the reference frequency f_{ref}, a low reference frequency f_{ref} must be used to achieve a small channel spacing. A low reference frequency, in turn, mandates a narrow loop bandwidth to keep the PLL stable and to block the signal components at f_{ref} and its harmonics from leaking through to the VCO control input, and modulating its output signal. However, a small loop bandwidth greatly increases the frequency acquisition time of the PLL following a channel switch event, and reduces VCO noise suppression potential of the PLL. Another drawback comes from the inverse relationship between the channel frequency spacing and phase noise. As the channel frequency spacing decreases, the divide ratio of the programmable frequency divider for a given LO frequency range must increase. The higher the divide ratio, the worse the phase noise inside the loop bandwidth close to the carrier frequency. The in-band phase noise is higher than system noise floor by about an amount of $20\log N$, where N is the total divide ratio[2][4]. Thus, a single-loop integer-N frequency synthesis, which commonly uses a dual-modulus prescaler and cycle-swallowing technique[3], might be unsuitable for the wireless systems requiring both low in-band phase noise and fast switching time.

Fractional-N synthesis technique[1-2][6-7] enables the use of reference frequencies larger than the channel frequency spacing. This technique is able to considerably reduce the divide ratio N in the loop for the same channel frequency spacing and output frequency range, while using the highest possible reference frequency. This has a significant beneficial side effect on the in-band phase noise performance of the synthesized output. The possibility of using a higher reference frequency also opens up the way to a wider loop bandwidth, hence faster switching time. Using a reference frequency higher than the channel frequency spacing can reduce the reference spurs at the output. However, use of the fractional-N technique introduces periodic disturbances in the loop, resulting in a large fractional spurs at all multiples of the offset frequency depending on the fractional input data.[1]

This paper presents a PLL-based fractional-N frequency synthesizer, which has an integrated voltage-controlled oscillator (VCO), that operates in the frequency band of 865 MHz to 1 GHz. The CMOS frequency synthesizer described in this paper employs a noise shaping method to suppress the fractional spurs using high-order discrete-time delta-sigma modulator. In Section II, the fractional-N frequency synthesis technique is described in detail. The proposed fractional-N synthesis uses a high-order delta-sigma modulator as a modulus controller for the multimodulus prescaler. Section III briefly describes circuit implementation to achieve low noise and low power. Experimental results are summarized in Section IV. Finally, conclusions are given in Section V.

Ⅱ. Fractional-N Synthesizer

2.1. A Concept

Fractional-N synthesizer has been developed to solve frequency resolution and acquisition time limitations and to improve the in-band phase noise at a VCO signal.[1-2][6-7] Shown in Fig. 2 is a typical fractional frequency synthesizer[1]. Using a dual-modulus divider and an m-bit binary accumulator, the idea of fractional division is to make the division ratio alternate between N or N+1 in a controlled and repetitive fashion, in such a way that on average an intermediate fractional value is obtained.

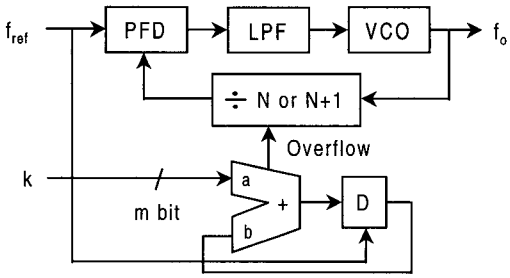


Fig.2. A typical fractional-N frequency synthesizer

A brief overview of the system shown in Fig. 2 is presented here to underscore the operation of a simple fractional frequency synthesis. The carry-out from a binary m-bit accumulator sets the divide ratio of a dual-modulus divider. The output frequency, for example, is divided by N+1 when there is an overflow and otherwise by N. The average division ratio is then $N+\frac{k}{2^m}$ for accumulator input k, and the average output frequency is given by

$$f_o=\left(N+\frac{k}{2^m}\right)f_{ref}=(N+F)\ f_{ref} \qquad (1)$$

where N and $F=\frac{k}{2^m}$ denote the integer portion and fractional portion of the effective division ratio, respectively. This expression shows that the output frequency can be varied in fractional increments of the reference frequency by changing accumulator input k, and fast switching time can be achieved by choosing wide loop bandwidth due to larger reference frequency than the channel frequency spacing. A smaller division ratio N can be chosen by selecting a proper reference frequency for a given output frequency band. This implies that the in-band phase noise of the output signal can also be improved.

Although the fractional-N technique has a very good potential for solving the acquisition time and frequency resolution limitations and improving the in-band phase noise of the VCO signal, it has its own drawbacks. The VCO signal contains the fundamental rate of the jitter because the instantaneous VCO frequency is modulated by the state of an accumulator. This causes the so-called fractional sideband tones at all multiples of the offset frequency $F\cdot f_{ref}$.[1] Since the fractional spurs can fall inside the loop bandwidth, fractional-N synthesizers are not practical unless in-band spurs are suppressed to a negligible level. Several spur reduction techniques have been reviewed in Ref.[2].

2.2 Noise Shaping Technique

As discussed earlier, a fractional-N synthesizer shown in Fig. 2 produces high spurious sideband tones at all multiples of the resolution frequency selected due to the periodic change of the instantaneous frequency of the VCO signal. The spurious tones can be suppressed to a negligible level using a noise-shaping technique.[1][6-7] The idea is to eliminate the low frequency phase error by rapidly switching the divide ratio between different ratios to eliminate the gradual phase error at the phase/frequency detector (PFD). By

changing the divide ratio rapidly between different values, the phase error occurs in both polarities, positive as well as negative, at a rapid rate that explains the phenomena of high frequency noise push-up. This noise, which is converted to a voltage by a PFD and loop filter, is then filtered out by the loop filter.

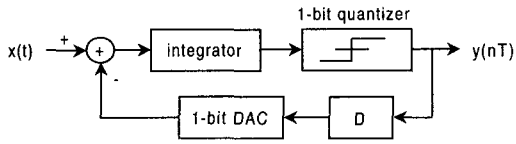
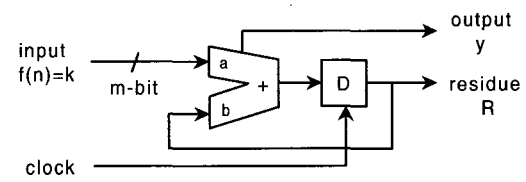


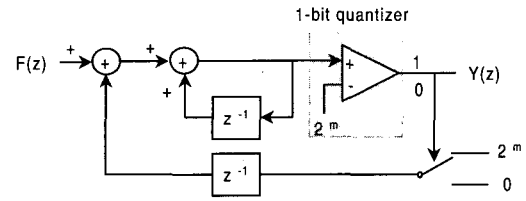
Fig.3. First-order analog delta-sigma modulator

An analog first-order delta-sigma modulator is shown in Fig. 3.[5] The input to the circuit feeds to a 1-bit quantizer through an integrator, and the quantized output y(nT) feeds backs to subtract from the input. This feedback forces the average value of the quantized signal to track the average input. As the loop integrates the error between the quantized signal and the input signal, it low-pass filters the signal and high-pass filters the quantization noise. In other words, the signal is left unchanged as long as its frequency contents does not exceed the cut-off frequency of the filter, but the delta-sigma loop pushes the quantization noise into a higher frequency band.

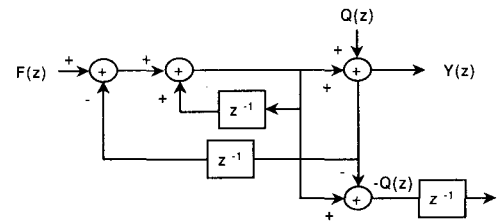
A discrete-time delta-sigma modulator can be implemented by replacing the analog blocks in Fig. 3 with their discrete equivalents. The analog differencer is replaced with a discrete differencer, the analog integrator with a discrete integrator, and the DAC can be removed since the input signal is discrete. The discrete-time first-order delta-sigma modulator can be implemented by using an m-bit accumulator.[1-2][6] The m-bit accumulator has m input bits, a single output bit (carry-bit or MSB), and m-bit residue as shown in Fig. 4. The residue signal represents the quantization error in the output signal. The residue output R in the accumulator is assigned the value R+k after one cycle of the reference clock if an overflow does not occur, i.e. y=0, or $R+k-2^m$ if the accumulator produces a carry-bit signal. In this way, the accumulator overflow is equivalent to the comparator decision in Fig. 4(b). The stored data in the accumulator is then essentially the integral error between the desired frequency data k and the actual frequency control input. In Fig. 4(b), F(z) indicates the Z-transform of the desired fractional portion, the output 0 means no carry generation, and the output 1 indicates carry generation. Finally, a discrete-time first-order delta-sigma modulator implemented by a binary m-bit accumulator could be modelled as shown in Fig. 4(c).



(a)



(b)



(c)

Fig. 4 (a) An m-bit accumulator, (b) model of the accumulator, and (c) a complete Z-domain model of the accumulator.

Standard discrete-time signal analysis for the first-order delta-sigma modulator of Fig. 4 yields

$$Y(z) = F(z) + Q(z) \cdot (1 - z^{-1}) \quad (2)$$

As indicated in Eq.(2), the single-bit carry output of a discrete-time accumulator is made up of two factors: the first is the desired term while the second, though undesired, is high-pass filtered quantization noise. Therefore, provided that the fractional data to the modulator, F(z), is oversampled, i.e. the reference clock frequency is much larger than the required resolution frequency, the quantization noise pushed into high frequency band can be suppressed by the loop filter in the PLL loop without affecting the fractional input characteristics residing in the loop bandwidth.

Higher-order cascaded delta-sigma modulator[5] has been chosen to implement the prototype. When multiple first-order modulator are cascaded to obtain higher order modulator, the signal that is passed to the successive loop is the quantization error from the current loop. If the input signal to the second stage delta-sigma loop is the negative quantization noise, $-q_1(n)$, of the first loop, the quantized outputs for the first stage and second stage loop are given by

$$Y_1(z) = F(z) + (1 - z^{-1})\, Q_1(z) \quad (3)$$

and

$$Y_2(z) = -Q_1(z) + (1 - z^{-1})\, Q_2(z) \quad (4)$$

which yield the output for the second-order delta-sigma modulator after bit manipulation as

$$\begin{aligned} Y(z) &= Y_1(z) + (1 - z^{-1})\, Y_2(z) \\ &= F(z) + (1 - z^{-1})^2\, Q_2(z) \end{aligned} \quad (5)$$

where Y(z) is the Z-transform of y(n). Similarly for the nth-order modulator the output is given by

$$Y(z) = F(z) + (1 - z^{-1})^n\, Q_n(z) \quad (6)$$

where $Q_n(z)$ is the quantization noise from the nth stage. From Eq.(6) it is concluded that higher-order modulators perform a higher-order difference operation of the error produced by the quantizer and thus stronger attenuation at low frequencies for the quantization noise. Fig.5 shows a simplified third-order delta-sigma modulator for the prototype. The output range of a modulator based on three modulators is -3 to 4.

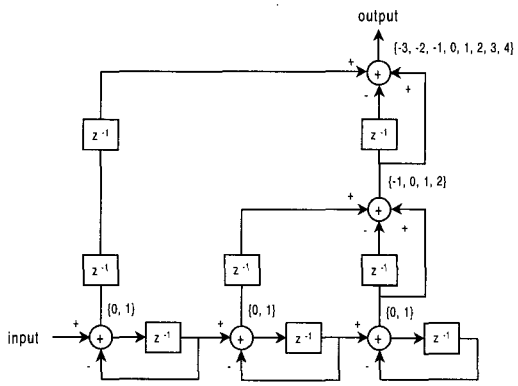


Fig.5. A third-order delta-sigma modulator for the prototype

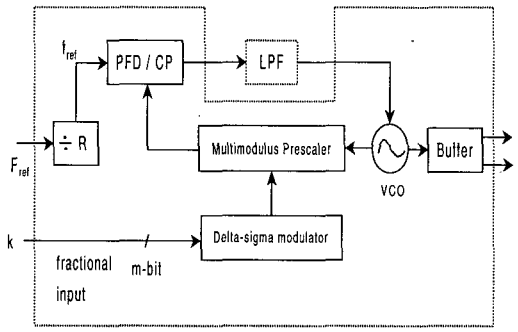


Fig.6. Simplified block diagram for the prototype

The block diagram of the prototype is shown in Fig 6. It consists of a reference divider R, a phase-frequency detector and charge pump, a LC VCO, a RF output buffer, a multimodulus prescaler, a third-order delta-sigma modulator, and a control generator to generate control signal for the multimodulus signal. When the PLL is locked, the RF output

frequency is

$$f_o = \frac{1}{R}\left(N + \frac{k}{2^m}\right) F_{ref} \quad (7)$$

where R is the divide ratio of the reference divider, N the integer part of the divide ratio of the feedback frequency divider, k the desired fractional input, m the bit size of the accumulator, and F_{ref} the frequency of the external reference signal. The output frequency is varied in $(F_{ref}/R) \cdot (k/2^m)$ frequency resolution. For a given frequency resolution, the effective divide ratio can be reduced by choosing a higher comparison frequency, $f_{ref} = F_{ref}/R$, than the frequency resolution, which reduces the in-band phase noise of the synthesized signal.

Ⅲ. Circuit Design

A multimodulus prescaler[2][4], which has several divide ratios controlled by the output of the delta-sigma modulator, is designed to simplify the hardware required for the design of fractional-N frequency synthesizer. The proposed multimodulus prescaler consists of a 8/9 dual modulus prescaler, a four-stage extender, a control logic, and a two-input multiplexer.[4] The divide ratio for the prescaler is set to be N-3 to N+4, which corresponds to the number of the output state of the third-order delta-sigma modulator.

Realization of a high-speed prescaler in mixed environment requires careful attention to certain aspects of the circuit design to contribute low noise to sensitive analog circuits such as a VCO, which shares the same substrate with noisy circuits, and to the synthesized output signal. Current-mode logic (CML) instead of a static CMOS logic is used to implement the prescaler. The CML uses constant current source, which causes lower digital noise generation, and differential signals at both input and output, which reduce coupling noise from the supply line and substrate because the inherent differential circuits reject the common-mode signals such as the power supply and substrate noise.

Another issue for the prescaler design is reduction in power consumption at a given frequency range. Most power consumption in the prescaler occurs in the front-end synchronous divider because it is the part of the circuit operating at the maximum frequency of the input frequency. A rising edge-triggered D-type flip-flop with an embedded NAND gate is used in the front-end design to reduce power consumption.[4] An edge-triggered T flip-flop implemented by a D-type flip-flop with feedback provides two signals: master (Qi) and slave (Q) outputs (Fig. 7). The master output always leads the slave output by 90 degree. The master outputs are used as the inputs to the control logic gates of the prescaler to relax the delay requirements in a critical path, which in turn causes reduction in power consumption.[2]

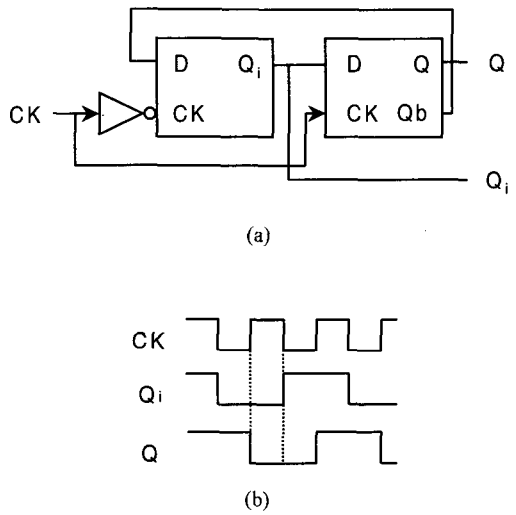


Fig. 7 (a) Positive edge-triggered T-type flip-flop and (b) its timing diagram.

A PFD and charge pump are designed to minimize the dead zone and results in improved spurious performance. The PFD uses modified D-type flip-flops

with small number of devices in signal path to increase speed to extra delay gates to increase the reset delay, thus eliminating the dead zone.[4] A charge pump (Fig. 8) consists of a cascode output stage for high impedance, constant current sources, and switches. The peak output current of the charge pump is designed to be 300 μA. When Dn is on, the charge pump sinks the current I_{out} from the loop filter and when Up is on, the charge pump sources the current I_{out} to the loop filter. The switches Up and Upb could be implemented by a PMOS and transmission gate, respectively. The switches Dn and Dnb could be implemented by NMOS transistors. Large transistors are suitable for the current sources to keep good matching between the sinking and sourcing currents for low sideband spurs. However, the large devices increase parasitic capacitance, decreasing the response speed and thus introducing dead zone to the combination of the PFD and charge pump. Thus, the trade-offs between the response speed and matching are needed. The proposed charge pump consumes low power because the switches turn on only during the small time slot of the reference period if the PLL is locked. The charge pump has a voltage compliance of 300 mV from either rail to minimize the required VCO tuning sensitivity, to cover wide frequency range, and to overcome process variations.

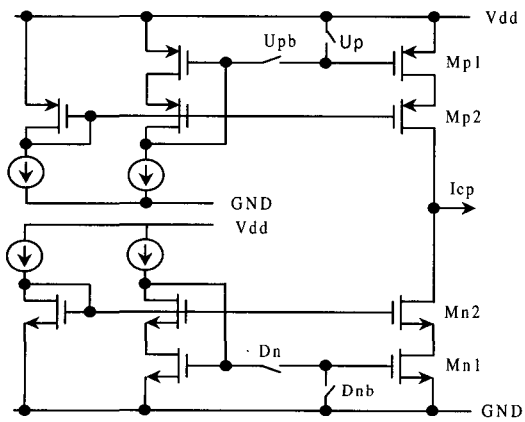


Fig. 8 A proposed charge pump.

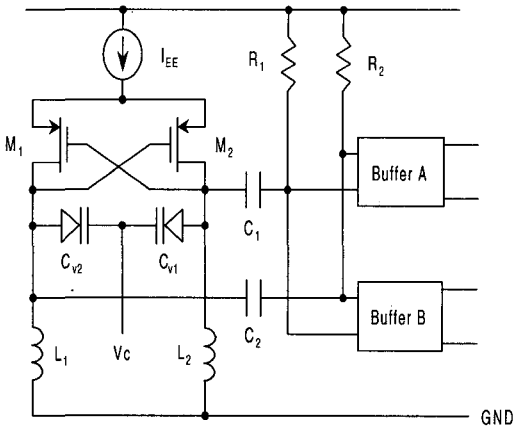


Fig.9. A Integrated LC VCO with buffers

A monolithic, fully differential, voltage-controlled oscillator with a single control input, designed using on-chip spiral inductors, varactors, and a cross-coupled differential pair as a negative resistance for a LC resonator is shown in Fig. 9. The fully differential architecture of the VCO provides more power supply rejection as well as more common-mode noisy immunity compared to single-ended designs. Two buffers are integrated to isolate the VCO pulling. AC coupling filters (C_1, C_2, R_1, and R_2) are designed to interface the VCO signals to the buffers. The resistors should be large enough to minimize their loading effects on the VCO RF output. PMOS transistors instead of NMOS transistors are used in the VCO core because PMOS has lower flicker noise than NMOS and is built in an N-well, thus having less substrate noise pick-up than its counterpart. Device size for M_1 and M_2 at a given power consumption are determined by noise matching technique to minimize phase noise contribution.[8]

Spiral inductors are implemented in metal 3 with a spacing of 2.1 μm and a trace width of 16 μm. The inductors have 5 turns and a $300 \cdot 300$ μm^2 outer size. The inductor has a value of 7.5 nH and quality factor of about 8.5 at 930 MHz.

With an inductance of 7.5 nH, the total capacitance must be about 3.7 pF to obtain an oscillation frequency of 950 MHz. The capacitance of the LC resonator is formed by the parasitic capacitance between the inductor and the substrate, the drain-bulk, gate-drain and gate-source capacitance of the transistors, the loading capacitance of the buffers, and a tunable p^+/n-well junction capacitance. In order to achieve a large tuning range, the contribution of the tuning capacitor to the total capacitance must be as large as possible.

Varactors (C_{v1} and C_{v2}) are implemented by a p^+ diffusion in an n-well layer. An interdigitating layout is used to decrease the series resistance, thus increasing the quality factor Q of the varactor and finally increasing loaded quality factor of the LC resonator, which results in low phase noise.

Ⅳ. Experimental Results

The prototype has been fabricated in a 0.5 μm CMOS technology with three metal layers and consumes 43 mW at a 3.3 V supply voltage.

For various control voltages, the output frequency is measured by a spectrum analyzer, while the output power at the VCO buffer are measured. Fig.10 shows a plot of the measured output frequency versus control voltage of the integrated LC VCO. The tuning range is 865 MHz to 1005 MHz with a control voltage of 0.4 V to 3.0 V at a supply voltage of 3.3 V. Due to the nonlinearity in the on-chip varactor diode capacitance to voltage ratio, the VCO sensitivity is lower at higher frequencies (larger reverse bias voltage across the varactor diode). Fig.11 shows a plot of the measured output power versus output frequency. As shown in the figure, the output power variation over frequency is about 1.0 dB. The slight increase in the output power with frequency is due to increase in the quality factor of the inductors with frequency.

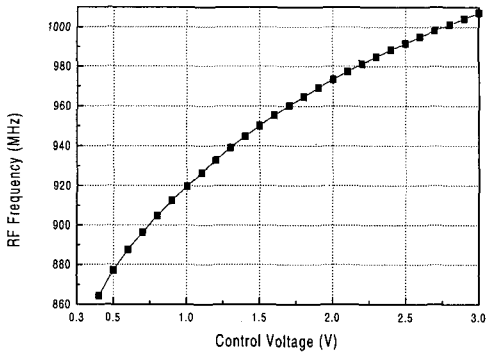


Fig.10. Tuning characteristics of the VCO

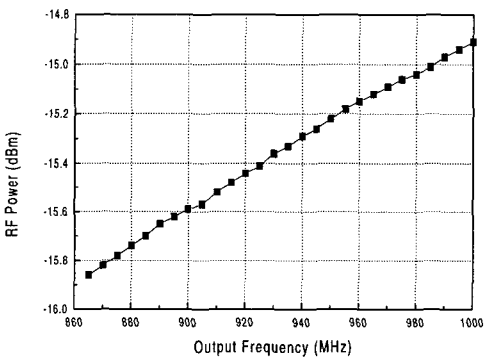


Fig.11. MEasured RF output power versus frequency

To test the signal quality at the output in a closed-loop PLL, the loop bandwidth of the PLL was set to 20 KHz. The single-sideband (SSB) phase noise within the PLL closed-loop bandwidth is nearly flat close-in the carrier (up to a few KHz offset). The close-in phase noise portion is the multiplied-up noise floor of the phase/frequency detector, the reference divider, and the prescaler. The integration of the area under the curve gives the RMS phase noise value in radians or degrees. This is one of the primary contributions to the overall transmitter modulation phase

accuracy. The integrated RMS phase noise, which can be measured within the loop bandwidth using the Phase Noise Analyzer, is around 2°. Fig.12 shows the SSB phase noise with a loop bandwidth of 6 KHz. The fractional input data k is programmed to be 1, which gives the carrier frequency of $f_o = 14MHz \cdot (70 + 1/64)$, resulting in a carrier frequency of 980.219 MHz. The measured phase noise is -110 dBc/Hz at a 200 KHz offset and -118 dBc/Hz at a 600 KHz offset. The measured phase noise with k=1 is the same as that with k=0, which means that the high frequency noise power due to the delta-sigma fractional division is suppressed by a narrow-band loop filter. With a 20 KHz loop bandwidth, the PLL loop suppresses the high frequency noise power of the modulator to a negligible level. As shown in Fig.12, none of the fractional spurs corresponding to the fractional input are present.

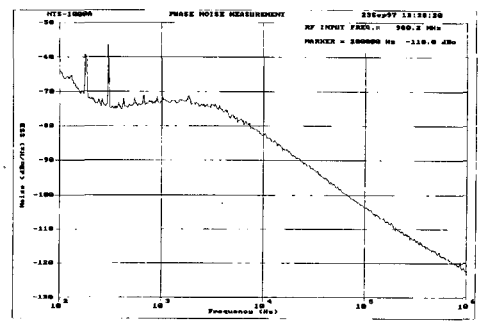


Fig.12. Single-sideband phase noise

Fig.13 shows the measured sideband spurs. The measured sideband spurs are less than -73.5 dBc. The main sources of the spurs are the leakage current in the varactor diode, the leakage current of the charge pump itself, the mismatches between the sourcing and sinking currents of the charge pump, and the switching mismatches in the charge pump. Also, the spur level is dependent on the PLL loop bandwidth. Although the level of the sideband spurs are more related to the performance of the synthesizer circuits, the spur level can be degraded by a leakage signal coupling through the substrate. According to measurements, the sideband spurs are limited by the substrate coupling. This means that the spurs in the prototype can not be reduced by decreasing the loop bandwidth if the loop bandwidth is less than 40 KHz. Thus, the reduction in signal coupling via the substrate is important to get lower sideband spurs. Table 1. shows the summary of the measurement results of the prototype.

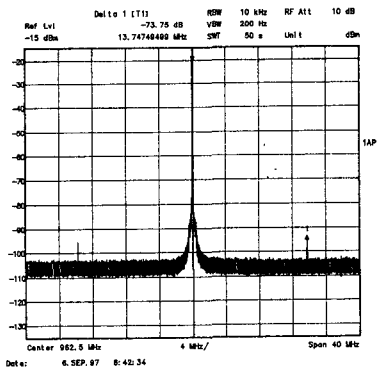


Fig.13. Reference sideband spurs with a loop bandwidth of 20 KHz

Table 1. Summary of experimental results

Items	Measured Results
Technology	0.5 μm CMOS
Phase noise @ 200 KHz	- 110 dBc/Hz
RF power variation	1.0 dB
Frequency range	865 - 1005 MHz
In-band RMS noise	2 degree
Reference spurs	less than -73.5 dBc
Second harmonic	-30 dBc
Power dissipation @ Vdd=3.3V	43 mW

V. Conclusions

A prototype fractional-N synthesizer with a low-phase noise LC VCO, a third-order cascaded delta-sigma modulator, and a multimodulus prescaler is successfully demonstrated for wireless communications applications in a 0.5 μm CMOS technology with triple metal layers. The synthesizer consumes low power while producing very low phase noise and sideband spurs.

An integrated LC VCO has low SSB phase noise performance of -104 dBc/Hz at a 100KHz offset, -110 dBc/Hz at a 200 KHz offset, and - 118 dBc/Hz at a 600 KHz offset with a carrier frequency of 980 MHz. The tuning range is 865 MHz to 1005 MHz with a control voltage of 0.4 V to 3.0 V at supply voltage of 3.3 V. The VCO consumes 7 mW at a 3.3V supply voltage. Table 2 shows the performance comparison of several VCOs with on-chip LC resonator.

The proposed fractional-N synthesizer, which uses the integrated LC VCO and a third-order sigma-delta modulator with a multimodulus prescaler, has 64 programmable frequency channels with a frequency resolution of $f_{ref}/64$. The measured closed-in RMS noise is less than 2^{o}. The measured phase noise at a 200 KHz offset is as low as -110 dBc/Hz. The sideband spurs are measured to be -73.5 dBc with a loop bandwidth of 20 KHz. These results show the possibility that scaled submicron CMOS technology can be used for high integration level and good performance fractional-N frequency synthesis.

Table 2. Performance comparison of VCOs with on-chip LC resonator

Design	Tehnology	Freq. (GHz)	Power (mW)	Reported phase noise (dBc/Hz)	Normalized phase noise (dBc/Hz)
Ref. [9]	0.7 μm CMOS	1.8	6	-116 @ 600 KHz	-112
Ref. [10]	0.6 μm CMOS	1.8	7.6	-90 @ 100 KHz	-101.4
Ref. [11]	11GHz BiCMOS	1.476	28	-105 @ 100 KHz	-114.6
Ref. [12]	1 μm CMOS	0.85	30	-100 @ 100 KHz	-104.9
Ref. [13]	25GHz Bipolar	0.913	10	-101 @ 100 KHz	-106.5
Ref. [14]	0.5 μm BiCMOS	4	24	-106 @ 1 MHz	-104.3
Ref. [15]	10 GHz Bipolar	1.1	43.2	-105 @ 100 KHz	-112.1
This work	0.5 μm CMOS	0.98	7	-110 @ 200 KHz	-110

References

[1] U. L. Rohde, *Digital PLL Frequency Synthesizers: Theory and Design*, Prentice-Hall, Englewood Cliffs, NJ, 1983.

[2] B. H. Park, "A Low-Voltage, Low-Power 900 MHz CMOS Frequency Synthesizer," *Ph.D. thesis*, Georgia Institute of Technology, USA, December 1997.

[3] 이정현, 이상오, 여민종, 류인효, 박병하, "A 9mW 1.2GHz Frequency Synthesizer IC with minimal Reference Spurs," *제6회 한국반도체학술대회*, pp.353-354, Feb. 1999.

[4] B. H. Park and P. E. Allen, "A 1GHz, Low-Phase-Noise CMOS Frequency Synthesizer with Integrated LC VCO for Wireless Communications," *in Proc. IEEE CICC*, pp.567-570, May 1998.

[5] James C. Candy and Gabor C. Temes, *Oversampling Delta-Sigma Data Converters: Theory, Design and Simulation*, IEEE Press, 1992.

[6] B. Miller and B. Conley, "A MULTIPLE MODULATOR FRACTIONAL DIVIDER," *Forty-Fourth Anual Symposium on Frequency Control*, pp. 559-567.

[7] Tom A. D. Riley, Miles A. Copeland, and Tad A. Kwasniewski, "Delta-Sigma Modulation in Fractional-N Frequency Synthesis," *IEEE J. of Solid-State Circuits*, vol. 28, no. 5, pp. 553-559, May 1993.

[8] B. H. Park, "Low-Power, Low-Phase-Noise CMOS Voltage-Controlled-Oscillator with Integrated LC Resonator," *J. of the Korean Physical Society*, Vol. 33, pp. S252-S257, Nov. 1998.

[9] J. Craninckx and M. Steyaert, "A 1.8-GHz Low-Phase-Noise Spiral-LC CMOS VCO," *in Symposium on VLSI Circuits Digest of Technical Papers*, pp. 30-31,1996.

[10] B. Razabi, "A 1.8GHz CMOS Voltage-Controlled Oscillator," *ISSCC Digest of Technical Papers*, pp. 388-389, Feb. 1997.

[11] L. Dauphinee, *et al*, " A Balanced 1.5GHz Voltage-Controlled Oscillator with an Integrated LC Resonator," *ISSCC Digest of Technical Papers*, pp. 390-391, Feb. 1997.

[12] A Rofougaran, *et al*, " A 900MHz CMOS LC-Oscillator with Quadrature Outputs," *ISSCC Digest of Technical Papers*, pp. 392-393, Feb. 1996.

[13] A. Ali and J. L. Tham, " A 900MHz Frequency Synthesizer with Integrated LC Voltage-Controlled Oscillator Integrated LC Resonator," *ISSCC Digest of Technical Papers*, pp. 390-391, Feb. 1996.

[14] M. Soyuer, " A 3V 4GHz nMOS Voltage-Controlled Oscillator with Integrated Resonator," *ISSCC Digest of Technical Papers*, pp. 394-395, Feb. 1996.

[15] B. Jansen, *et al*, " Silicon Bipolar Familiy for 1.1 to 2.2GHz with Fully Integrated Tank and Tuning Circuits," *ISSCC Digest of Technical Papers*, pp. 392-393, Feb. 1997.

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