Metal Plasma-Etching Damages of NMOSFETs with Pure and N_2O Gate Oxides

Jae-Seog Yoon*, Chang-Wu Hur**

게이트 산화막에 따른 nMOSFET의 금속 플라즈마 피해

윤 재 석*, 허 창 우**

요 약

N_2O 게이트 산화막을 사용한 nMOSFET가 금속 플라즈마 식각 피해에 대한 면역도가 동일한 두께의 순수한 산화막을 갖는 nMOSFET보다 향상됨을 보여준다. Area Antenna Ratio(AAR)를 증가 시킴에 따라 N_2O 산화막을 갖는 nMOSFET는 좁은 초기 분포 특성과 정전계 스트레스하에서 더 작은 열화특성을 보이는 데 이는 Si기판과 산화막 계면에서의 질소기의 영향으로 설명되어진다. 또한 N_2O 게이트 산화막을 사용하면 순수한 게이트 산화막을 사용할 때 보다 금속 Area Antenna Ratio(AAR)과 Perimeter Area ratio(PAR) 의 최대 허용 크기를 더 증가할 수 있다. 이러한 N_2O 게이트 산화막을 갖는 NMOSFET의 개선은 Si기판과 N_2O 산화막 계면에 있는 질소기에 의한 계면 강도의 영향때문으로 판단된다.

Abstract

The metal plasma-etch damage immunity of nMOSFET with N_2O gate oxide is found to be improved comparing to that with regular pure oxide of similar thickness. With increasing the antenna ratio (AR), the characteristics of nMOSFETs with N_2O oxide shows tighter initial distribution and smaller degradation under constant field stress, which is explained by the effect of the nitrogen at the substrate Si/SiO_2 interface. Also, if N_2O gate oxide is used, the maximum allowable size of metal AAR and PAR may be increased to the much larger values. These improvements of nMOSFETs with N_2O gate oxide are attributed to the effect of the interface hardness improved by the nitrogen included at the substrate-Si/N_2O-oxide interface.

* 대진대학교 컴퓨터공학과 교수

** 목원대학교 전자공학과 교수

접수일자 : 1999년 1월 25일

Ⅰ. Introduction

Very thin gate oxides are required for continue device scaling into the deep submicron regime. The reliability of these very thin gate oxides is naturally a very important concern. One of the stress modes that do not scale with the oxide thickness is plasma-charging damage. Improving the gate oxide's immunity to plasma-charging damage is therefore a high priority issue. Plasma processes are widely used in the delineation of fine line pattern and the deposition at low temperature. In the plasma process, the devices are usually exposed to plasma directly and charges are collected by poly-Si or metal antennas. As a result, degradation of thin gate oxides by plasma process has become one of the serious problems in ULSI manufacturing. Several authors discussed the degradation of the breakdown voltage for MOS capacitor with larger Antenna Ratio after plasma processing[1]-[3] and the effect of N_2O oxide on plasma damage after poly-Si gate-etch processing[4]-[6]. However, there are few reports about the effect of the different gate dielectric layers in MOSFET as metal plasma etching. In this paper, we like to report a study of plasma damage immunity of N_2O gate oxide MOSFET after metal plasma-etching process. The distribution of initial characteristics for nMOSFET with N_2O gate oxide is compared with that for nMOSFET with pure gate oxide using the different metal antenna ratios of Common Gate(CG) and Separate Gate(SG) test structures with the various channel widths. Also, the degradation of electrical properties for N_2O oxide nMOSFET under constant field stress is compared.

Ⅱ. Experimental

MOS transistors were fabricated with conventional twin-well process and n^+-poly gate technology. The growth conditions of pure and N_2O gate oxides are shown in Table 1. Sample A, B and C is pure gate oxide, 950℃ N_2O gate oxide and 1000℃ N_2O oxide respectively. After all samples were grown, they were annealed at the growth temperature in N_2 ambient for 10 minutes. The etching of metal lines was carried out in a magnetically enhanced reactive ion etching (MERIE) system. The cathode is connected to a 13.56-MHz RF generator and maintained at 80℃ as indicated by the heat label. The etchant gases used for metal etching are a mixture of Cl_2 and other gases, and the chamber pressure is kept at 170 mtorr.

Table 1. The growth conditions of gate oxides

Items / Sample	H_2O 800℃	N_2O	TOX,eq
A	15 min.	×	88Å
B	8 min. 20s	950℃, 38 min.	87Å
C	7 min.	1000℃, 30 min.	87Å

Sample A: pure oxide
Sample B: 950℃ N_2O oxide
Sample C: 1000℃ N_2O oxide

Table 2 shows metal Area Antenna Ratios and Perimeter Antenna Ratios for Common Gate and Separate Gate structure nMOSFETs used in this work. While metal pad of Common Gate is connected with gates of several nMOSFETs, that of Separated Gate is connected only one polysilicon gate. In this work, the important parameters are Area Antenna Ratios and Perimeter Antenna Ratios because the ratio means how many charges are collected. That is, Area Antenna Ratios is defined as the area exposed to the plasma divided by the area of gate oxide ($AREA_{antenna}/AREA_{gate}$). Perimeter Antenna Ratios is also defined as the perimeter exposed to the plasma divided by the perimeter of gate oxide ($P_{antenna}/P_{gate}$). The numbers following CG or SG in Table 2 represent channel width (W) and length (L).

Table 2. The metal antenna parameters for nMOSFETs measured in this paper

Items / Sample	Channel (㎛)		Metal AR	
	Length	Width	AAR	PAR
CG20/0.6	0.6	20	54	82
CG5.0/0.6	0.6	5	618	937
CG2.5/0.6	0.6	2.6	1018	1544
SG20/0.6	0.6	20	873	68

Ⅲ. RESULTS AND DISCUSSION

Fig. 1 shows the distribution of initial transconductance(G_m) values for pure and N_2O oxide nMOSFETs with different gate oxides and metal ARs. With increasing the metal AR, G_m values are more degraded, that is, more widely distributed and more reduced. SG20/0.6 nMOSFET (the smallest PAR) shows the best distribution, which is better than or similar to the distribution of G_m values for CG20/0.6 nMOSFET (the smallest AAR). Also, CG2.5/0.6 nMOSFET (both the largest AAR and PAR) shows the worst distribution. As shown in table 2, SG20/0.6 has the smallest PAR but it has larger AAR than both CG20/0.6 and CG5/0.6. Therefore the distribution of initial G_m may be explained to be more influenced by PARs than by AARs. While 1000℃ N_2O nMOSFETs show the best distribution, pure oxide nMOSFETs show the worst, irrespective of ARs.

Fig. 2 show the degradation of drain current (I_D) values for pure and N_2O nMOSFETs under positive constant-field stress of E_G=+10 MV/㎝. While 1000℃ N_2O nMOSFET shows the smallest degradation, pure oxide nMOSFET shows the largest degradation. Also, while CG20/0.6 nMOSFET (the smallest AAR and second smaller PAR) shows the smallest degradation, CG2.5/0.6 nMOSFET (the largest AAR and PAR) shows the largest degradation. However, the degradation of SG20/0.6 nMOSFET (the smallest PAR) is slightly larger than or comparable to that

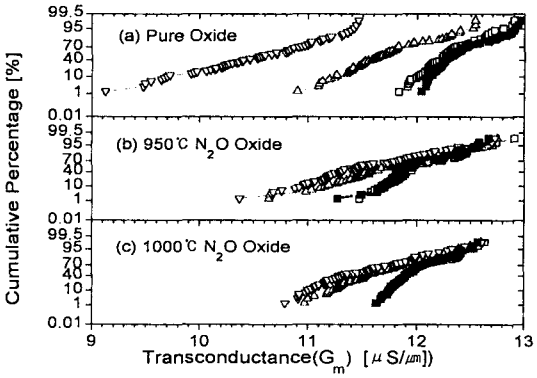

Fig. 1 The distribution for initial G_m values of nMOSFETs with different gate oxides and metal ARs.
□ : CG20/0.6 nMOSFET
△ : CG5.0/0.6 nMOSFET
▽ : CG2.5/0.6 nMOSFET
■ : SG20/0.6 nMOSFET

of CG5/0.6 (second larger PAR). As AAR of SG20/0.6 is larger than AAR of CG5/0.6, the degradation of Fig. 2 may be explained to be more influenced by AAR than by PAR, which is different from the explanation in Fig. 1. The degradation under negative constant-field stress was also measured (not shown). Comparing with the degradation under positive stress, I_D values under negative stress are increased due to hole traps generated at the gate oxide. Also it shows that the difference of degradation for nMOSFETs with different ARs is much smaller. This is similar to the previous reports[2]-[3].

Fig. 3 shows the degradation of I_D values during the Hot Carrier(HC) stress at the maximum substrate current($I_{SUB,MAX}$) condition of V_D=5V. Comparing with pure gate oxide nMOSFET, 950℃ nMOSFET with N_2O gate oxide shows slightly improved characteristics and 1000℃ N_2O nMOSFET shows more improved characteristics. $I_{SUB,MAX}$ values of 950℃ and 1000℃ CG20/0.6 N_2O nMOSFETs are 9.4×10^{-5}A and 1.15×10^{-4}A, respectively, and that

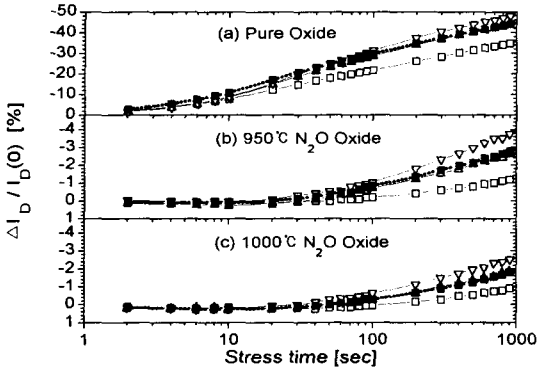

Fig. 2 The degradation of I_D values for nMOSFETs with different gate oxides and metal ARs under positive constant-field stress of E_G=+10MV/cm.

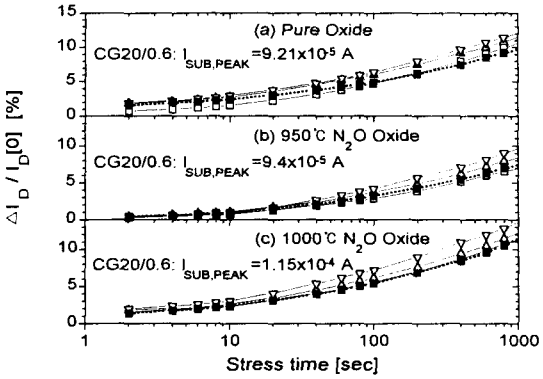

Fig. 3 The degradation of I_D values for nMOSFETs with different gate oxides and metal ARs under HC stress at $I_{SUB,MAX}$ condition of V_D=5V.

of pure oxide CG20/0.6 nMOSFET is 9.21×10^{-5}A. Therefore N_2O nMOSFETs show slightly better HC characteristics than pure oxide nMOSFET.

While Fig. 1 shows that the initial characteristics of nMOSFETs are more influenced by metal PAR than by metal AAR, both Fig. 2 and Fig. 3 show that the degradation of pure oxide nMOSFETs are larger under positive constant-field stress than under HC stress. There are many structures with large metal AAR and PAR in real semiconductor ICs. Thus, If pure gate oxide is used, the size of metal PAR must be restricted to make the variation of initial characteristics for nMOSFETs smaller than the maximum allowable limit. Also, the size of metal AAR must be restricted to make the lifetime under positive stress larger than 10 years. However, if N_2O gate oxide is used, the maximum allowable size of metal AAR and PAR may be increased to the much larger values. These improvements of nMOSFETs with N_2O gate oxide are attributed to the effect of the interface hardness improved by the nitrogen included at the substrate-Si/N_2O-oxide interface [4]-[7].

Ⅳ. CONCLUSION

The metal plasma-etch damage of N_2O oxide nMOSFET has been compared with that of pure oxide. N_2O oxide nMOSFETs have been shown better distribution of initial characteristics and more influenced by PAR than by AAR. Also nMOSFETs with N_2O gate oxide have been shown much smaller degradation under positive constant-field stresses, more influenced by AAR than by PAR, and slightly improved HC characteristics. In conclusion, plasma damage immunity of nMOSFETs with N_2O gate oxide is better than nMOSFETs with pure gate oxide.

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윤 재 석(Jae-Seog Yoon)

1978년 3월~1982년 2월 경북대학교 전자공학과 학사

1983년 3월~1985년 2월 연세대학교 전자공학과 석사

1989년 1월 1991년 5울 미국 Wastington Univ. 전기 및 컴퓨터공학과 M.S.

1994년 3월~1997년 2월 연세대학교 전자공학과 공학박사

1998년 3월~현재 대진대학교 전임강사

*관심분야 : 디지털시스템 및 VLSI 설계, 반도체 소자

허 창 우(Chang-Wu Hur)

1978.3~1982.2 : 광운공과대학교 전자공학과 학사 졸업

1982.3~1984.2 : 연세대학원 전자공학과 석사 졸업

1984.3~1991.2 : 연세대학원 전자공학과 공학박사

1986.9~1994.2 : 금성사 중앙연구소 선임연구원

1994.2~현재 : 목원대학교 전자·정보통신공학부 조교수

*관심분야 : 반도체공학,VLSI설계