Design of A CMOS Analog Multiplier using Gilbert Cell

*Geun-Ho Lee, *Hyun-Seung Choi, *Young-Gyu Yu, *Tae-Pyung Kim,
*Jae-Young Kim, *Dong-Yong Kim

Abstract

The CMOS four-quadrant analog multiplier for low-voltage low-power applications are presented in this thesis. The circuit approach is based on the characteristic of the LV (Low-Voltage) composite transistor which is one of the useful analog building blocks. SPICE simulations are carried out to examine the performances of the designed multiplier. Simulation results are obtained by 0.6μm CMOS parameters with 2V power supply. The basic configuration of the multiplier is the CMOS Gilbert cell with two LV composite transistors. The linear input range of the multiplier is over $\pm$0.4V with a linearity error of less than 1.3%. The measured -3dB bandwidth is 288MHz and the power dissipation is 255μW.

I. Introduction

In recent years, the design of small or battery-operated portable equipment, such as mobile telephones, hand held movie cameras, and radio receivers, has received significant attention. As ULSI technologies advance and the demand for portable and mobile electronic equipment is increasing, it is highly desirable to develop CMOS analog signal building blocks including multipliers which can operate with low supply voltages(lower than 3V) and low power consumption. The trend towards lower supply voltage for integrated circuits requires new design techniques to realize high performance analog multipliers.

A four-quadrant analog multiplier is an important building block of many applications in modern analog VLSI signal and information processing such as modulators, phase-locked loops, frequency mixers and Aut omatic Gain Controlling(AGC) Amplifiers[1]. It can also be applied to frequency doublers, neural networks, correlators, adaptive filters, function generators and other signal processing circuits.

Several techniques of implementing the four-quadrant analog multipliers in CMOS technology have been reported as follows : some of these have been realized on a modified Gilbert cell, which was originally implemented with bipolar transistors, applying the variable transconductance[2]. Others have been based on square-algebraic identity[3] that can be easily performed using the square law characteristics of MOS devices operating in saturation region, or on the current-voltage characteristics of MOS devices working in triode region. Then other multipliers using the quarter square technique[4], pulse width time division technique[5] and composite transistor technique[6] are reported.

The analog multiplier based on variable transconductance principles which lend themselves well to bipolar technology can not easily be extended to MOS technology. This is mainly due to hard to cancel inter-coupled terms in the output current equations. Some multipliers based on the quarter-square principle required the circuits to realize the addition and subtraction of the input signals. Their linear input range is apt to be limited. Pulse-modulation technique can also be employed. Since a sampled-data circuit is used, the maximum signal frequency should be at least one order of magnitude smaller than the clock frequency. Thus this technique handles only low-frequency input signals. Multipliers using composite CMOS pairs were also developed but they required large power supply voltages.

Many CMOS analog multipliers which exploited the MOS transistors operating in the saturation region were developed[3,4]. However, in modern communication and instrument systems, there is a high pursuit of low-voltage low-power and high speed multipliers[7]. With the reduction of power supply voltages, many of the existing CMOS analog multipliers, designed to operate from higher supply voltages, are not suitable for applying to battery-powered systems such as portable communication equipment, radio receivers and hand-held movie cameras. Therefore, a four-quadrant analog multiplier which can operate at less than 3V is highly desirable. To meet the

* Faculty of Electronic & Information Engineering, Chonbuk National University

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requirements of handy and smaller dimensions, modifications of analog circuits have become more necessary.

Ⅱ. Composite cell CMOS multiplier using Gilbert cell

The number of transistors can be reduced by applying the Gilbert cell to composite cell CMOS multiplier. Fig. 1. shows the block diagram of the proposed four-quadrant multiplier which consists of two LV composite transistors and Gilbert multiplier structure and Fig. 2. is the circuit of the complete multiplier, realized in the block diagram in Fig. 1.

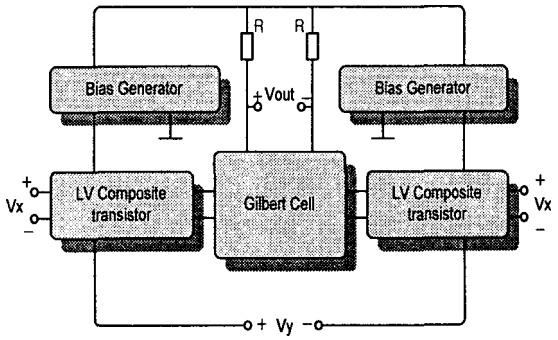

Figure 1. Block diagram of the proposed multiplier.

Assume that all transistors in Fig. 2. are biased in the saturation region and that devices are sized and matched so that the transconductance parameters satisfy the equations $K_1=K_2=K_3=K_4=K_n$ and $K_5=K_6=K_p$. Using the MOS current equation, the differential currents (I_1-I_2) and (I_4-I_3) are given by

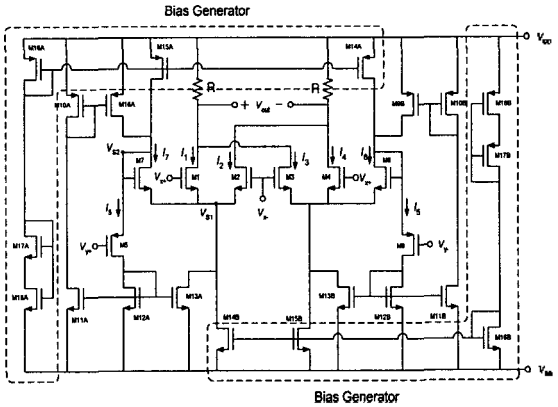

Figure 2. Complete circuit diagram of composite cell CMOS multiplier using Gilbert cell.

$$I_1-I_2=\sqrt{2K_n}v_x\sqrt{I_5}\sqrt{1-\frac{K_n v_x^2}{2I_5}} \tag{1}$$

$$I_4-I_3=\sqrt{2K_n}v_x\sqrt{I_6}\sqrt{1-\frac{K_n v_x^2}{2I_6}} \tag{2}$$

$$\text{If} \quad -\sqrt{\frac{2I_5}{K_n}}\ll v_x\ll\sqrt{\frac{2I_5}{K_n}} \tag{3}$$

$$\text{and} \quad -\sqrt{\frac{2I_6}{K_n}}\ll v_x\ll\sqrt{\frac{2I_6}{K_n}} \tag{4}$$

It follows that the output current becomes linearly dependent on the product of v_x and $(\sqrt{I_5}-\sqrt{I_6})$ and given by the expression of

$$\begin{aligned} I_{out} &= (I_1-I_2)+(I_3-I_4) \\ &= \sqrt{2K_n}v_x(\sqrt{I_5}-\sqrt{I_6}) \end{aligned} \tag{5}$$

If $(\sqrt{I_5}-\sqrt{I_6})$ is made proportional to the input voltage v_y, we can make the output current proportional to the product of v_x and v_y. Using the MOS current equation, the gate-source voltage of each transistor (M1, M5, M7) can be written by

$$V_{cm1}+\frac{v_x}{2}-V_{s1}=\sqrt{\frac{I_1}{K_n}}+V_{Tn} \tag{6}$$

$$V_{s2}-V_{cm2}-\frac{v_y}{2}=\sqrt{\frac{I_5}{K_p}}+|V_{Tp}| \tag{7}$$

$$V_{gs7}=V_{s2}-V_{s1}=\sqrt{\frac{I_7}{K_{n7}}}+V_{Tn} \tag{8}$$

From the above equations, we can obtain an expression for the current I_1.

$$I_1=K_n\left(V_{cm1}+\frac{v_x}{2}-V_{cm2}-\frac{v_y}{2}-\sqrt{\frac{I_5}{K_p}}+\sqrt{\frac{I_7}{K_{n7}}}-|V_{Tp}|\right)^2 \tag{9}$$

In the same way, the current I_4 can be calculated as

$$I_4=K_n\left(V_{cm1}+\frac{v_x}{2}-V_{cm2}+\frac{v_y}{2}-\sqrt{\frac{I_6}{K_p}}+\sqrt{\frac{I_7}{K_{n7}}}-|V_{Tp}|\right)^2 \tag{10}$$

Through some calculations, it can be found that $(\sqrt{I_5}-\sqrt{I_6})$ depends on v_y and is given by the expression

$$\sqrt{I_5}-\sqrt{I_6}=\frac{\sqrt{K_p}(\sqrt{I_1}-\sqrt{I_4})}{-\sqrt{K_n}}-v_y\sqrt{K_p} \tag{11}$$

Substituting (3.32) into (3.26), the output current can then be rewritten by

$$\begin{aligned} I_{out} &= -\sqrt{2K_nK_p}v_xv_y-\sqrt{2}v_x\sqrt{K_p}(\sqrt{I_1}-\sqrt{I_4}) \\ &= -\sqrt{2K_nK_p}v_xv_y\left(1-\frac{(\sqrt{I_1}-\sqrt{I_4})}{\sqrt{K_n}v_y}\right) \\ &= -\sqrt{2K_nK_p}v_xv_y\left(1+\frac{1}{1+\frac{\sqrt{K_n}(\sqrt{I_5}-\sqrt{I_6})}{\sqrt{K_p}(\sqrt{I_1}-\sqrt{I_4})}}\right) \\ &\cong -2\sqrt{2K_nK_p}v_xv_y \end{aligned} \tag{12}$$

The above derivations have shown that the analog multiplier can be implemented by the structure of Fig. 1.

III. Simulation results

Fig. 3. shows SPICE simulations of the DC transfer characteristic of the circuit sweeping vx from -0.4V to +0.4V and stepping vy from -0.4V to +0.4V in 0.1V steps. The simulated linearity error of the multiplier is shown in Fig. 4. The circuit has a linearity error less than 1.3% over ±0.4V input range. The linearity error is degraded due to the nonlinearity characteristic of the Gilbert cell. The simulated -3dB bandwidth is about 288MHz as shown in Fig. 5. Fig. 6. demonstrates the use of the multiplier as a modulator and Fig. 7. shows the performance of the multiplier as a frequency doubler.

The active chip area of the multiplier is $130\times250\ \mu m^2$ and power consumption is $255\ \mu$W. This is achieved mostly because the number of transistors in the multiplier is small, and also because the dimensions of the transistors were chosen to be small. The small area and low power consumption make it suitable for use in the implementation of the integration as part of a large circuit. The complete multiplier's performances are summarized in Table 1. And then the performance comparison results of multipliers are showed in Table 2.

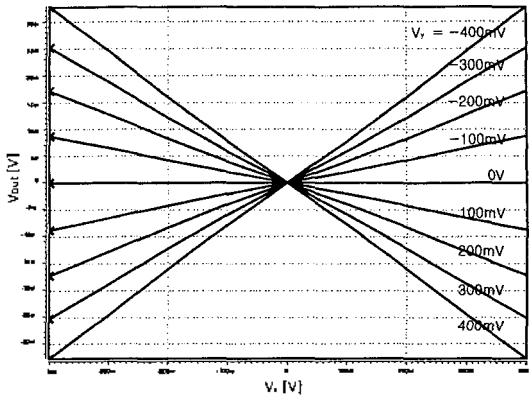

Figure 3. DC transfer curves of the composite cell CMOS multiplier using Gilbert cell.

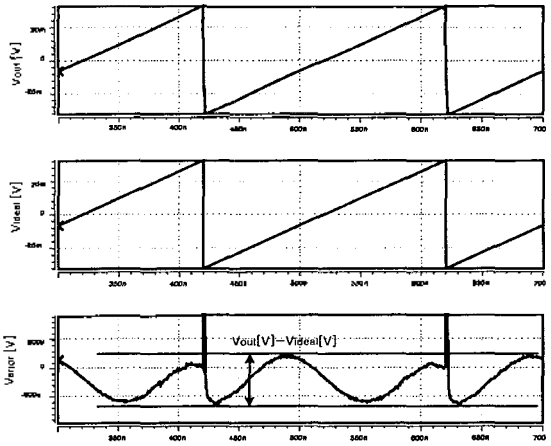

Figure 4. Linearity error of composite cell CMOS multiplier using Gilbert cell.

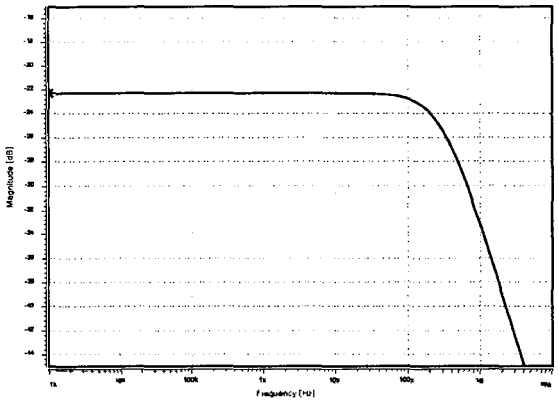

Figure 5. Frequency response of composite cell CMOS multiplier using Gilbert cell.

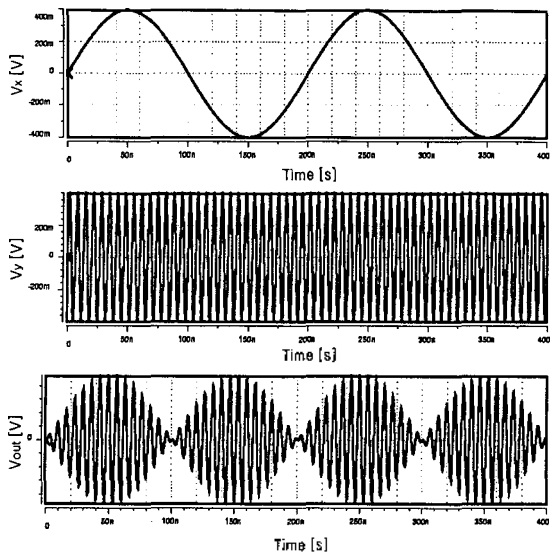

Figure 6. Modulation waveform diagram.

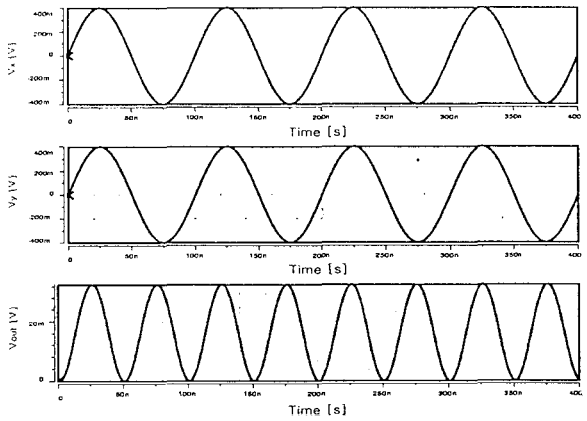

Figure 7. Multiplier of two sine waves of the same frequency.

Table 1. Performances of the multiplier in Fig. 2.

Power supply voltage	2V
Bias currents (M14A~M18A, M14B~18B)	12 μA
Input range	±0.4V
Linearity error	< 1.3%
-3dB Frequency	288MHz
Power dissipation	255 μW
Active chip area	130×250 μm^2

Table 2. Performance comparison results of the multipliers.

	1994 Electron. Letter	1994 Electron. Letter	1996 Electron. Letter	1997 ISCAS	1997 ISCAS	Proposed
Supply Voltage	±1.5V	1.5V	2.5V	±2.5V	1.2V	2V
Input Range	±0.8V	±0.25V	±1V	±1V	±0.25V	±0.4V
Linearity Error	<2%	<2%	<2%	<5%	<0.89%	<1.3%
-3dB Freqeuncy	12 MHz	12MHz	1MHz	230MHz	2.2MHz	288MHz

The composite cell CMOS multiplier using Gilbert cell was fabricated in a 0.8μm n-well CMOS process and its die photograph of the chip is shown in Fig. 8.

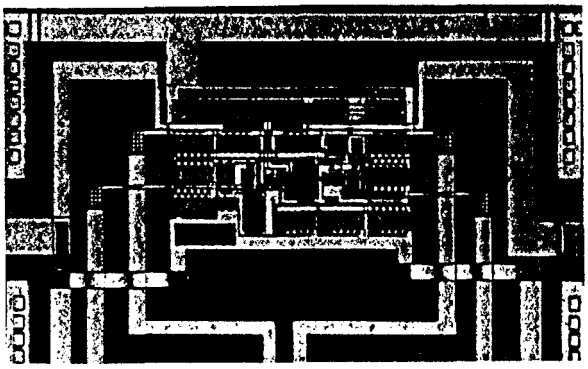

Figure 8. Die photograph of the fabricated chip.

IV. Conclusion

In recent years, the reduction of the power supply voltage has become a main trend in the design of VLSI ICs. This has been driven by increased market demands for mobile or portable battery-operated products. In addition, small chip area and low power consumption are necessary for integration as part of a larger circuit. Circuit designers are forced to reconsider and redesign existing circuits and develop new analog circuits for low voltage operation. In this paper, CMOS analog multiplier based on the characteristics of the LV composite transistor was presented. The designed CMOS multiplier presented in this paper operate from a single 2V supply. The linear input range of the multiplier is over ±0.4V with a linearity error of less than 1.3%. The measured -3dB bandwidth is 288MHz and the power dissipation is 255 μW.

The advantages of the proposed multiplier are simple configuration, small chip area, low power consumption,

and suitable for low supply voltages. Simulation results were given to demonstrate the feasibility of the proposed circuit. The drawback of the proposed multiplier is that linear input voltage range is small. The input voltage range can be extended using active attenuator. However, it degrades signal to noise ratio and linearity characteristics. As a future work, the new method should be considered to increase the input voltage range.

The proposed multiplier is expected to be suitable for analog signal processing applications such as portable communication equipment, radio receivers, and hand-held movie cameras.

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▲ Geun-Ho Lee

Geunho Lee received the B.S. and M.S. degrees in electrical engineering from Chonbuk National University, Korea, in 1994 and 1997, respectively. Currently, he is a Ph.D. student in electrical engineering at the same school. His research interests are analog signal processing, circuits & systems.

▲ Hyun-Seung Choi

Hyunseung Choi received the B.S. and M.S. degrees in electrical engineering from Chonbuk National University, Korea, in 1996 and 1998, respectively. Currently, he is a assistant teacher in electical engineering at the same school. His research interests ars analog signal processing, circuits & systems.

▲ Young-Gyu Yu

Younggyu Yu received the B.S. and M.S. degrees in electrical engineering from Chonbuk National University, Korea, in 1996 and 1998, respectively. Currently, he is a Ph.D. student in electrical engineering at the same school. His research interests are analog signal processing, circuits & systems.

▲Tae-Young Kim

Taepyoung Kim received the B.S. degree from un 1980 and M.S. degrees from Chonbuk National University, Korea, 1999, respectively. Currectly, His research interests are analog signal processing, circuits & systems.

▲ Jae-Young Kim

Jaeyoung Kim received the B.S. and M.S. degrees in electrical engineering from Korea University, Korea, in 1980 and 1986, respectively. Currently, he is a Ph.D. student in electrical engineering at Chonbuk National University. His research interests include analog VLSI design, circuits analysis.

▲ Dong-Yong Kim

Dongyong Kim received the B.S. and M.S. degrees in electrical engineering from Chonbuk National University, Korea, in 1967 and 1973, respectively. In 1985, the Ph.D. degree in electrical engineering from the Manitoba University, Canada. His current research interests include analog signal processing, circuits & systems.