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# HOL블럭킹 없는 공유 다중 버퍼 ATM 스위치 아키텍처 개발 및 성능 평가

# (Design of a Shared Multi-Buffer ATM Switch with Enhanced Throughput in Multicast Environments)

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(Jongick Lee, Jongmoo Sohn, and Moonkey Lee)

요 약

본 논문에서는 각 유니캐스트 셀이 세 번의 연속된 셀 읽기 싸이클마다 공유 버퍼에서 셀을 읽을 수 있고 멀티캐스트 셀은 마지막 읽기 싸이클에서 유니캐스트 셀을 읽기 위해 공유 버퍼가 사용되지 않을 경우에만 읽히도록 하는 공유 다중버퍼형 ATM 교환기를 제안한다. 유니캐스트 셀에 대한 HOL효과는 멀티캐스트 셀에 의해 영향을 받지 않으며, 유니캐스트 셀 뿐 아니라 멀티캐스트 셀도 각 출력 포트에서 읽힐 수 있는 기회가 생기므로 출력 포트의 이용율이 증가한다. 고정된 멀티캐스트 셀 비율에서, 제안된 방법은 제공부하가 1일 경우에도 98.9%의 수율을 보인다. 제안된 공유 다중 버퍼형 ATM교환기는 0.6㎛ single-poly triple metal CMOS 공정을 사용하여 설계되었다. 설계된 교환기는 8 × 8의 포트 크기를 가지며 STM-1의 대역폭 155.52Mbps를 각 포트에서 지원할 수 있도록 20MHz에서 동작한다.

**Abstract**

We propose a shared multi-buffer ATM switch, in which each unicast cell has chances to be read from a shared buffer during three consecutive read cycles and each multicast cell is read from a shared buffer if the shared buffer is not accessed for read of a unicast cell at the last read cycle. The HOL effect that the unicast cells experience is not augmented by the multicast cells and utilization rate of the output ports is increased because both a unicast cell and a multicast cell have the opportunity to be read for each output port. For a fixed multicast rate, the proposed scheme shows 98.9% throughput even though the offered load reaches 1. We designed the proposed shared multi-buffer ATM switch in 0.6um single-poly triple metal CMOS technology. The designed shared multi-buffer ATM switch has 8 × 8 ports and operates at 20MHz, which supports 155.52Mbps STM-1 source rate for each port.

## I. Introduction

There have been extensive studies in an effort to realize a high-speed and high-throughput asynchronous transfer mode(ATM) switch. The shared buffer ATM switch shows high memory utilization efficiency and high throughput.[1-3] In shared buffer ATM switches, ATM cells from input ports are stored in a common memory, called shared buffer memory(SBM) and the cells stored in the SBM are read for all output ports per single ATM cell period. Because the cells are time-multiplexed in shared buffer ATM switch, the required access time to SBM is proportional

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to the port size of the ATM switch as well as to the input/output link speed.

The shared multi-buffer ATM switch is proposed to solve the access time restriction in shared buffer ATM switch. In this architecture, multiple SBMs are provided so that the cells are accessed to the SBMs in parallel. Therefore, the access time is not related to the port size and the high-speed ATM switch is achievable.

The HOL effect occurs in shared multi-buffer ATM switch when cells destined for different output ports reside in the same SBM and are scheduled to be read for their output ports in parallel. The HOL effect degrades the throughput of the switch to 58.6%.[4] It is announced that the consecutive three-read operation for each SBM improves the throughput of the shared multi-buffer ATM switch to 98% for a random traffic situation.[5] The multicasting is the main function for the real time multimedia communications such as video conferencing, video-on-demand and so on. The address-copy multicast scheme has been proposed to support multicast function in shared multi-buffer ATM switch.[6,7] In this scheme, a multicast cell is stored in one cell location of an SBM and the SBM number and the address of the SBM, in which a multicast cell is written, are stored in all the output queues corresponding to the destination ports of the multicast cell. This scheme improves the memory utilization efficiency because a multicast cell is stored in one cell location.

However, as the multicast connections increase, the address data in output queues is augmented in proportion to the destination ports of the multicast cells. In this case, the number of the valid cells in the output queues becomes much greater than the number of the multicast cells stored in the SBMs. This out-numbered valid cells in output queues aggravates the HOL blocking and the throughput of the switch is degraded.

Recently, a scheme is announced to improve the throughput in shared multi-buffer ATM switch by reducing the HOL blocking.[8] In this scheme, each output queue for unicast cells has multiple sub-queues, each for an SBM. The multicast cells are stored in separate queues. The order of read for sub-queues and the slot for the multicast cells are scheduled to reduce the HOL blocking.

However, the unicast cells which reside in the same SBMs as the multicast cells do experience the HOL blocking in the multicast slot. Moreover, hardware complexity is increased because additional control logic is required to guarantee the transmission sequence of cells for each ATM connection.

We propose that queues for multicast cells be separated from those of unicast cells and each multicast cell be read from an SBM in the last third read cycle, only if the SBM is not accessed for read of a unicast cell. In this scheme, the multicast cells do not affect the HOL blocking of unicast cells and the utilization rate of output ports is increased because both unicast and multicast cells have the opportunity to be read for each output port.

We use the length of output queues for unicast cells and the length of multicast queues for multicast cells to determine the read priority of SBM. This scheme reduces the average waiting time of ATM cells in queues.

In section II, we describe the cell-copy multicast scheme and the address-copy multicast scheme. The issue of throughput enhancement in shared multi-buffer ATM switch in multicast environment is dealt in section III. In section IV, the performance evaluation of the proposed multicast scheme is carried out for various traffic conditions. The VLSI design of the shared multi-buffer ATM switch employing the proposed multicast scheme is described in section V. We conclude this paper in section VI.

## Ⅱ. The Current Study on Multicast schemes in Shared Multi-buffer ATM Switch

Two multicast schemes are proposed for shared multi-buffer ATM switch. They are cell-copy multicast scheme and address-copy multicast scheme. In the cell-copy multicast scheme, a cell-copy circuit is located in front of the ATM switch fabric and each multicast cell is copied to generate multiple unicast cells destined to the output ports of the multicast cell. Figure 1 shows the cell-copy multicast scheme. Because a multicast cell generates multiple unicast cells, the buffer utilization efficiency is exacerbated.

Moreover, the total size of the hardware becomes large because the cell-copy circuit is needed in addition to the switching fabric.

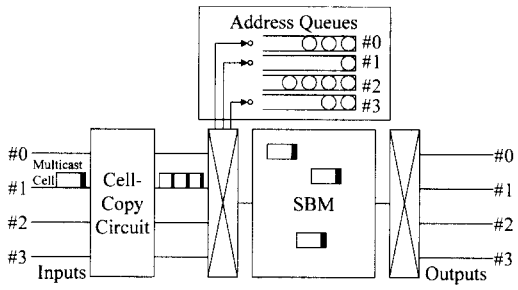


그림 1. 셀 복사 멀티캐스트 방식
Fig. 1. Cell-Copy Multicast Scheme.

The address-copy scheme has been proposed to improve the buffer utilization efficiency. In this multicast scheme, each multicast cell is stored in only one cell location of shared buffer as if it were a unicast cell and the address of the multicast cell in SBM is stored in the output queues corresponding to the destination ports of the multicast cell. Figure 2 shows an example of the multicasting in the address-copy scheme. In Figure 2, a multicast cell arrives whose destination ports are #0, #1, #3. The multicast cell is written in one cell-space in SBM and the address is copied to the output queues corresponding to the destination ports.

In this scheme, Multicast Cell Counters(MCCs) are provided to detect the release time of the addresses where multicast cells are stored. Figure 3 shows the MCCs maintained for each cell location of SBMs. The value of each MCC decreases when a cell is read out from an SBM and sent out to the one of the destination ports. When the value of the MCC becomes zero, the address, at which the multicast cell is stored, is released.

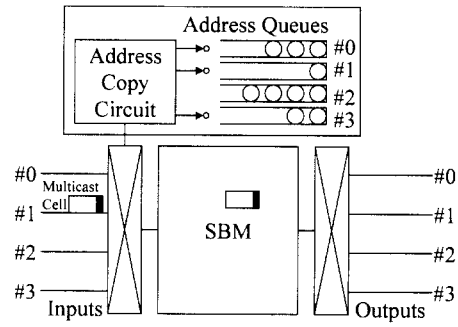


그림 2. 주소 복사 멀티캐스트 방식
Fig. 2. Address-Copy Multicast Scheme.

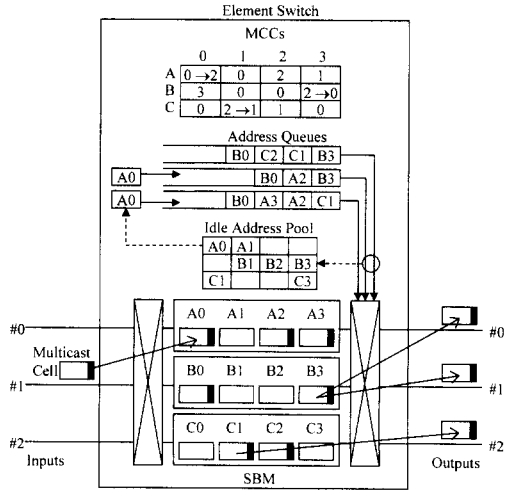


그림 3. 주소 복사 멀티캐스트 방식에서의 멀티캐스트 셀 카운터
Fig. 3. Multicast Cell Counters in address-copy multicast scheme.

In the address-copy multicast scheme, the buffer utilization efficiency is improved because

each multicast cell is stored in only one cell location. However, as the multicast cells are increased, the address data in the output queues is also increased because the addresses of multicast cells are duplicated in the output queues corresponding to the destination ports of the multicast cell. This means that the number of valid cells observed in the output queues is greater than that observed in SBM. Moreover, the address of each multicast cell is ubiquitous among the different output queues because each multicast cell is stored in one cell location and a multicast cell is not released until the cell is sent out to all of its destination ports. Thus, the HOL blocking occurs more frequently when the multicast cells are increased. Although the address-copy multicast scheme achieves the high buffer utilization efficiency, it brings about the degradation of throughput by the HOL effect in multicast environments.

## Ⅲ. Throughput Enhancement in Shared Multi-buffer ATM switch in Multicast Environments

### 1. Multicast architecture

The concept of the Multicast Connection Identifier(MCI) has been proposed to identify each multicast connection in switch fabric.[9] The multicast cells pertained to each MCI has the same destination ports. A multicast queue is provided for each MCI and the multicast queue contains the SBM number and the address data for multicast cells. A write pointer is maintained for each multicast queue and provides the write address for the multicast queue. The value of write pointer is increased whenever a multicast cell of the corresponding MCI arrives. The read pointer supplies the read address for the multicast queue. Because each multicast cell is read separately for each output port, the read pointers are maintained not only for each multicast queue but also for each output port as shown in Figure 4. In Figure 4, the read pointer of MCI#0 indicates that the address data at the address of 16 of the multicast queue should be accessed to read the multicast cell for output port #0 and the address 10 for output port #1 and so on. When a multicast cell is read from SBM and sent out through an output port, the read pointer of the corresponding MCI and output port is increased.

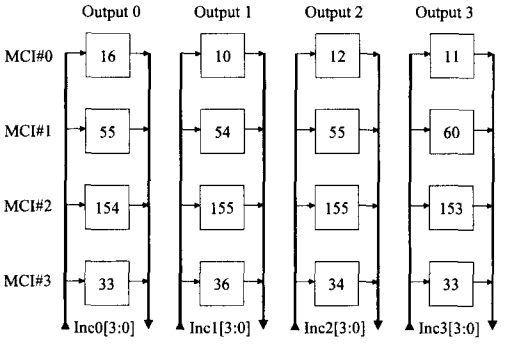


그림 4. 멀티캐스트 연결의 읽기 포인터
Fig. 4. Read pointers of multicast connections.

Before the cells are read from SBMs, the queue-length of MCIs are calculated for each output port. For an MCI, the write pointer and the read pointer for an output port determine the queue-length of the MCI for the output port. The registers containing the destination ports for each MCI are also accessed to determine the queue-length. The queue-length of MCIs can be weighted by external control signal. For each output port, the multicast cell whose queue-length is longest, is selected to be read out for the output port. The HOL blocking occurs when the multicast cells which are selected to be read out for each output port reside in the same SBM. The longest queue method is applied again to the multicast cells and the multicast cell whose queue-length is longest has the first read priority for the SBM.

### 2. Throughput enhancement in Shared Multi-buffer ATM switch in multicast environments

The shared multi-buffer ATM switch provides multiple SBMs and the cells are accessed to shared buffers in parallel. The HOL blocking occurs when cells destined for different output ports reside in the same SBM and are going to be read for their output ports simultaneously. In the prior study, the three-read operation for each SBM shows 98% throughput for a random traffic situation.[5] In this study, it is notable that the throughput improvement obtained in the second read cycle is much less than that obtained in the first read cycle and the throughput improvement is least in the third read cycle. This means that the fewer SBMs are accessed to read cells as the read cycle advances. Figure 5 shows the simulation result, which shows the probability of an SBM not being accessed in the third read cycle. The probability is at least 93% up to 16 x 16 switch size.

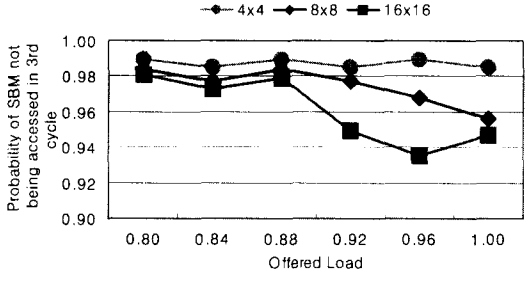


그림 5. 세 번째 읽기 사이클에서 하나의 SBM에서 읽기가 일어나지 않을 확률

Fig. 5. The probability of an SBM not being accessed in the third read cycle.

We use the SBMs to which no access is performed for unicast cells in the third read cycle to read the multicast cells. In the first and the second read cycles, only the unicast cells are read. In the third read cycle, the unicast cells are read from SBMs with higher priority than the multicast cells. The multicast cells are read only in the third read cycle from the SBMs to which no read access is carried out for unicast cells. This scheme guarantees the 98% throughput for the unicast cells in the multicast environments regardless of the multicast traffic because the multicast traffic does not affect the read of unicast cells. Moreover, the utilization rate of the output ports is improved because a multicast cell as well as a unicast cell may reach for each output port. When two cells arrives at an output port, the one with the longer queue-length is sent out through the output port.

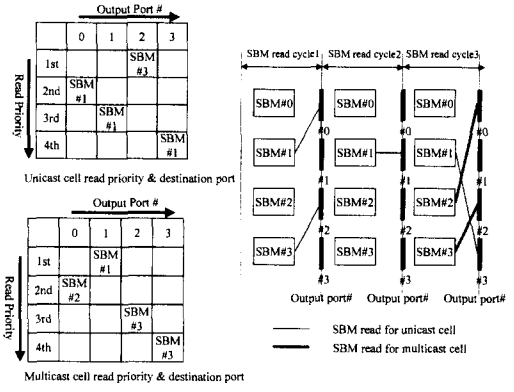


그림 6. 셀 읽기 동작 예

Fig. 6. An example of the cell-read mechanism.

Figure 6 shows an example of the cell-read mechanism. The unicast cells destined for output port #0, #1 and #3 resides in the same SBM and the HOL blocking occurs among the cells. In the first read cycle, the SBM#3 is accessed to read a unicast cell for output port #2, and the cell whose destination port is #0 is read from SBM#1 because the cell has the highest read priority among the cells provoking the HOL blocking. The cell destined for output port #1 is read from SBM#1 in the second read cycle and the cell going to the output port #3 is drawn from SBM#1 in the third read cycle. The multicast cell whose destination port is #1 has the highest read priority among the multicast cells. However, the multicast cell is not read because the SBM#1 is accessed to read a unicast cell in the third read cycle. The multicast cells destined for output port #0 and #2 respectively are read in the third read cycle. A unicast cell and a multicast cell arrive at the output port #0 and #2. At these output ports, the

cell having the longer queue-length is sent out through the output ports. When a multicast cell is sent out through the output ports, the value of the corresponding multicast read pointer is increased.

## Ⅳ. Performance Evaluation

In this section, we evaluate the performance of the proposed shared multi-buffer ATM switch in multicast environments. The performance is compared with that of shared multi-buffer switch employing the address-copy multicast scheme. Throughout the simulation, the switch size is fixed to 8 x 8 and the number of destination ports for each MCI is fixed to 4. The random traffic is assumed for simulations.

### 1. Throughput evaluation

Figure 7 shows the throughput of the proposed ATM switch architecture for various offered load.

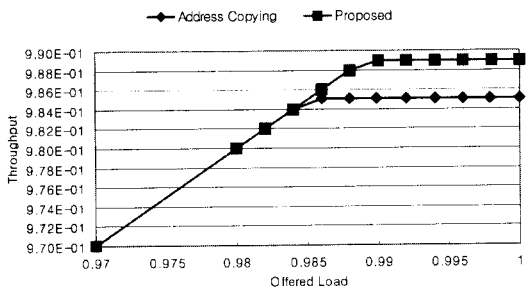


그림 7. 제공 부하에 따른 수율
Fig. 7. Throughput for the offered load.

The number of multicast cell arriving at the switch input is increased as the offered load increases because the arrival rate of the multicast cells is fixed to 10e-3. The proposed switch and the switch adopting the address-copy scheme show the same throughput, which is proportional to the offered load until the offered load reaches 0.985. However, the throughput of the ATM switch employing the address-copy scheme is degraded from that point and saturated. Meanwhile, the proposed architecture shows 98.9% even though the offered load reaches 1. The proposed switch architecture enhances the throughput in the multicast environments because the increase of multicast cells does not aggravate the HOL effect among the unicast cells and the utilization rate of the output ports is increased.

The throughput of the proposed switch architecture for various arrival rate of multicast cells is shown in Figure 8. As shown, the proposed architecture has an improved throughput in multicast environments. In the address-copy multicast scheme, the traffic observed in the output queues becomes much heavier than that observed in the SBMs as more multicast cells arrive. Moreover, the address of each multicast cell is ubiquitous among the different output queues because each multicast cell is stored in one cell location and a multicast cell is not released until the cell is sent out to all of its destination ports. The heavy traffic in the output queues makes more HOL blocking and degrades the throughput.

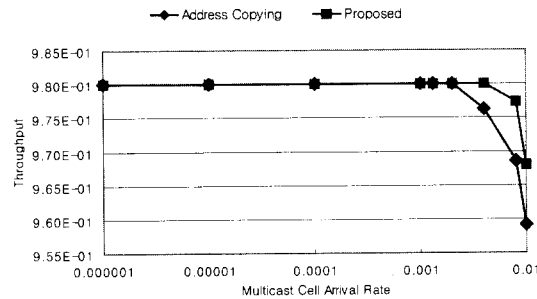


그림 8. 멀티캐스트 셀 도착율에 따른 수율
Fig. 8. Throughput for the arrival rate of multicast cells.

### 2. Evaluation by average queue-length

The average queue-length in the proposed switch architecture for the offered load is shown in Figure 9. As the offered load increases, the queue-length of unicast cells and that of multicast cells grow in the proposed architecture. However, the sum of the queue-length is equal to

or less than the queue-length in the switch employing the address-copy scheme for all conditions.

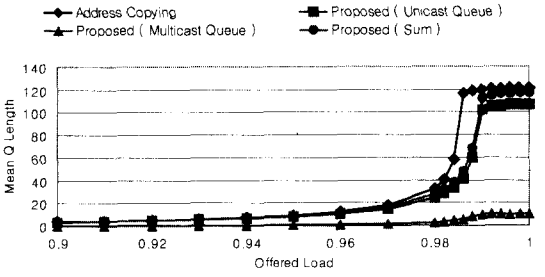


그림 9. 제공 부하에 따른 평균 큐 길이
Fig. 9. Average Queue-Length for the offered load.

Figure 10 shows the average queue-length for the arrival rate of multicast cells. In this simulation, the sum of the queue-length of unicast cells and that of multicast cell in the proposed switch architecture is equal to or less than the queue-length in the switch adopting the address-copy scheme. The queue-length of unicast cell in the proposed architecture is almost constant until the arrival rate of multicast cells reaches 0.1%. This means that the HOL effect among unicast cells is not increased albeit the number of multicast cells increases. However, if the multicast cell arrives more frequently, the queue-length of the unicast cells grows because the queue-length of multicast cells is increased and the multicast cells are more likely to win the unicast cells in the comparison of queue-length at the output ports.

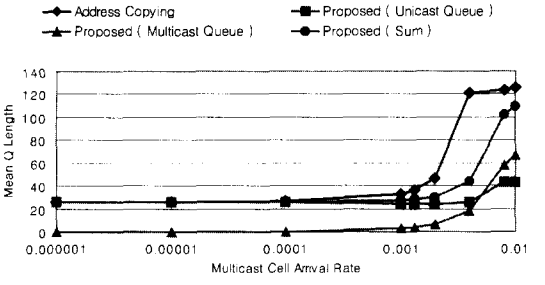


그림 10. 멀티캐스트 셀 도착율에 따른 평균 큐 길이
Fig. 10. Average queue-length for the arrival rate of multicast cells.

## V. VLSI Design

We designed an 8 x 8 shared multi-buffer ATM switch, which has the proposed architecture. The shared multi-buffer ATM switch is described in Verilog-HDL and is synthesized using ASIC synthesizer with standard cell library. The ATM switch is implemented in a two-VLSI chip set. They are a switch chip and a multicast-pointer chip as shown in Figure 11.

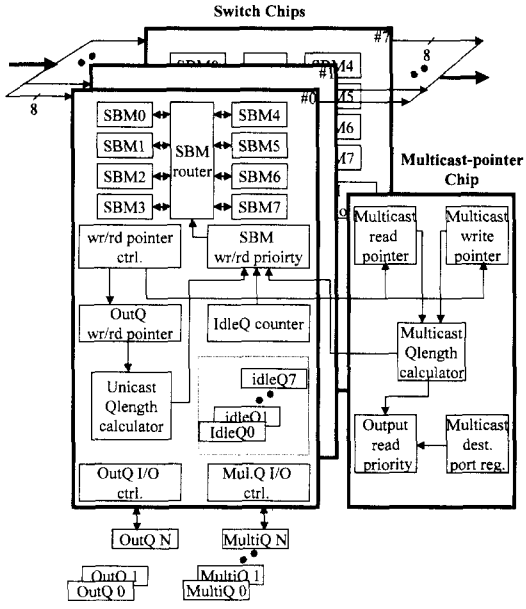


그림 11. 8 x 8 공유 다중 버퍼 ATM 스위치의 칩-셋 구조
Fig. 11. Chip-set architecture of the 8 x 8 shared multi-buffer ATM switch.

### 1. Switch chip

The switch chip includes SBM write priority logic, SBM read priority logic, SBM input/output router, idle queues, SBMs and queue I/O controllers for external output queues and multicast queues. The SBM write priority logic determines the write priority for each SBM. The SBM write priority is calculated with the number of vacant cell spaces in each SBM. The less filled SBM is given a higher write priority to improve the buffer utilization efficiency.

When cells arrive, the number of valid cells is calculated and the SBM input router is configured to route incoming cells to SBMs in accordance with the SBM write priority. An idle address queue is provided for each SBM and supplies the write addresses for each SBM. The SBM number and the write address of each cell are written into external queues. The queue I/O controllers provide the addresses for output queues and multicast queues so that they operate as FIFOs.

To read unicast cells from SBMs, the address data in each output queue is read and the SBM read priority logic determines read priority for the unicast cells. The SBM read priority is calculated with the queue-length of each output queue. In case of multicast cells, the output read priority logic in multicast-pointer chip compares the queue-length of MCIs for each output port and the multicast cells which have the longest queue-length are selected for the output ports. The address data for the multicast cells is read from the corresponding multicast queue. Then, the SBM read priority logic calculates the read priority of each multicast cell with the queue-length of each multicast queue. The multicast cell whose queue-length is longer gets higher read priority.

The three-read operation is performed for each SBM. During the first two read cycles, only the unicast cells are read. When two or more unicast cells resides in the same SBM, the SBM read priority is used to determine the order of read for the SBM. The multicast cells are read only in the third read cycle. When HOL blocking occurs between unicast cells and multicast cells in the third read cycle, the unicast cells have the higher priority. However, when HOL blocking occurs among the multicast cells, the SBM read priority for multicast cells determines the order of read for the SBM. When the outgoing cells are determined for output ports, the read pointers of the corresponding unicast queues and multicast queues are increased. The addresses of cell spaces where the outgoing cells were stored, are written to the corresponding idle queues.

Each SBM is implemented as asynchronous SRAM and is designed to have 16-bit common input/output bus. A 16-bit serial-to-parallel converter is located between the SBM input router and SBMs to convert the 8-bit input data. The size of each SBM is 8-kbit so that eight switch chips can store 1,024 cells, which corresponds to 128 cells per port. Idle queues are also implemented as asynchronous SRAMs.

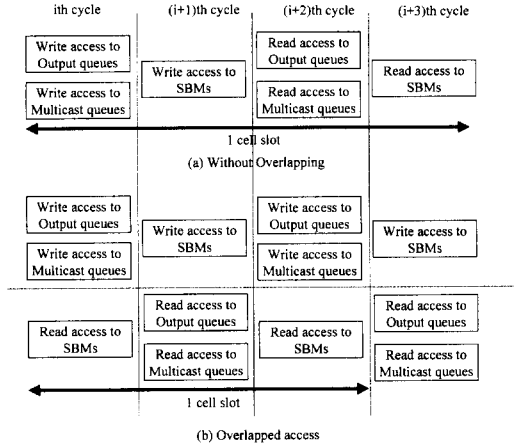


그림 12. 중첩된 메모리 엑세스
Fig. 12. Overlapped memory access.

The access to output queue and multicast queue occurs simultaneously and it is overlapped with the access to SBMs as shown in Figure 12. The switch chip accommodates higher source rate owing to the overlapped memory access.

The switch chip is laid out in a 0.6um CMOS triple metal single poly process. The layout of the switch ship is shown in Figure 13. The size of switch chip is 12.98mm x 13.85mm and contains 479,334 transistors excluding SRAMs. The maximum operating frequency is 20Mhz, which supports 155.52Mbps STM-1 source rate per port. The critical path lies between the read access to multicast queues and the increase of read pointers of the multicast queues. Table 1

summarizes the characteristics of the switch chip.

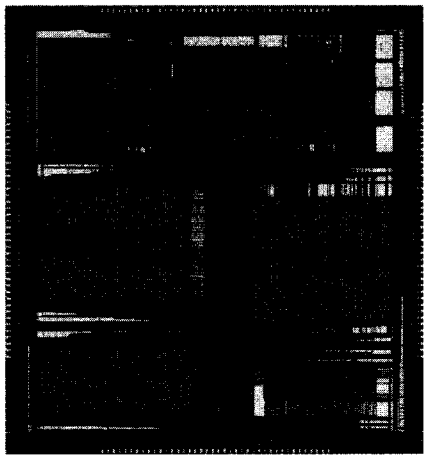

그림 13. 스위치 칩의 레이아웃
Fig. 13. The layout of switch chip

표 1. 스위치 칩의 특성
Table 1. Characteristics of the switch chip.

| | |
|---|---|
| Process Technology | 0.6um 3-metal 1-poly CMOS |
| Chip Size | 12.98 mm X 13.85mm |
| Transistors | 479,334 |
| Operating Frequency | 20Mhz |

2. Multicast-pointer chip

The multicast-pointer chip includes the multicast write pointers, the multicast read pointers, multicast destination registers and output read priority logic. Each multicast connection has a unique MCI and has a multicast queue. A multicast write pointer is maintained for each multicast queue and the multicast write pointer is increased whenever a multicast cell of the corresponding MCI arrives at the switch fabric. The multicast read pointers are provided for each output port as well as for each multicast queue. The multicast destination registers contains the destination ports of each MCI in the switch fabric. The queue-length of each MCI for an output port is calculated with the write pointer and the read pointer for the output port. The queue-length of MCIs can be weighted by external control signal. For each output port, only the MCIs with a destination for the output port are qualified to be compared the queue-length for the output port. The output read priority logic compares the queue-length of MCIs for each output port and the multicast cells which have the longest queue-length are selected for the output ports. Figure 14 shows the path along which the multicast cells are selected for each output port and are prioritized in the SBM read prioirty logic. The comparator and the carry save adder(CSA) encode the result of queue-length comparison and the decoder gives the priority to each multicast cell.

The multicast pointer chip contains 402,240 transistors.

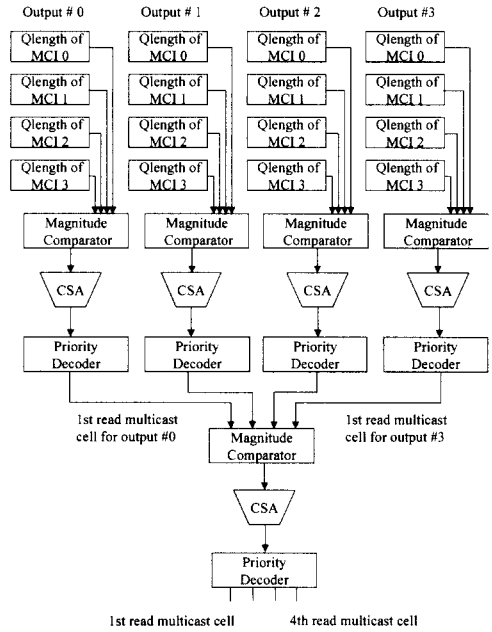


그림 14. 출력 포트에 대한 멀티캐스트 셀 선택과 우선 순위 부여
Fig. 14. Selecting the multicast cells for the output ports and prioritizing.

## VI. Conclusion

We proposed a multicast scheme in which the queues for multicast cells are separated from those for unicast cells and the multicast cells are

read separately for each output port. The multicast cells are read from the SBMs to which no read access is performed for unicast cells in the third read cycle so that the HOL blocking among the unicast cells is not augmented by the multicast traffic in the multicast environments. Simulation is performed to evaluate the performance of the proposed switch architecture. Two parameters - throughput and average queue-length - are used for performance evaluation. The performance of the proposed switch is compared with that of the switch adopting the address-copy multicast scheme. The proposed ATM switch architecture shows improved throughput in multicast environments compared with that of the ATM switch employing the address-copy multicast scheme. The proposed ATM switch shows 98.9% throughput even though the offered load reaches 1. In multicast environments, the average queue-length of the proposed switch architecture is also reduced.

We designed an 8 x 8 shared multi-buffer ATM switch, which has the proposed architecture, in a two chip set. The switch chip is laid out in 0.6um CMOS single poly triple metal standard cell library. The operating frequency of the switch chip is 20Mhz, which supports 155.52Mbps STM-1 source rate per port.

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