무선가입자망용 CMOS 중간주파수처리 집적회로

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A CMOS Intermediate-Frequency Transceiver IC for Wireless Local Loop

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요 약

본 논문에서는 10-MHz 대역폭을 갖는 무선가입자망용 중간주파수 아날로그 IC 설계에 관하여 논한다. 본 IC는 RF 부와 MODEM사이에서 인터페이스 역할을 하며, 수신 단에서는 중간주파수 신호를 기저대역으로 저역변환을 하고 송신 단에서는 기저대역 신호를 중간주파수 신호로 바꾸어 준다. 본 회로는 이득조절증폭기, 위상잠금회로, 저역통과필터, 아날로그-디지털 및 디지털-아날로그 변환기로 구성된다. 위상잠금회로에서 전압발진기 및 분주기, 위상비교기, 전하펌핑회로는 동일 칩 안에 구현하였고, 외부소자로는 루프필터용 소자와 LC 탱크 소자만이 사용되었다. 본 IC는 0.6-μm CMOS 공정에 의하여 제작되었고, 전체 크기는 4 mm x 4 mm 이며, 3.3 V에서 약 57 mA를 소모하였다.

ABSTRACT

This paper describes a CMOS IF transceiver IC for 10-MHz bandwidth wireless local loops. It interfaces between the RF section and the digital MODEM section and performs the IF-to-baseband (Rx) and baseband-to-IF (Tx) frequency conversions. The chip incorporates variable gain amplifiers, phase-locked loops, low pass filters, analog-to-digital and digital-to-analog converters. It has been implemented in a 0.6-μm 2-poly 3-metal CMOS process. The phase-locked loops include voltage-controlled oscillators, dividers, phase detectors, and charge pumps on chip. The only external components are the loop filter and the varactor-tuned LC tank circuit. The chip size is 4 mm x 4 mm and the total supply current is about 57 mA at 3.3 V.

I. 서 론

Wireless local loop (WLL) is a system for connecting the subscribers to the public switched telephone network by using radio signals as a substitute for the copper connection between the subscriber and the switch. Since the WLL system uses digital radio signals to provide the final link from the telephone network to the subscriber, the cost of connection is dramatically reduced. For the WLL system, FDMA, TDMA, or CDMA can be used as an access method. However, since the CDMA allows the widened spectra of many users to fall in the same frequency band and thus can potentially achieve a higher capacity than the other two, Korea have adopted a wide-CDMA method as an Interim Standard for WLL system summarized in Table I [1].

Typically, there are many standard architectures for the IF design: single IF conversion, dual IF conversion, and triple IF conversion. Normally, the dual and triple IF conversions use less

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expensive filters but require the second and third mixers, local oscillators, and additional IF amplifiers. Meanwhile, the single IF conversion requires high quality filters, but reduces the number of local oscillators, mixers, and amplifiers.

Table I. Korean Interim Standard for 10-MHz Bandwidth WLL System

Parameter	Specification
Connection Method	Wide-CDMA
Frequency Band (Reverse Link)	Tx : 2.30-2.31 GHz
	Rx : 2.37-2.38 GHz
Channel Bandwidth	10 Mcps
PN Code Chip Rate	8.192 Mcps
Vocoder	64K PCM, 32K ADPCM
N-ISDN	144 Kbps (2B+D)

Therefore, in order to minimize the power consumption and the chip size, the single IF approach was chosen here as shown in Fig. 1.

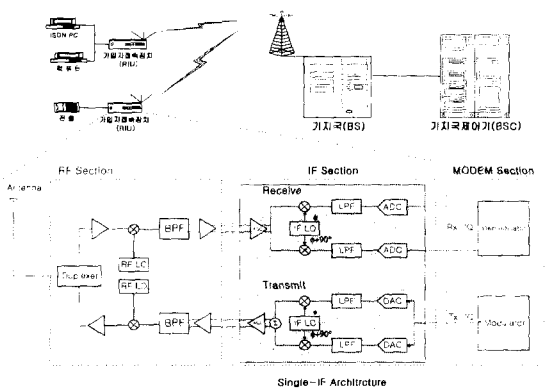


Fig. 1 WLL system.

To briefly describe the WLL system, the signal received from the antenna is amplified and then converted to the IF frequency range by the RF mixer. After IF filtering, this signal is input to the IF section. This IF signal is fed to the quadrature demodulator and converted to I (in-phase) and Q (quadrature-phase) baseband signals. Subsequently, the I and Q signals are filtered to reject the unwanted frequency components and converted into digital signals. These digital signals are sent to the MODEM section for data reconstruction.

Similarly, I and Q baseband digital data from the MODEM section are converted into analog signals. After low pass filtering, these analog signals are fed to the quadrature modulator and converted to the IF frequency range. The modulated IF signal is filtered using an external SAW filter prior to the RF section. Finally, this IF signal is up-converted to the RF frequency range by the RF mixer and then sent the antenna.

In this paper, we describe an IF transceiver integrated circuit for the Korean WLL system. This chip interfaces between the RF section and digital MODEM section.

Ⅱ. Integrated IF Transceiver

Fig. 2 shows the block diagram of an IF transceiver integrated circuit for 10-MHz bandwidth WLL system. It incorporates variable gain amplifier (VGA), phase-locked loops (PLL), low pass filters (LPF), analog-to-digital converters (ADC), digital-to-analog converters (DAC), and other power control circuits. The PLL's include voltage-controlled oscillators (VCO) and all frequency synthesizing logic circuits on chip. The only external components are the loop filter and varactor-tuned *LC* tank circuit.

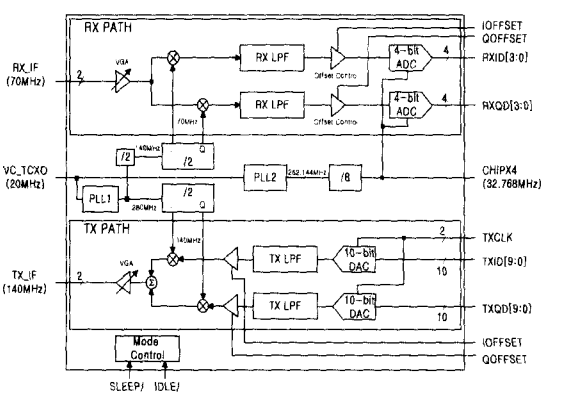


Fig. 2 IF transceiver block diagram.

A. Receive Path

The Rx path receives a differential IF signal

with CDMA spread spectrum modulation extending ±4.096 MHz from a center frequency of 70 MHz.

This input signal is divided into I and Q baseband signals by mixing with 70-MHz local oscillator (LO) signals. These I and Q LO signals are generated by the master-slave divide-by-2 circuit and fed to the I and Q mixers. The mixers are preceeded by ±45-dB variable gain amplifier to obtain a sufficient gain and to reduce the effect of high noise figure in the mixer. A double-balanced mixer architecture was chosen to reduce the second-order and higher even-order harmonic components of the mixer. Then, the I and Q baseband signals are input to the Rx LPF's, respectively, prior to A/D conversion. The performance of the overall WLL system is dominated by these LPF's, in conjunction with an external SAW (surface acoustic wave) filter. It is well known that the *LC* ladder filter has the smallest sensitivity to element values and the active filter built from it also have good characteristics. In our design, the seventh-order elliptic *Gm-C* filter is realized from the *LC* ladder filter using the signal flow graph method [2]. It also has a switched-capacitor tuning circuit to compensate for the variation of frequency characteristics due to process, temperature, and power supply variations [3]. The tuning circuit maintains a constant *Gm/C* ratio value using feedback. Fig. 3 shows the schematic diagram of the seventh- order elliptic *Gm-C* low pass filter (LPF). The passband frequency of the LPF is 3.92MHz and stopband attenuation should be at least −40 dB at 4.94 MHz.

The two identical 4-bit flash ADC's convert the outputs of the LPF's into digital signals. Then, the outputs of the ADC's are provided to the MODEM section at each rising edge of the ADC clock signal CHIPx4. This 32.768-MHz CHIPx4 signal is generated from the PLL2.

The name CHIPx4 means that the ADC clock frequency is exactly four times of the PN code rate of 8.192 Mcps for the Korean 10-MHz WLL system.

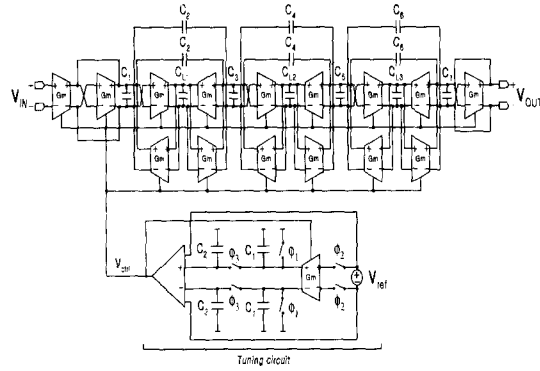


Fig. 3 Receiver LPF with switched-capacitor tuning scheme.

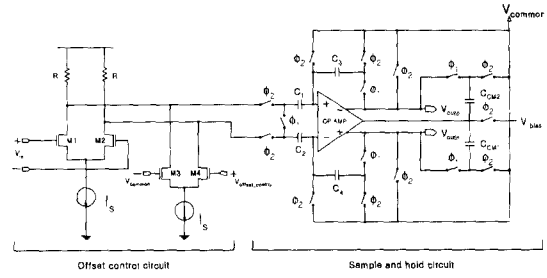


Fig. 4 Sample-and-hold circuit with offset control in ADC.

On the other hand, the offset at the inputs of the ADC's is critical to the performance of the whole WLL system. Typically, in CMOS processes, the DC offset voltage due to the threshold voltage mismatch, the geometry mismatch, and the oxide thickness mismatch is known to be about 5-20 mV. Thus, the offset voltage at the input stages of the ADC's should be eliminated by the I and Q offset control signals provided from the MODEM section [5]. Fig. 4 shows the sample-and-hold circuit of the ADC with the offset control circuit.

B. Transmit Path

The Tx path receives digital I and Q baseband data from the MODEM section and provides a modulated IF output centered at 140 MHz to the RF section. The 10-bit I and Q digital signals are input to the two identical DAC's at the rising edge of the clock signal TXCLK from the MODEM. Fig. 5 shows the current cell structure

of the DAC. As well known, the lower 5-bit current sources (*I*, 2*I*, 4*I*, 8*I* and 16*I*) are designed by size ratio, while the upper 5-bit current sources are decoded after duplicating the current source 32*I*. Here, *I* denotes a unit current source. Each DAC is followed by the LPF to remove the unwanted clock frequency components of the DAC output. The specifications of the Tx LPF are modest and thus implemented by the fourth-order *Gm-C* elliptic filter. Although the DC offset problem of the Tx path is not severe since the gain of the whole Tx path is low, compared to the Rx path, the offset trimming circuits are added. The trimming circuits have external pins and thus the DC offset voltage is adjusted by external variable resistors. Note that in the Rx path, the DC offset voltage is controlled by the digital MODEM, but in the Tx path, the digital MODEM cannot control the DC offset voltage since there is no way to detect the DC offset voltage. Thus, the DC offset voltage in the Tx path is not controlled but trimmed. The output of the Tx LPF's are then converted up to the 140-MHz IF signal by the Tx LO signals, After mixing, these I and Q IF signals are summed and sent to the RF section through the ±45-dB VGA.

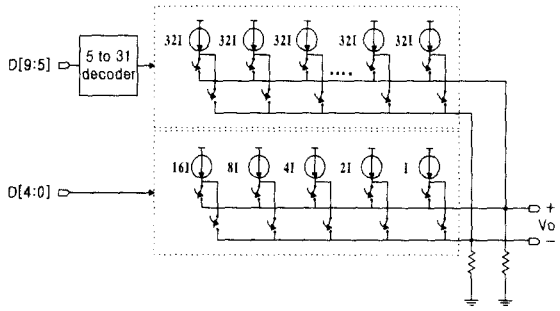


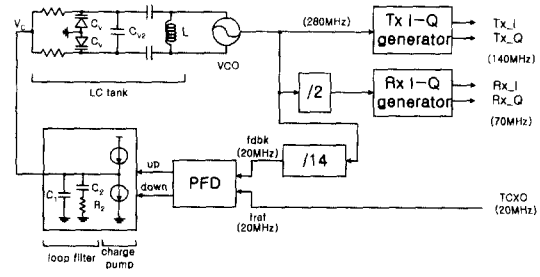
Fig. 5 DAC current cell structure.

C. Frequency Synthesizer

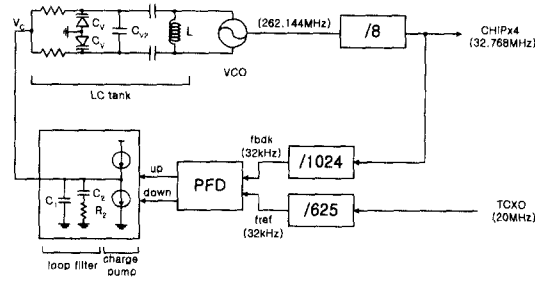
In our design, two separated PLL's are required. One is to generate the Rx and Tx LO signals and the other is to generate the ADC sampling clock CHIPx4.

The PLL1 generates the I and Q LO signals for the Rx and Tx mixers, that is, 70 MHz for the Rx mixer and 140 MHz for the Tx mixers, respectively. The Rx LO signals can simply be generated by a divider-by-2 circuit from the Tx LO signals. In the Korean WLL Interim Standard, the difference between the Rx and Tx IF is exactly 70 MHz. Normally, there are many choices in determining the Rx and Tx IF values. When the Rx and Tx IF are the integer multiples of the Rx and Tx IF difference, the Rx and Tx LO signals can simply be generated from a single PLL as shown in Fig. 6(a). In other choices, an additional PLL may be required or the dividers becomes very complicated.

On the other hand, the CHIPx4 signal that is used as the clock of the ADC's cannot be generated directly from the PLL1 and thus the PLL2 shown in Fig. 6(b) is used to generate the CHIPx4 signal.



(a) PLL1



(b) PLL2

Fig. 6 Frequency Synthesizer. (a) PLL1 and (b) PLL2.

Each PLL incorporates a VCO, dividers, a phase detector, and a charge pumping circuit on chip. Only external requirements are varactor-tuned *LC* tank components for tuning the frequen-

cy of the VCO, and standard passive components for the PLL loop filter. A 20-MHz temperature compensated crystal oscillator is in common used as a frequency reference.

Ⅲ. Experimental Results

The IF transceiver integrated circuit has been implemented in a 0.6-μm 2-poly 3-metal CMOS process and assembled in 100-pin plastic quad flat packages. The two PLL's are located at the left coner to reduce the interference with other circuits and the signal path is made to progress around the periphery of the chip. The VCO has an internal bandgap reference circuit to reduce the supply voltage or temperature variation effects. Also, another bandgap reference is used to offer the constant bias to each circuit. The chip area is 4 mm x 4 mm. The total supply current for the Rx and Tx paths is about 57 mA at 3.3 V. Fig. 7 shows the layout of the fabricated chip.

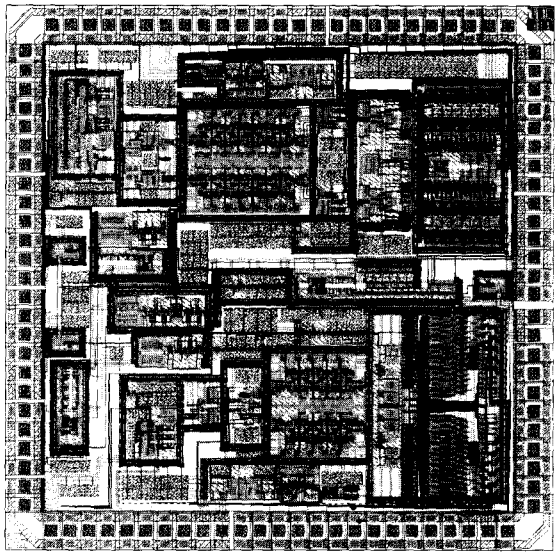


Fig. 7 Layout of the fabricated chip.

Fig. 8 shows the measured frequency characteristics of the seventh-order elliptic *Gm-C* Rx LPF. The passband frequency is about 3.904 MHz and the stopband attenuation is $\leq$ -45 dB. Also, the passband ripple is $\leq \pm$1.2 dB. Since the Rx

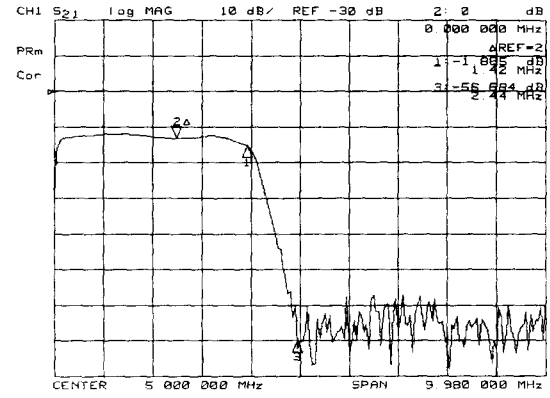
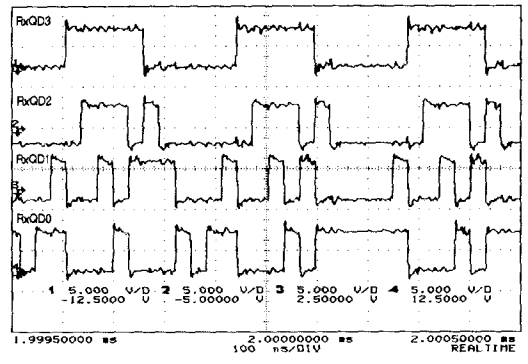
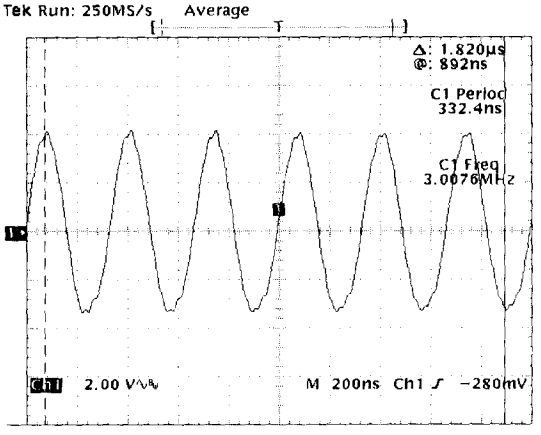


Fig. 8 Measured Rx LPF characteristics.

LPF has sharp attenuation characteristics, a large group delay difference over transition frequencies is caused. This group delay difference is very critical in data processing and thus must be equalized. Normally, the equalization is performed in the base station, *i.e.*, the second-order or third-order all pass filter that has the frequency characteristics corresponding to the approximate inverse function of overall phase characteristics in the Rx path is inserted prior to the quadrature modulator in the base station. To demonstrate the ADC operation, a sinusoidal input of 73 MHz (that is, equivalent of 3-MHz sinusoidal baseband signal with a carrier frequency of 70 MHz) is applied to the input of the Rx path. The final 4-bit digital output data of the Rx ADC is shown in Fig. 9(a). To examine the frequency of the baseband digital output, the ADC output was again converted to an analog signal by an external DAC (Fig. 9 (b)). The measured frequency is 3.0076MHz (The exact value is 3.0 MHz). To demonstrate operation of the PLL1, the spectrum of the Rx LO signal (70 MHz) has been measured. Since the Rx VCO has no internal buffered output, its spectrum is measured indirectly. The spectrum of the VCO has been measured from the output of the mixer, that is, using the feedthrough from the LO signal to the baseband signal (Fig. 10). The measured phase noise is -81 dBc/Hz at 1 KHz offset and -104 dBc/Hz at 10 KHz offset, respectively. Also, since the Tx and Rx LO sig-



(a)



(b)

Fig. 9 Measured ADC characteristics.
(a) 4-bit ADC output (b) Its D/A conversion.

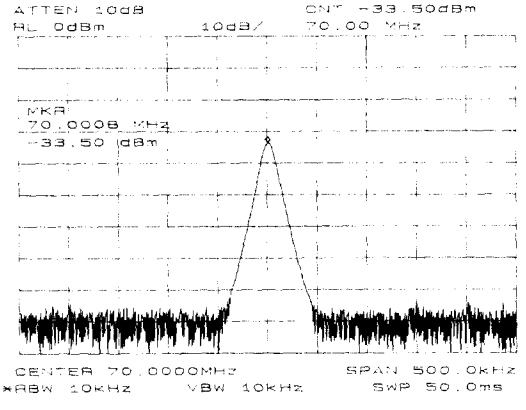


Fig. 10 Measured spectrum of Rx LO signal (PLL1).

nals are generated from the same VCO as shown in Fig. 6(a), we can presume that the Tx LO signal also has almost the samefrequency spectrum. To demonstrate the single sideband modulation of the Tx path, 1-MHz digital cosine and sine signals are input to the I and Q DAC, respectively. Fig. 11 shows the output spectrum with single sideband modulation of the transmitter. The output is −26.81 dBm into 200-Ω load. The carrier component and unwanted sideband component are −32 dB and −37 dB, respectively, below the wanted signal.

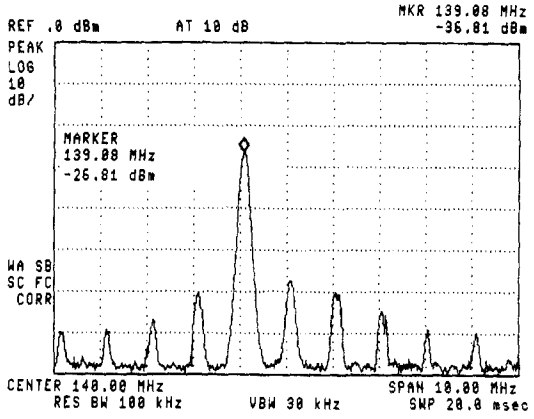


Fig. 11 Measured output spectrum of Tx path.

Ⅳ. Conclusions

An IF transceiver IC for 10-MHz WLL system has been described. It has been implemented in a 0.6-um CMOS process. All circuits have operated well a s expected. The chip size 4 mm x 4 mm and the total supply current is about 57 mA at 3.3 V.

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