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0.7 inch FED Panel system build-up by using proper sealing process

Sang Jik Kwon, Kun Jo Hong, Tae Hee Cho, Jong Duk Lee*, Chang Woo Oh* and Yong Bum Kwon**

Dept. of Electronics Eng., Kyungwon Univ, Bokjung-Dong, Soojung-Gu, Seongnam-City, Kyunggi-Do 461-701
**School of Electrical Eng., Seoul Nat'l Univ., San 56-1, Shinlim-Dong, Gwanak-Gu, Seoul 151-792*
***Sinheung Hi-Tech., LTD, 39-11, Paho-Dong, Daiseo-Ku, Daegu 704-220*
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Abstract – FED panel was successfully fabricated through the integration of a 0.7" diagonal Si-based Mo-tip FEA with 25×25 pixels, Y_2O_3:Eu or ZnO:Zn phosphor screen, and vacuum sealing through an exhausting glass tube, including a getter. The panel system was driven by an external driver circuit having pulse width modulation(PWM) driving scheme. Before character imaging, it was stabilized through tip aging by slowly increasing a pulse-mode emission current and phosphor aging by a coulombic charging process. After aging, luminescent characteristics such as emission uniformity, charging and arcing phenomena were shown to be improved significantly.

I. Introduction

Field emission display has drawn a strong attention by many researchers owing to its fundamental advantages such as high brightness, high resolution, large viewing angle, low power consumption, and low fabrication costs, even with window-pane flat panel shape [1]. However, in order to commercialize FED system, more extensive achievements in the following four areas should be done in areas of : (1) field emitter array, (2) low voltage color phosphors, (3) high vacuum sealing and (4) high voltage driver circuit. Some critical issues [2-4] have been resolved in our previous studies. However, the performance of whole panel system was not reported. In this study, we have fabricated the whole panel system of 0.7 inch diagonal FED and investigated aging effect on the luminescent characteristics including an emission current uniformity.

II. Fed Panel System Build-up

The fabricated panel structure includes a cathode electrode which has Mo-tip field emitter array based on Si substrate, and an anode phosphor screen which is coated on a soda-lime glass plate with indium thin oxide (ITO) film. Two electrodes are merged into a vacuum sealed glass panel with a getter loaded on an exhausting glass tube, as shown in Fig. 1.

2.1. Field Emitter Array

Field emitter array(FEA) consists of 25×25 pixels with 0.7 inch diagonal size. The pixel contains 25×25 Mo-tips fabricated on Si substrate. The crossing areas between Mo-metal gate lines (column or data lines) and n-well cathode line(row or scan lines) create pixels of which size are 300 mm×300 mm. Pixel pitch is 500 mm, which allows the spacing of 200 mm between lines. The p^+ channel stop lines are inserted between n-well cathode lines which prevent the creation of parasitic n-MOS channels when a corresponding metal gate line is biased with a given data pulse. If the parasitic channels occur, all cathode lines under the biased gate line would be selected, as a result, a line by line addressing will not be implemented. The key process in our FEA structure is the gate-hole size reduction by local oxidation (LOCOS) commonly used in conventional MOS device processing. The LOCOS process also produces a very good quality of oxide as a gate insulator in FEA structure. Through the reduced gate holes, Mo-tips are formed by using conventional spindt-type process. The well-defined large volume of the space around tip, which is resulted from the bird's beak shape by the

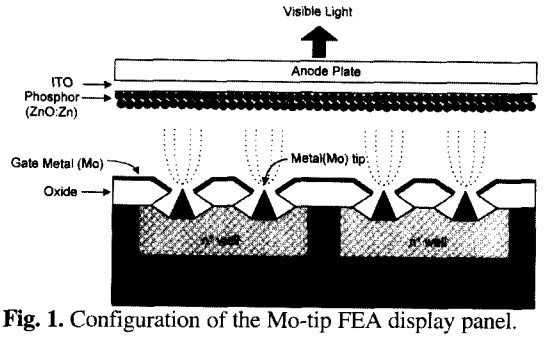
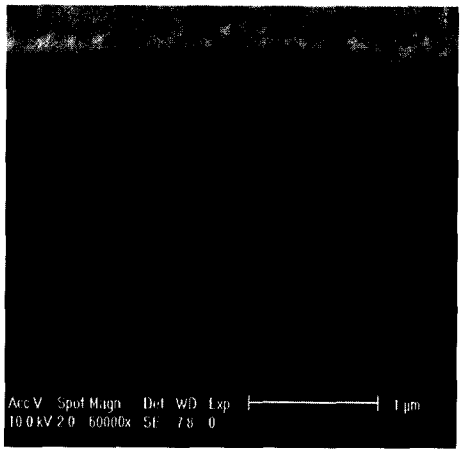
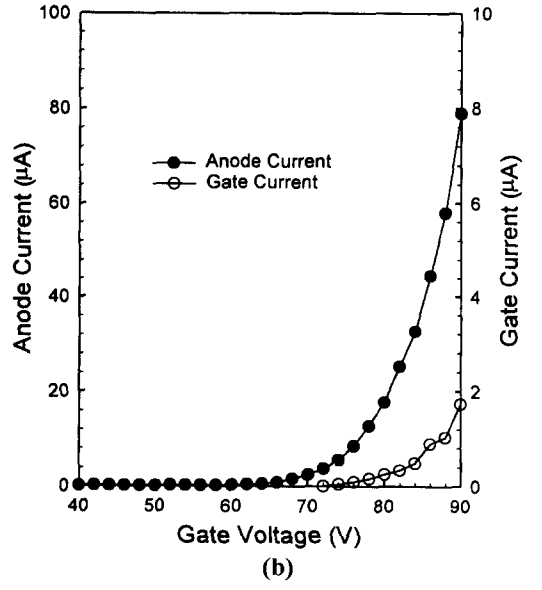


Fig. 1. Configuration of the Mo-tip FEA display panel.



(a)



(b)

Fig. 2. (a) Cross sectional view of a fabricated emitter tip and (b) field emission characteristics for one pixel of the tips.

LOCOS process, can make the leakage current between emitter and gate very low and the parasitic gate-to-cathode capacitances small. More detailed process sequences are well described in our previous paper [2]. The cross-sectional view of the completed field emitter structure is shown in Fig. 2(a), and the resultant emission characteristics in Fig. 2(b). The emission currents were measured in a test chamber with a vacuum level of 1.0×10^{-8} torr. In the emission characteristics, turn-on voltage was shown to be 52 V with an emission current of 10 nA/tip at 75 V. And also, the gate leakage current was less than 2 percent of the anode current.

2.2. Color Phosphor Synthesis and Screening

In order to obtain enough luminescence of the phosphor screen even at very low anode voltage around 300 V, we have used the phosphor powders synthesized by using aerosol pyrolysis [3]. Y_2O_3 : Eu, $ZnGa_2O_4$: Mn and Y_2SiO_5 : Ce are synthesized respectively for red, green and blue phosphors. In our panel system, the Y_2O_3 : Eu red phosphor was applied to the anode glass plate by using electrophoretic deposition method. In the electrostatic deposition process for a screening, the synthesized powders are diluted in the IPA (Iso Prophyl Alcohol) and Mg $(NO_3)_2$ mixtures. For comparison, commercialized ZnO : Zn powders are also used for mono-blue screening. The resultant cathode luminescent characteristics are shown in Fig. 3.

2.3. Vacuum Sealing

For a successfully operating FED system, all components composing a panel such as FEA, phos-

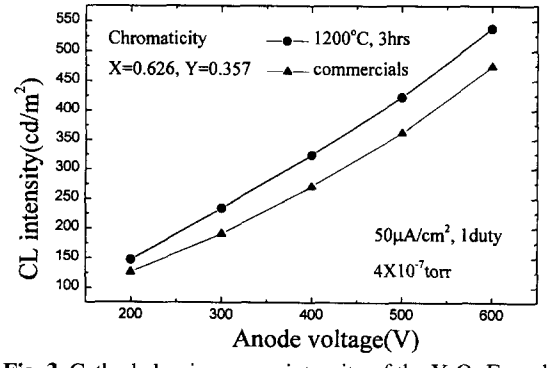
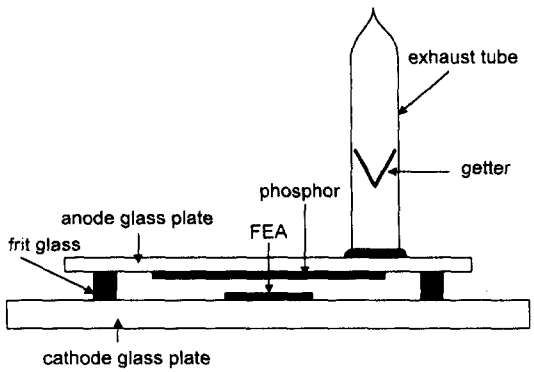
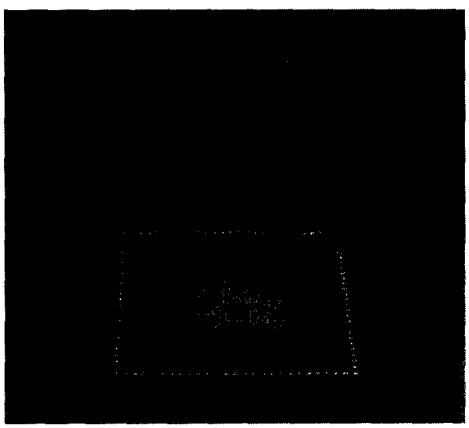


Fig. 3. Cathode luminescence intensity of the Y_2O_3:Eu red phosphor as a function of anode voltage.



(a)



(b)

Fig. 4. (a) Schematic diagram of a packaged FED panel and (b) picture of the completed panel.

phor screen and getter should be merged into a high vacuum glass enclosure as shown in Fig. 4(a). We have adapted a soldering method using a frit glass paste for the glass sealing. High vacuum was obtained by pumping through an exhausting glass tube under baking [4]. During the vacuum sealing process, FED panel suffers several high temperature cycle which would result in some problems such as outgassing of absorbed contaminants, vaporization of some contents from several components, oxidation of Mo-tip or gate material and glass breakage, etc. we have successfully sealed all components including the activation of getter and evaluated the real vacuum level inside the FED panel, by using ECCM (Emission Current Calibration Method) which is considered as most accurate method tried until now for the vacuum measurement inside panel [4]. Finalized FED panel picture is shown in Fig. 4(b). The real vacuum level inside the panel was evaluated as 1×10^{-6} torr before seal-off, 1.1×10^{-5} torr right after seal-off, and then, improved to 3×10^{-6} torr after getter activation.

III. Luminescent Characterization of the Completed Panel

During the sealing process, under baking around 200 for 10 hours, almost all absorbed contaminants including H_2O will be outgassed through the exhaust. However, some particles stuck to the emitters or protruding morphology of the tips will be still remained. In order to remove such particles or contaminants, tip aging and phosphor aging were performed before tip-off under pumping through the exhaust. Tip aging is done during the field emitting process by increasing a pulse-mode driven voltage up to $80V_{p\text{-}p}$ starting from $60V_{p\text{-}p}$ with $5V_{p\text{-}p}$ step every 20 min. After tip aging, average emission current level was decreased, while uniformity in the emission current levels for all pixels was improved. Phosphor aging is done during a coulombic charging by an emission current of 50 mA/cm^2 exerted on the screen. During phosphor aging, luminescence was decreased consistently and then began to be saturated after around 10 mins. The saturated luminescence value was less than half of the initial value before aging. In our sealing procedure, above two aging modes were performed simultaneously. Fig. 5(a) and (b) show the light emitting patterns including the emission current distributions all over 0.7 inch panel before and after the aging process, respectively. As shown, the uniformity of the light emission and the current emission were improved by the aging process. The emission current distribution was obtained from the selected 6×6 pixels over 0.7 inch panel. As shown, before aging, the average current level was shown to be 1.62 mA with a standard deviation of 1.06 mA. While, after aging, it was 0.18 mA with a standard deviation of 0.09 mA. From the distribution data, we can see that the excessive current levels of a few pixels were alleviated. In contrast, the much less current levels from some others were improved. We have also observed several luminescent characteristics such as arcing and charging phenomena which will be issued in the

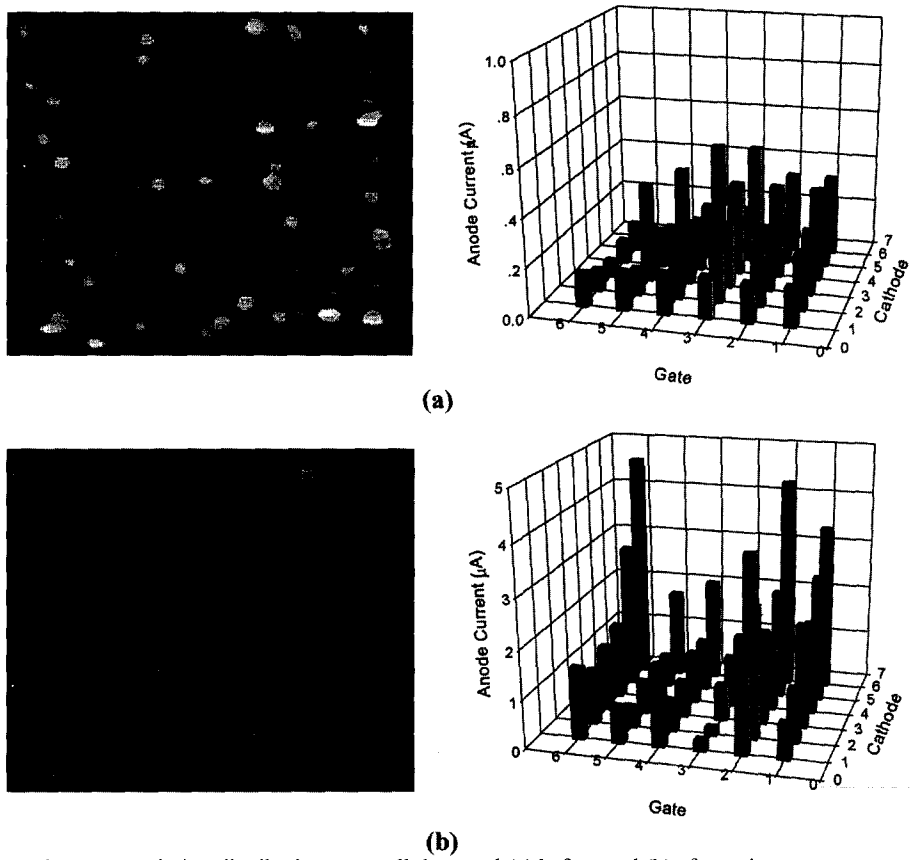


Fig. 5. Light and current emission distributions over all the panel (a) before and (b) after aging process.

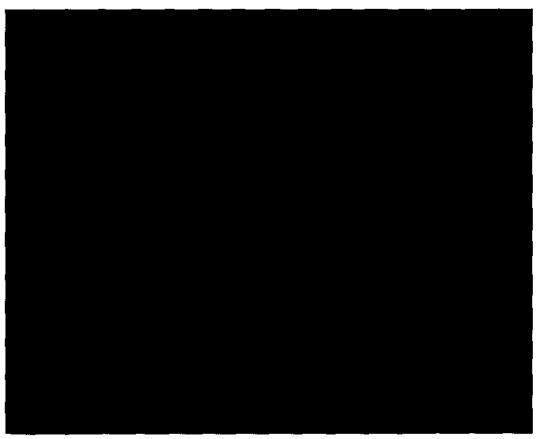


Fig. 6. Character image displaying of the addressed FED panel.

presentation more details. Character images will be successfully displayed by a driver circuit using PWM driving scheme as shown in Fig. 6

IV. Conclusions

During the sealing of 0.7 inch diagonal Mo-FEA, aging process steps were incorporated for a stabilization of a spatial emission current distribution and cathodoluminescence of the phosphor screen. After aging by increasing the emission current up to 50 mA/cm^2 for 2 hours, the emission current uniformity was so improved from 1.06 mA standard deviation down to 0.76 mA. And also, light emission uniformity was improved. In addition, some irregular problems such as charging and arcing phenomena were alleviated.

Acknowledgment

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