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Design of MOSFET-Controlled FED integrated with driver circuits

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Abstract – In this paper, the design of one-chip FED system integrated with driving circuits is reported on the basis of MOSFET controlled FEA (MCFEA). To integrate a MOSFET with a FEA efficiently, a new fabrication process is proposed. It is confirmed that the MOSFET with threshold voltage of about 2 volts controls the FEA emission current up to 20 μA by applying driving voltage of 15 volts, which is enough current level to utilize the MCFEA as a pixel for FED. The drain breakdown voltage of the MOSFET is measured to be 70 volts, which is also high enough for 60 volt operation of FED. The circuits for row and column driver are designed stressing on saving area, reducing malfunction probability and consuming low power to maximize the merit of on-chip driving circuits. Dynamic logic concept and bootstrap capacitors are used to meet these requirements. By integrating the driving circuit with FEA, the number of external I/O lines can be less than 20, irrespectively of the number of pixels.

I. Introduction

A field emission display (FED) can be a thin light-weighted flat panel display like LCD maintaining the merits of CRT such as wide viewing angle, bright image, and stable operation under severe environment conditions, and it consumes much lower power than PDP in principle. Consequently, it has been a powerful candidate expected to replace the old style displays for all-sized applications.

A small-sized and high-resolution display with low power consumption required for head-mounted-displays (HMDs) or electronic view finders of video camera systems can be a breaking through application which can utilize all the merits of FED. For the small-sized high-resolution display with simple matrix driving type, the driving signal lines are too dense to connect them to driver circuits easily. Therefore, it is essentially required to integrate the driving circuits into the display panel.

For the smaller displays than 4 inches, it can be made on single-crystal silicon wafer and driver circuits can be integrated using the transistors with good performance. Moreover, the developed semiconductor fabrication technology can be applicable to minimize the pixel size and to attain uniformity over the whole area of the display. Actually, 0.5 to 1.0 inch diagonal would be enough size for HMDs or view finders [1], and the conventional lithography process using contact aligner, projection printer, and stepper can be used for this size. Low-cost mass production of small-size high-resolution displays is possible since the field emitter fabrication process is compatible with the semiconductor IC process.

The purpose of this paper is to investigate some design considerations for one-chip FED system integrated with MCFEAs and driving circuits on a single substrate.

II. Design of MCFEA Pixels

The first thing to be considered is the adequate pixel structure for one-chip FED. Most of recently developed field emitters require high driving voltage about 50~100 V and on-chip driving circuit must be capable of driving at that high voltage. The high voltage MOSFET (HVMOSFET) like LDMOS (lateral double-diffused MOS) can be used, but the processing sequence becomes too complicated to fabricate it together with field emitters. Many researchers have tried to reduce the driving voltage of FEA by using low work function materials such as diamond, diamond-like-carbon, and various nitrides. However, practical applications of these materials are not achieved yet. As another solution to reduce driving voltage, a conception that an active device controls the emission

current of FEA has already been proposed [2], and some successful results by combining an active device and an FEA or an emitter on a single substrate are reported [3, 4].

One-transistor and one-FEA configuration seems to be the simplest and most suitable for one-chip FED [5]. In the configuration, the MOSFET acts as a line selection switch by driving the gates of MOSFET and the common sources are controlled by current or voltage driving mode. The term, MCFEA (MOSFET-controlled FEA) has been proposed in IDW97 [6]. When integrating FEA and driving circuits with MOSFET, the active devices in the pixels for driving FEAs can be made without any additional process steps. Ideally, it requires only as high as the threshold voltage of the MOSFET to drive an MCFEA and it gives extra benefits including stable and uniform emission current. It also reduces loading capacitance of driver circuits since MOSFET gates are driven instead of the FEA gates that have larger area.

Although the driver circuit for MCFEA can be composed of the ordinary MOSFETs, the MOSFET in MCFEA must endure high voltage between the drain and the source. When turned on, it must be able to flow drain current as large as required emission current. When turned off, it must restrict drain current under 1/100 of the turn-on emission current and must be protected from breakdown due to the drain to source voltage as high as the FEA extraction gate voltage.

Fig. 1 shows the structure of a fabricated HVMOSFET for an MCFEA [3, 6]. 4600 Å silicon dioxide layer is used for the gate insulator and patterned molybdenum layer is used for the gates. The MOSFET channel is composed of an active region

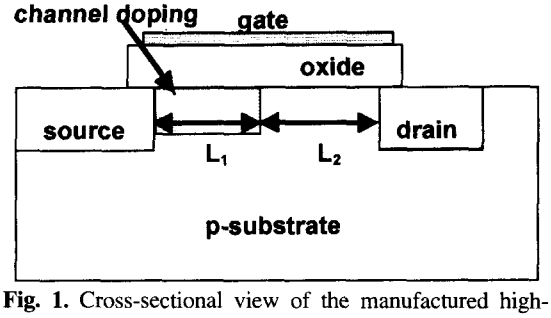

Fig. 1. Cross-sectional view of the manufactured high-voltage MOSFET for MCFEA.

(L_1) and a drift region (L_2). While L_1 is mainly contributed to channel current control, L_2 is designed for high voltage breakdown. Therefore the threshold of active region is controlled by doping p+ impurities. Instead, the threshold voltage of drift region remains about 0 volt to keep low doping concentration which reduces electric field around drain edge to increase the drain breakdown voltage. Fig. 2 shows the measured turn-on and turn-off characteristics for two HVMOSFETs with the same channel width, W (50 μm) and L_1 (40 μm), and different L_2 (60 μm and 120 μm). As expected, only the active region controls the saturation current but the linear region current is fairly affected by drift region also, because the voltage drop across the drift region modulated the effective drain voltage at the active region. When turned on, the measured results show rapid current increasing near the drain voltage of 70 V and the starting voltage lowers with increasing saturation current. It is mainly caused by the avalanche breakdown at the drain edge. Since the field emitter requires large gate to cathode voltage to flow cathode current, the MOSFET drain voltage is less than 30V when turned on. So only the breakdown voltage of turn-off characteristics must be considered. The measured breakdown voltage at the gate voltage of 0V is 70 V which is high enough comparing with the FEA operating voltage of 60 V. When turned off, the drain current is measured to be under 10 nA with drain voltage of 60 V. So, the on-off current ratio of MCFEA can be over 100 assuming maximum pixel current of 10 uA order.

Fig. 3 shows the measured emission current char-

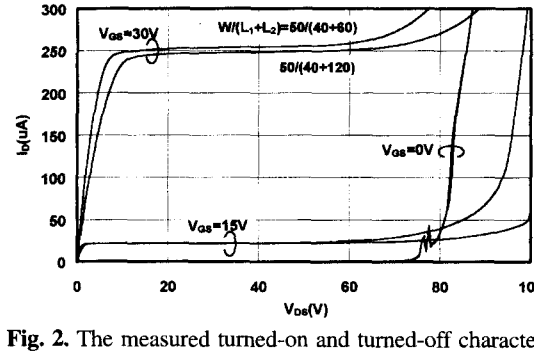

Fig. 2. The measured turned-on and turned-off characteristics for the high voltage MOSFETs with 60 μm and 120 μm drift region length. The drift region width is 50 μm and the active region sizes are 50 μm / 40 μm for each.

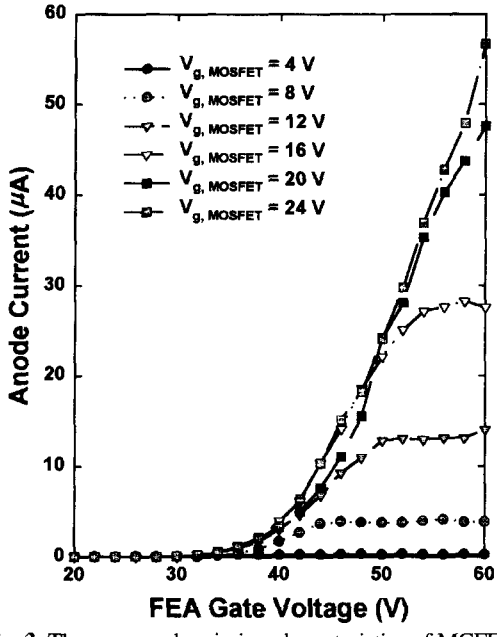

Fig. 3. The measured emission characteristics of MCFEA.

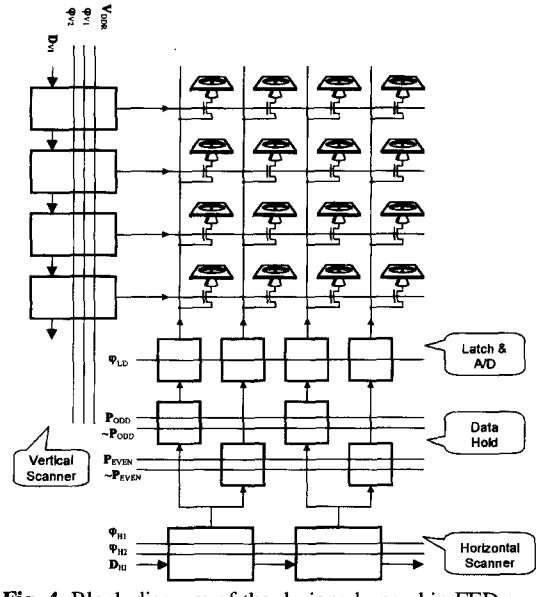

Fig. 4. Block diagram of the designed one-chip FED system.

acteristics with variable HVMOSFET gate voltages. As expected, the emission currents are limited to the saturation current levels of HVMOSFET.

III. Integration of Driver Circuits

The whole structural configuration of one-chip MCFED including MCFEAs and on-chip driving circuits is shown in Fig. 4. Progressive line scanning method is adopted for matrix driving. Either CMOS or nMOS circuits can used for the on-chip driver. CMOS circuits are generally used for integrated TFT-LCD drivers because the thin film transistors reveal unreliable characteristics. However, it requires complicated manufacturing processes including multi layered interconnection and also causes latch-up problem in the case of high voltage driving required for FED operation. Accordingly, nMOS circuits are preferable to integrate with field emitter arrays. But the circuit design should be based on minimum power consumption and large operational margin.

In Fig. 4, the column scanner as a part of the column driver generates the sequential sampling clock signal for pixel data latching and the data holding part samples the pixel data and holds it to drive the current of the pixels. The column scanner is a dynamic one-bit shift register. Bootstrap circuit is used to compensate the signal level drop by the threshold voltage of transfer gate in the column scanner [7]. To reduce the power consumption of nMOS circuit, dynamic logic design is commonly used and can be easily designed for display because the operating frequency is fixed. Fig. 4 shows the circuit design of column scanner circuit, which is similar circuit to that for MOS type image sensor [8].

A unit circuit of the data holding part for the column driver is composed of two signal latch circuits and a digital-to-analog converter (DAC). The first latch samples the continually incoming pixel data synchronized by the output of the column scanner, and the second latch sustains the sampled pixel data for the next one horizontal scanning time to drive the DAC. The DAC controls the emission current according to the latched pixel data and is composed of a constant current source, which is a MOSFET with constant gate bias voltage and a switching transistor. They embody the current-mode pulse amplitude modulation driving for FED [9]. Fig. 6 shows the designed unit circuit of data holding part. If the pixel data have depth of N bits, N sets of unit circuits have to be connected to the corresponding col-

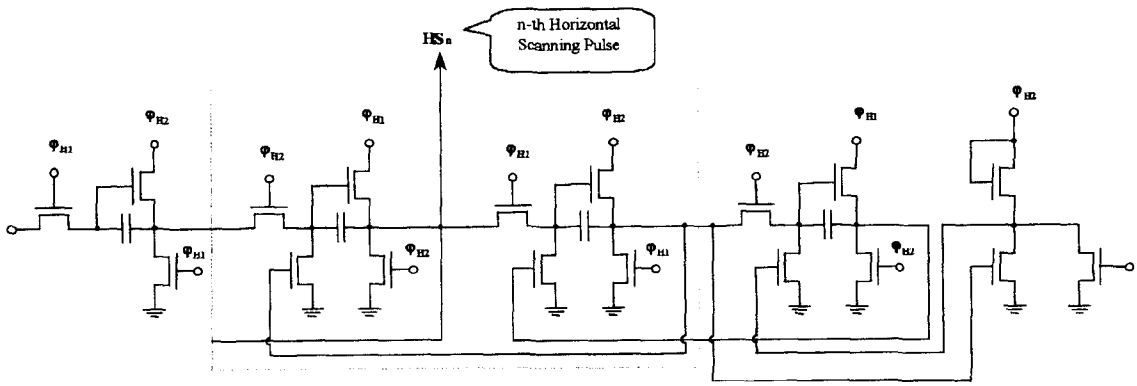

Fig. 5. The designed scanner circuit of the column driver for one-chip MCFED.

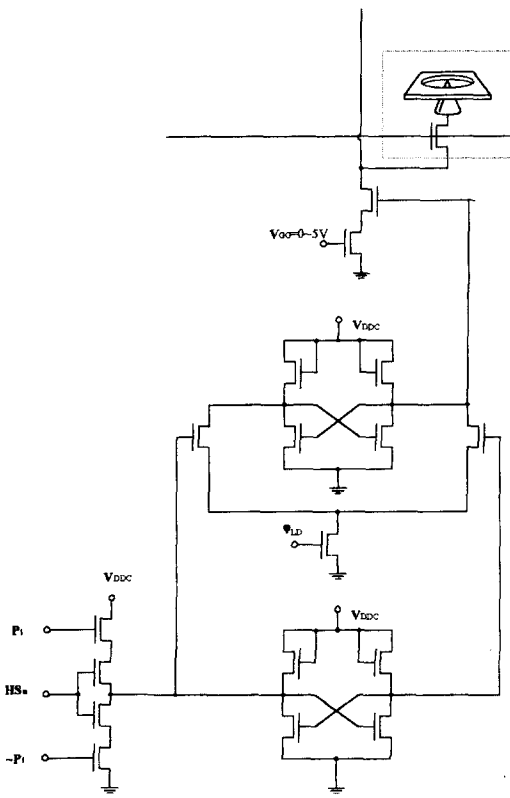

Fig. 6. The designed latch and buffer circuit for the column driver.

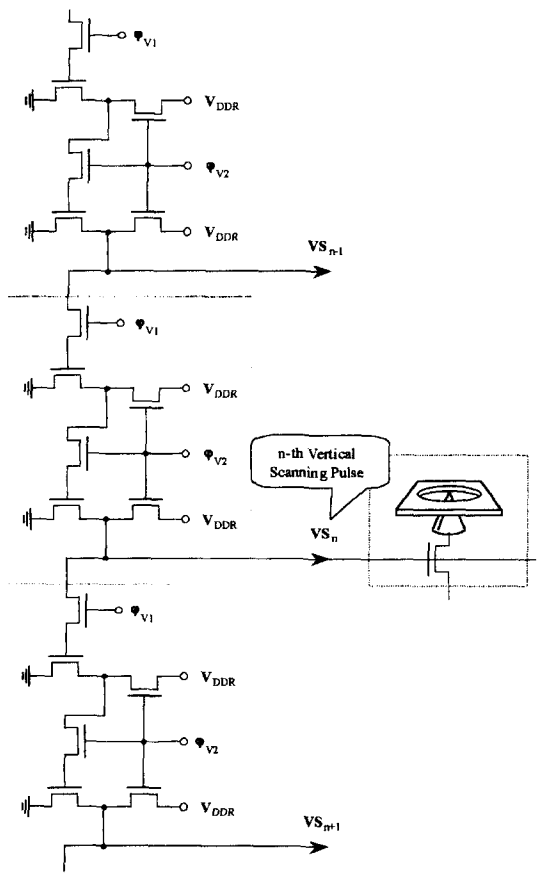

Fig. 7. The designed scanner circuit of the row driver for one-chip MCFED.

umn line in parallel and the width-to-length ratios of the MOSFETs for current sources are increased in binary order according to the weight of connected pixel data.

The row driver circuit is a single-bit shift register with relatively low operating speed. Unlike the column scanner, the row driver cannot use the bootstrap circuit because the row scanning signal must be sustained for a long time over 25 μs and changed completely within the horizontal blanking time of

about 5 μs. Thus level amplifiers, which are inverters activated temporally, are used for the shift register and the loading capacitors formed by gate input capacitance of HVMOSFET are used for signal storage. Fig. 7 shows the designed row driver, which is also similar to that for MOS type image sensor [8]. In the circuit, the two complementary driving clocks go to the HIGH level sequentially during only the horizontal blanking time to activate the inverters and shift the signal. They are kept at the LOW level to minimize the static power consumption.

All the designed circuits are verified by SPICE circuit simulation. Level 3 models are used for LVMOSFET and HVMOSFET. The field emitters are also modeled by dependent current sources and

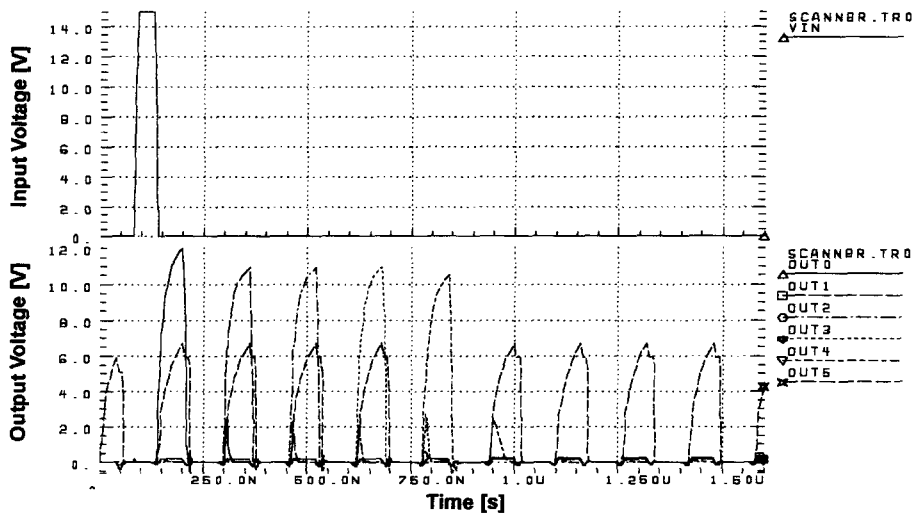

Fig. 8. SPICE circuit simulation result of the designed scanner circuit of column driver.

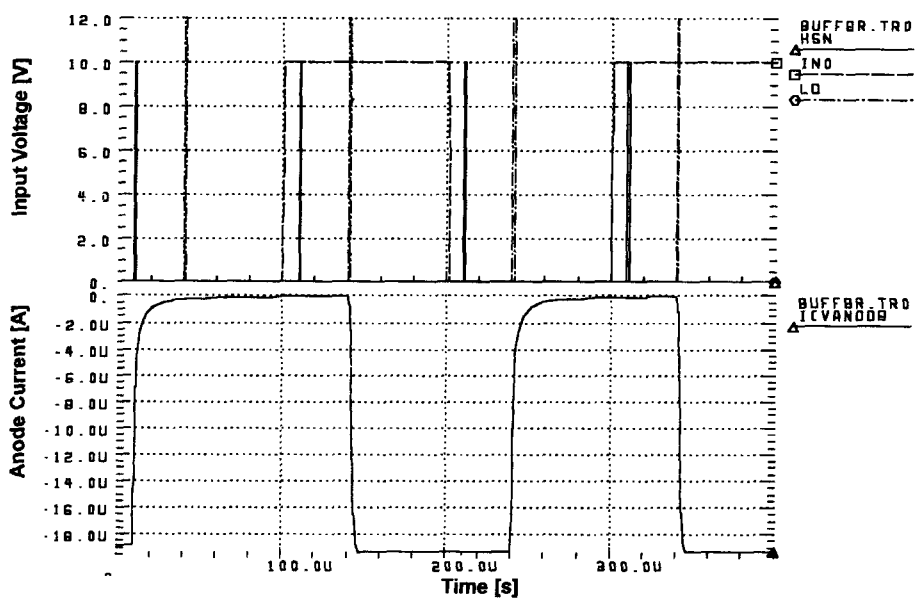

Fig. 9. SPICE circuit simulation result of the designed latch and buffer circuit of column driver.

parasitic elements [10]. In time transient simulation, the operating speed is assumed to be in VGA mode 2 in which the display pixel numbers are 640(H) × 480(V). Fig. 8 to 10 show the simulation results for the designed column and row driver circuits, which prove that all the circuits work as expected.

Fig. 8 shows the result for 5 stages of column scanners driven by 6.3 MHz clocks that is quarter of VGA pixel data rate. The scanner output signals named OUT0 to OUT4 sequentially rise and fall to the proper levels within a driving period. The output named OUT5 represents the final stage output for feedback to discharge the bootstrap capacitor of the last stage. Fig. 9 shows the result for a column buffer stage and a MCFEA pixel with alternating pixel data signal named IN0. The buffer stage latches the pixel data while the scanner output signal named HSN is high and transfers it to the second latch, which activate the current source connected to the MCFEA pixel while the loading signal named LD is high. The result shows that the anode current rises to 20 μA rapidly after latching high pixel data and falls relatively slowly after latching low pixel data. But the output waveform is enough for driving in VGA mode. Fig. 10 shows the results for row driver circuits driven by 28 kHz clocks that is vertical driving frequency for VGA mode. After the input signal named VIN get high, the output signals name OUT0 to OUT5 for the six row driver stages sequentially stay in high level for one horizontal scan time with proper rising and falling times.

IV. Conclusion

Fig. 11 shows a part of the physical layout result for the designed circuits by adopting 5 μm design rule. In the figure, MCFEA pixels of 400 μm 400 μm size are arrayed as core part and the row and column driver circuits are located at left side and bottom, respectively. Each pixel contains 625 field emitter tips.

These circuits are designed for simplicity to save area and to reduce error probability and for low power consumption to maximize the merit of on-chip driving circuit. By integrating the driver circuits and MCFEAs on a same substrate, the number

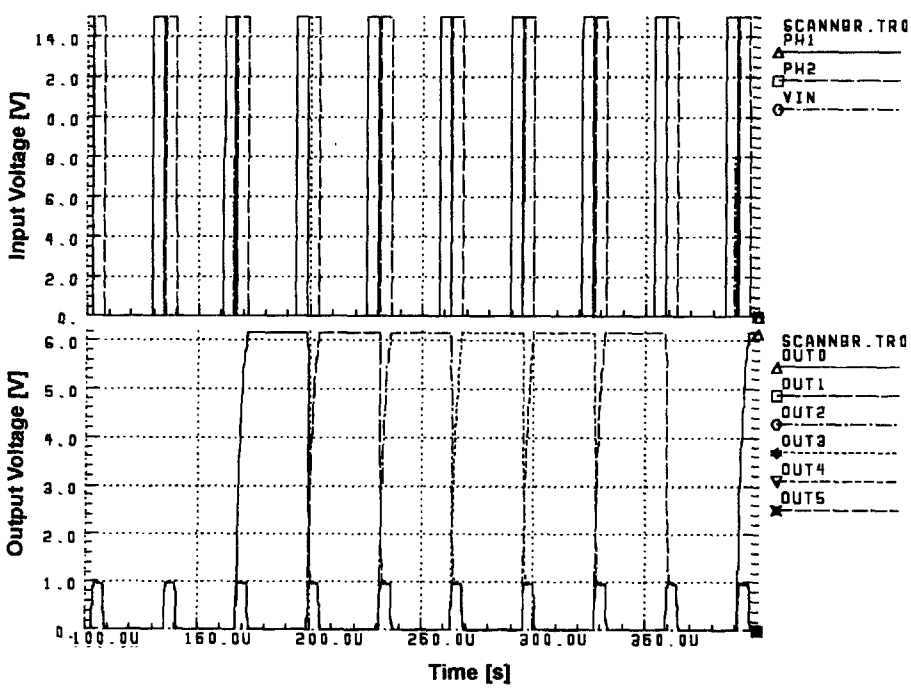

Fig. 10. SPICE circuit simulation result of the designed scanner circuit of the row driver.

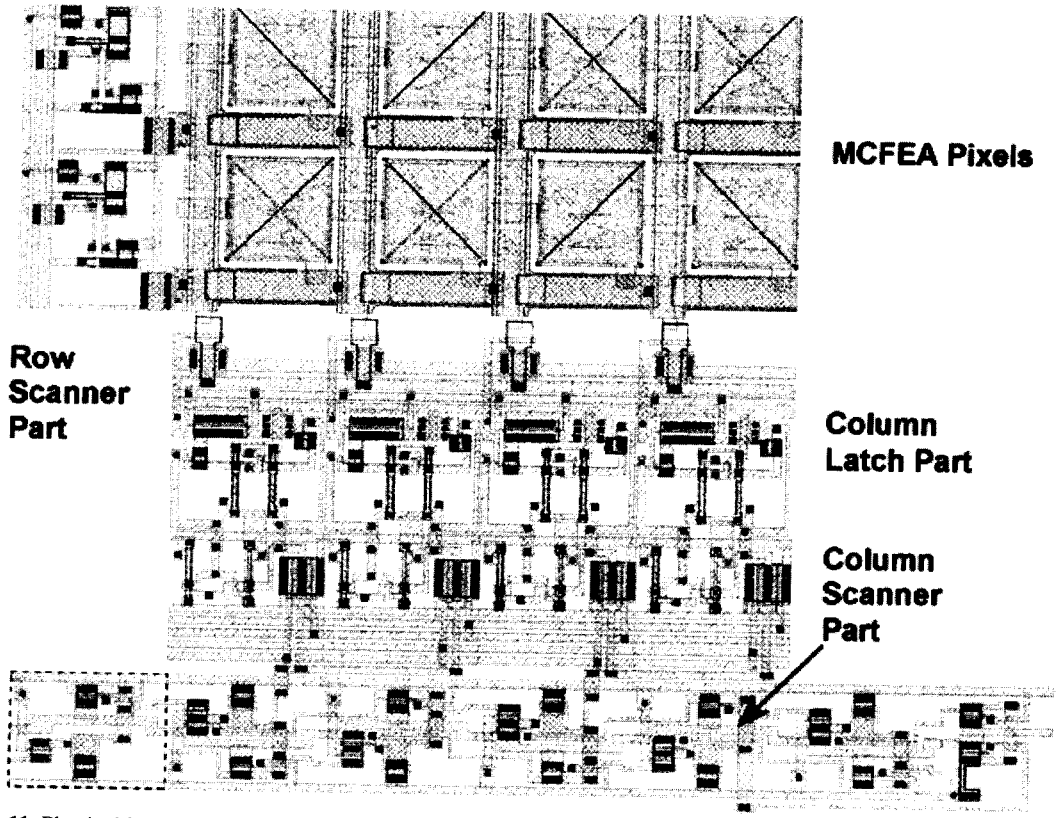

Fig. 11. Physical layout result of the integrated driving circuits and MCFEA pixels.

Table 1. The designed signal I/O line names

Number	Signal Name	I/O	Function
1	GND	Input	Ground
2	VDDH	Input	Column driver power supply
3	PHIH1	Input	Column scanner driving clock 1
4	PHIH2	Input	Column scanner driving clock 2
5	DINH	Input	Column scanner start signal
6	DOUTH	Output	Column scanner end signal
7	PODD	Input	Pixel data for odd columns
8	PODD-	Input	Inverted pixel data for odd columns
9	PEVEN	Input	Pixel data for even columns
10	PEVEN-	Input	Inverted pixel data for even columns
11	PHILD	Input	Column latch load signal
12	VGG	Input	Gate bias for constant current sources
13	VDDV	Input	Row driver power supply
14	PHIV1	Input	Row scanner driving clock 1
15	PHIV2	Input	Row scanner driving clock 2
16	DINV	Input	Row scanner start signal
17	DOUTV	Output	Row scanner end signal
18	VFEAG	Input	Extraction gate bias voltage for field emitters

of external I/O lines can be less than 20 irrespective of number of pixels. The designed I/O line names are listed in Table 1. The driver circuits consume the area as large as two or three lines of pixels and it can be negligible compared with the 640×480 lines of VGA display.

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