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Electrical characteristics of lateral poly-silicon field emission triode using LOCOS process

Jae-Hoon Lee, Myoung-Bok Lee, Dong-Il Park, Sung-Ho Ham*,
Jong-Hyun Lee and Jung-Hee Lee

School of Electronic and Electrical Engineering,
**Sensor Technology Research Center, Kyungpook National University, Taegu, 702-701, Korea*

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Abstract – Using the LOCOS process, we have fabricated the lateral type polysilicon field emission triodes with poly-Si/oxide/Si structure and investigated their current-voltage characteristics for three biasing modes of operation. The fabricated devices exhibit excellent electrical performances such as a relatively low turn-on anode voltage of 14 V at $V_{GC} = 0$ V, a stable and high emission current of 92 μA/triode over 90 hours, a small gate leakage current of 0.23 μA/triode and an outstanding transconductance of 57 μS/5triodes at $V_{GC} = 5$ V and $V_{AC} = 26$ V. These superior electrical operation is believed to be due to a large field enhancement effect, which is related to the sharp cathode tips produced by the LOCOS process as well as the high aspect ratio(height/radius) of the cathode tip end.

key words: LOCOS (local oxidation of polysilicon), low turn-on anode voltage, large transconductance, microwave device, lateral type FED(field emission display)

I. Introduction

Recently the study of field emission devices has been actively progressed for their various applications [1-7] in high speed and high frequency devices, microsensors and flat panel displays [8], using the advanced semiconductor production techniques adaptable to fabricate the micron scale field emission devices.

In 1976, Spindt *et al.* fabricated the thin-film field emission cathode and demonstrated them as a potential source of free electrons for the first time [2]. In the late 1980s, Kosmahl developed a wide band amplifier including a field emission triode with an appropriately modified molybdenum cathode for high frequency operation [3] and Lally et al. also reported the design of an X-band amplifier based on the same cathode material [4]. Later, Spindt *et al.* [5] presented a field emitter array with a cut-off frequency of 5 GHz. They have stressed that high emitter packing density and small total area of the array are strongly relevant to high frequency operation. Park *et al.* recently proposed and fabricated a lateral field emitter triode with a polysilicon cathode and a molybdenum gate by utilizing an in-situ vacuum sealing technique [6].

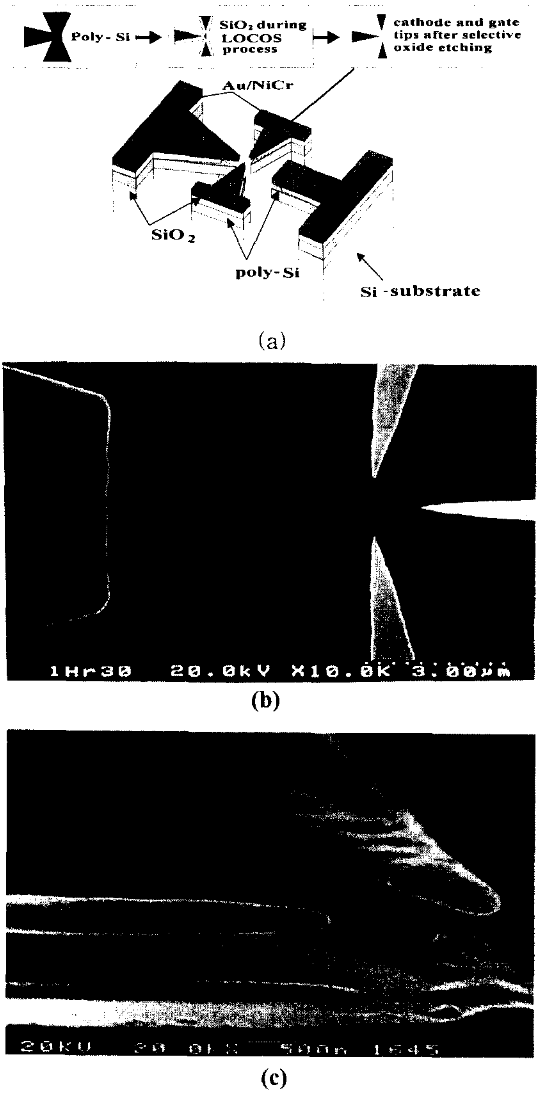
Nevertheless, most of the devices mentioned above suffer from a low output current density and/or relatively small transconductance. The compatibility with standard IC fabrication processes also remains questionable. In this study, we report on a lateral polysilicon field emission triode array with silicon on insulator structure (Si_3N_4 / SiO_2 / poly-Si/ SiO_2) fabricated using a simple LOCOS process. The final devices exhibit a lower turn-on anode-cathode voltage and higher current operation with much higher transconductance, all of which are strongly related to the cathode shape with extremely sharp tip and also relatively short inter-electrode/tip distance obtained especially by LOCOS process.

II. Experiment

A schematic view of the fabricated field emission triodes is shown in Fig. 1(a), of which detailed processes are similar to those used for the fabrication of the diodes as described elsewhere [9]. Typical features of fabrication are as follows: i) A buried silicon dioxide of 6000 Å thickness was grown on a p-type (100) silicon substrate by a wet thermal oxidation at 1000°C. ii) An n^+-doped polysilicon layer of 5000 Å was then deposited by LPCVD (low pressure chemical vapor deposition). iii) After sequential depositing of silicon dioxide of 500 Å and silicon nitride of 1600 Å as an oxidation barrier, the top three layers of Si_3N_4 / SiO_2 / poly-Si were selectively etched down to the bottom oxide by RIE (reactive ion etching) with photolithographic definition of the electrodes. The pattern of the polysilicon cathode tip was broadly designed to overlap with those of two gates by approximately 0.4 μm and the anode pattern was separated from the gate tip end by 5 μm. iv) Next, the polysilicon layer was laterally oxidized by the LOCOS at 1150°C in dry oxygen ambient for 90 min to control both the spacing between the cathode and gate electrodes and the sharpness of the tip ends of those electrodes. During the oxidation, the overlapped polysilicon layer is to be separated into four parts, one cathode, two gate tips and one small triangular shaped island. v) For metallization, the top Si_3N_4/SiO_2 layers were selectively etched and then Au/NiCr contact was made by thermal evaporation and subsequently annealed at 350°C for 30 min in the nitrogen ambient. vi) Finally, all the oxides surrounding the polysilicon, laterally formed LOCOS oxide, deposited top oxide and thermally grown bottom oxide, were etched out in BHF (buffered hydrofloric acid) solution to lift off the polysilicon island and to isolate the sharpened cathode and gate tips.

III. Results and Discussion

SEM photographs after the LOCOS plus subsequent oxide etching are shown in Fig. 1(b) and (c) with an anode-to-cathode tip distance of approximately 6.5 μm, a gate-to-cathode tip distance of approximately 1 μm and a gate aperture of approximately 1.5 μm. It is well illustrated that both cathode and gate tips are sharpened by the LOCOS and isolated by the selective oxide etching. Prior to the electrical measurement, the samples were loaded into a vacuum chamber in a pressure of about 2×10^{-6} torr and heated at 100°C for 1 h to get rid of water vapor or other residual contaminants near the electrodes. An array of 5 field emitters is prepared for the electrical measurement. To check the applicability and identify the emission mechanism, we have measured the current-voltage (I-V) characteristics in three configurations of i) normal operation mode with lateral symmetric gates, ii) silicon substrate-gate mode and iii) silicon substrate-anode mode as shown in Fig. 2 (a), (b) and (c).



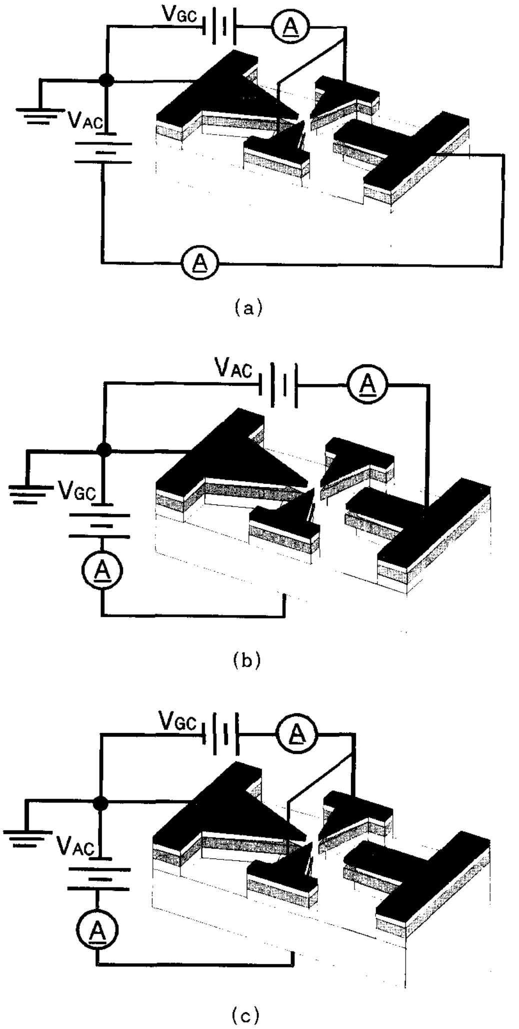
(a)

(b)

(c)

Fig. 1. A schematic view and SEM photographs of the field emission triode : (a) the lateral field emission triode, (b) and (c) top and side view of the triode.

As a typical result, Fig. 3 displays the normal operation-mode anode I-V curves for various gate voltages (V_{GC} ; −15 V SIM 15 V) as marked in each curve and clearly illustrates a strong and effective modulation of the anode current (I_A) by gate bias.



(a)

(b)

(c)

Fig. 2. Three operation modes of lateral field emission triodes : (a) Normal operation, (b) Asymmetric Si-substrate gate mode, and (c) Si-substrate anode mode.

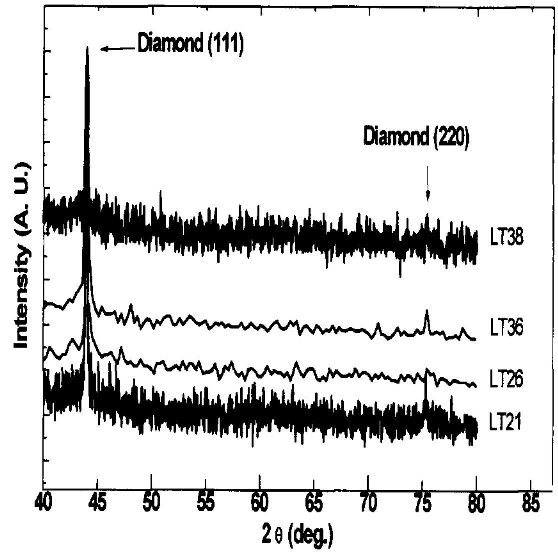


Fig. 3. Anode I-V characteristics of the field emission triodes in the normal operation mode. Insert : anode I-V characteristics for V_{GC} = 0 V and the corresponding Fowler-Nordheim plot.

The turn-on cathode-anode voltage for the electron tunneling was as low as only 14 V at $V_{GC} = 0$ V and also, the average emission current of each device was observed to be as high as 65 μA. As a representative driving capability of the fabricated triodes, the average transconductance (g_m) of 5 triodes was calculated to be about 57 μS at a bias condition of V_{GC} = 5 V and V_{AC} = 26 V and is gradually enhanced from 11 to 113 μS for the increase of gate voltages from −10 to 15 V. The current levels and transconductance were one or two orders higher than those of other lateral field emission triode previously reported [5, 6]. This outstanding performance can be understood by the optimized device specifications; the lateral oxidation of polysilicon renders both tips of cathode and gate electrodes to be sharp enough with high aspect ratio, keeping a minimum inter-electrode distance. Then, strong field enhancement effect would be induced between the two electrodes as described in ref. [9].

The insert in Fig. 3 shows the anode I-V curve for cathode-gate bias and the resulting Fowler-Nordheim plot. The linearity of the Fowler-Nordheim plot as shown has been indicative of the field emission phenomena between the cathode and anode tips. The gate leakage current of each triode was observed to be as low as about 0.23 μA at $V_{GC} = 5$ V and $V_{AC} = 26$ V. The current ratio, I_A/I_G was larger than 400 under the same bias condition and higher than 352 up to V_{GC} = 15 V. The test result of the long-term stability of the triodes is shown in Fig. 4 for the emission current of 460 μA driven by the bias condition of $V_{GC} = 5$ V and $V_{AC} = 26$ V and reveals a stable emission property with only small fluctuations of ±4.6% over 90 hours.

Fig. 5 shows the I-V characteristics of the triodes measured by the silicon substrate-gate mode and the anode current turns out also to be strongly modu-

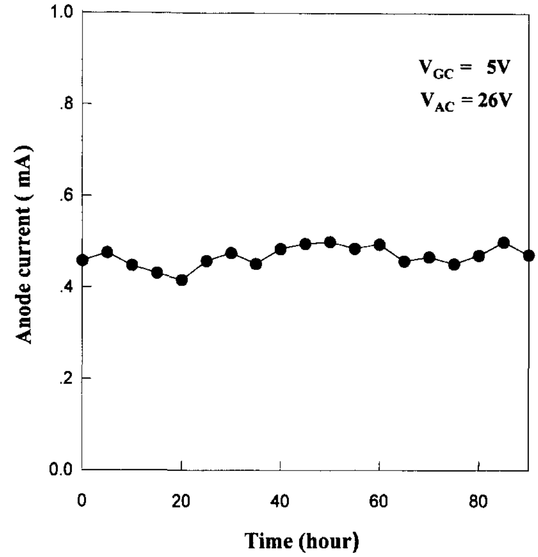


Fig. 4. Long term stability curve of the field emission triodes at a constant current of 460 μA.

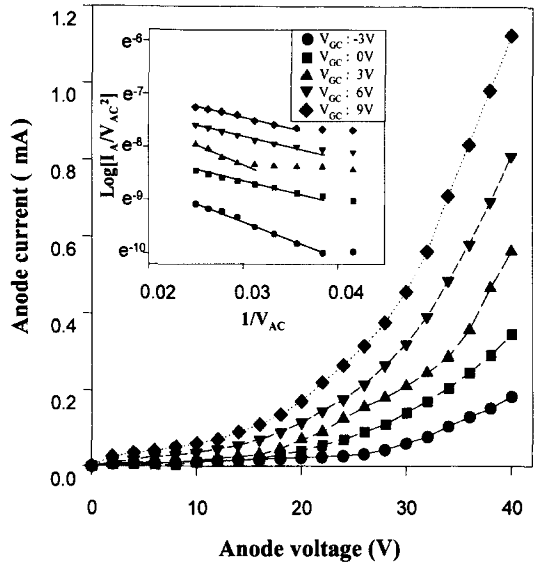


Fig. 5. I-V characteristics of the triodes in the asymmetric Si-substrate gate operation.

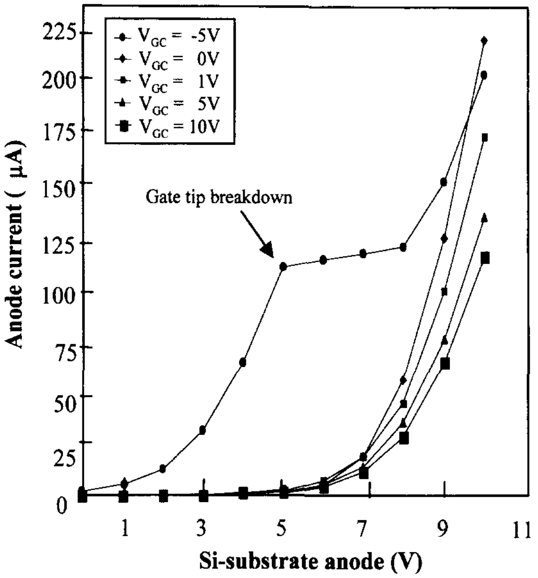


Fig. 6. I-V characteristics of the triodes in the Si-substrate anode operation mode.

lated by applying the gate voltage between the cathode and silicon substrate. The turn-on anode voltage was about 22 V at $V_{GC} = 0$ V and the transconductance was about 47 μS / 5 triodes at $V_{GC} = 5$ V and $V_{AC} = 26$ V. These inferior electrical characteristics compared with those of the normal mode operation is believed to be due to the flat shape of the silicon substrate gate with an extremely narrow gap of 0.6 between the cathode tip and substrate. The insert also displays the corresponding Fowler-Nordheim plot which confirms the field emission mechanism of the anode current.

Similar I-V curves of the triodes has been recorded in a configuration of silicon substrate-anode mode and is demonstrated as Fig. 6. This operation mode is practically important for the applicability to the flat panel display. The turn-on anode voltage was as low as about 6 V and the emission current was about 43 μA/ triode at $V_{GC} = 0$ V and $V_{AC} = 10$ V. Since the distance (0.6 μm) between the cathode and substrate anode is shorter than the cathode-to-gate distance of about 1 μm, much lower turn-on anode voltage and much higher emission current have been expected with respect to those of lateral emission mode. In this orientation, the gate tips can also act as a cathode under the bias condition resulting in the large difference between the anode and gate electrodes. As a result, we have observed a dramatic change of the emission current with the polarity change of the gate bias as shown in Fig. 6. Furthermore, the abrupt decrease in dI/dV observed at $V_{GC} = -5$ V and $V_{AC} = 5$ V can be attributed to the arc discharge phenomena between the gate and substrate or gate tip breakdown because of the high electric field strength of approximately 2×10^5 V/cm. Considering these results, one can predict an average current density of about 50 A/cm^2 for a probable arrangement of an FED pixel of 60×60 μm^2 area including 40 tips and conclude these current density to be sufficient for a typical FED application.

IV. Conclusion

Using the LOCOS process, we have fabricated a lateral field emitter array. The sharpness of both cathode and gate tips and the gap between them could be controlled by carefully designed LOCOS process conditions. The fabricated devices exhibited excellent field emission characteristics such as relatively lower turn-on anode voltage, very high emission current per tip with small gate leakage current and high transconductance which are relevant to the strong field enhancement effects due mainly to the sharper cathode and gate tips formed during the LOCOS. As a typical feature of the fabricated triodes, the high anode current per tip of the array may provide a good possibility in fabricating a vacuum microwave power device and field emission display. We have also checked the practical applicability of the devices to the flat panel display devices as well as high speed electronics.

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References

[1] I. Brodie and C. A. Spindt, Adv. *Electron. Phys*. **83**, 1 (1992).
[2] C. A. Spindt, I. Brodie, L. Humphrey, and E. R. Westenberg, *J. Appl. Phys*. **47**, 5248 (1976).
[3] H G. Kosmahl, *IEEE Trans. Elec. Dev.* **36**, 2728 (1989).
[4] P. N. Lally, Y. Gorden, and E. A. Nettesheim, *IEEE Trans. Elec. Dev.* **36**, 2738 (1989).
[5] C. A. Spindt, C. E. Holland, A. Rosengreen, and I. Brodie, *IEDM Dig. Tech. Papers*, 749 (1993).
[6] C. M. Park, M. S. Lim, and M. K. Han, *IEEE Elec. Dev. Lett* **18**, 538 (1997).
[7] S. Kanemaru and J. Itoh, *IEEE Trans. Elec. Dev.* **38**, 2334 (1991).
[8] C. A. Spindt, C. E. Holland, I. Brodie, J. B. Mooney, and E. R. Westerberg, *IEEE Trans. Elec. Dev.* **36**, 225 (1989).
[9] J. H. Park, H. I. Lee, H. S. Tae, J. S. Huh and J. H. Lee, *IEEE Trans. Elec. Dev.* **44**, 1018 (1997).