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A prototype active-matrix field emission display with poly-Si field emitter arrays and thin-film transistors

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Abstract – We present, for the first time, a prototype active-matrix field emission display (AMFED) with 25×25 pixels in which polycrystalline silicon field emitter array (poly-Si FEA) and thin-film transistor (TFT) were monolithically integrated on an insulating substrate. The FEAs showed relatively large electron emissions above at a gate voltage of 50 V, and the TFTs were designed to have low off-state currents even though at high drain voltages. The integrated poly-Si TFT controlled electron emissions of the poly-Si FEA actively, resulting in improvement in the emission stability and reliability along with a low-voltage control of field emission below 25 V. With the prototype AMFED we have displayed character patterns by low-voltage peripheral circuits of 15 V in a high vacuum chamber.

I. Introduction

Recently, field emission display (FED) has emerged as a leading contender in display technologies because it combines the best features of cathode ray tube (CRT) and flat panels [1]. The FED utilizes field emitter arrays (FEA) arranged in a X-Y matrix, simple-matrix FEA, as a cold cathode. While the simple-matrix FEA has a merit in the fabrication process it retains the intrinsic problems of field emission mechanism, such as non-uniformity and instability, and further requires high-voltage circuits for driving.

An active-controlled FEA or active-matrix FEA (AMFEA) with the semiconductor devices such as metal-oxide-semiconductor field-effect transistor (MOSFET) and thin-film transistor (TFT) has been proposed to solve the intrinsic problems of field emission [2-5]. The incorporated semiconductor devices directly connected to FEAs should have the properties of high-voltage transistors to switch the emission current at a constant FEA gate voltage. In the off-state, the voltage at the FEA cathode is increased to turn off field emission, and the drain voltage is also increased. As the result, the control transistors are required to have a high-breakdown voltage and a low leakage current in the off-state. Since the control device of the AMFEA controls electron emission of the FEA actively, the addressing voltage and power consumption can be greatly reduced along with improvement in uniformity and stability of field emission. Also, all pixels in the AMFEA are isolated each other so that the cross-talks between neighbor pixels and the line faults due to a short-circuit-failure of the gated FEA can be completely excluded, like the case of active-matrix liquid crystal display (AMLCD).

Although a single active-controlled FEA using single crystalline [2, 3] or polycrystalline silicon (poly-Si) devices [4, 5] has been reported, no work has been made in active-matrix approach for the FED panel. In this work, we first report the active-matrix FED (AMFED) using poly-Si FEA [6] and TFT technologies in the cathode plate. The poly-Si TFT that has been commonly used in AMLCD [7] was selected as a control device because of its relatively high drive-current and process compatibility with glass-substrates.

II. Experiments

We have designed the AMFEA with 25×25 pixels, and each pixel consisted of a gated poly-Si FEA and a poly-Si TFT on an insulating substrate, as shown in Fig. 1. The poly-Si TFT was designed to have an offset of undoped poly-Si, in which the off-

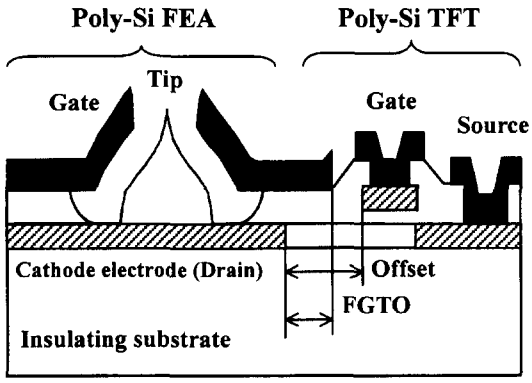

Fig. 1. Unit pixel structure of the AMFEA with a gated poly-Si FEA and a poly-Si TFT. The FGTO indicates the FEA gate-TFT offset overlap.

set decreased off-state drain currents even at a high drain voltage. Furthermore, the gate of the poly-Si FEA was extended to the offset region of the TFT, resulting in the FEA gate-TFT offset overlap (FGTO). In the operation of AMFEA, the FGTO can increase the reduced on-current of the offset-TFT because it is biased with a constant extraction gate voltage and then induces carriers in the offset region.

The poly-Si FEA and TFT of the AMFEA shown in Fig. 1 can be monolithically integrated on a single substrate. The detailed fabrication processes are as follows; Amorphous silicon (a-Si) films of 0.3 μm thickness were formed on thermally oxidized silicon wafers (SiO_2/Si) by low-pressure chemical vapor deposition (LPCVD) using Si_2H_6 gas at 470°C. The films were then solid-phase crystallized at 600°C and patterned to define the active channel of the TFT and the cathode electrode. After isolating the TFT region using oxide, a-Si of 1.5 μm thickness was deposited for the FEA and emitter tips of a-Si were formed by an etching process [6]. A 0.1-μm-thick oxide and a 0.3-μm-thick poly-Si were sequentially deposited as a gate dielectric and a gate of the TFT, respectively. After patterning the gate and offset of the TFT, phosphorus with $5\times10^{15}/cm^2$ was implanted for doping of the a-Si tips and the source/drain of the TFT. An oxide film of 0.8 μm thickness was deposited by LPCVD at 420°C as a gate dielectric of the FEA. The samples were annealed at 850°C both to convert the a-Si tips into poly-Si ones and to activate the dopants. The contact holes were formed and then TiW of 0.3 μm thickness as a gate metal of the FEA was deposited by sputtering. Using an etch-back process [6], the gate holes of the FEA were formed. Finally, the electrodes of the poly-Si FEA and TFT were patterned by a standard photolithography.

Figure 2 shows micrographs of a unit pixel with the poly-Si FEA and TFT, and a gated poly-Si micro-emitter. The row and column bus lines are connected to the gate and the source of the TFT, respectively. The FEA has 5×5 sub-arrays, and each sub-array consists of 9×9 tips. The micro-emitter has a tip-radius of about 500 Å, a height of 1.0 μm, a cylinder-diameter of 0.5 μm, and a gate hole of 1.5 μm. The length of the TFT offset is 8 μm and the FGTO length from the TFT drain edge is 6 μm.

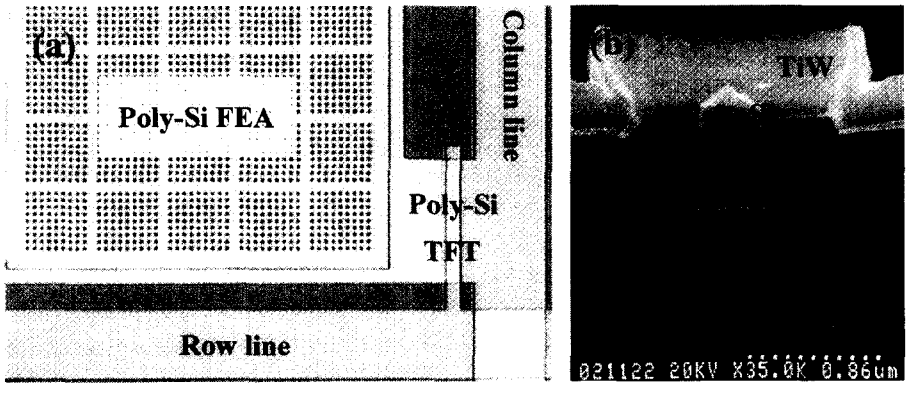

Fig. 2. Micrographs of (a) the unit pixel with poly-Si FEA and TFT, and (b) the gated poly-Si emitter.

III. Results and Discussion

Before measuring the field emission characteristics of the AMFEA, the poly-Si TFT with the offset and FGTO structure was analyzed. Figure 3 shows the output and transfer characteristics of the TFT with a gate length of 10 μm, an offset length of 8 μm, and a FGTO length of 6 μm. The FGTO electrode was biased to 70 V during the measurement. The drain currents showed good saturated behaviors to a drain voltage of 50 V for the gate voltage below 12 V. This result implies that the developed poly-Si TFT can regulate the emission current very well. The breakdown voltage between the source and drain was higher than 70 V which is relatively high comparing with the extraction voltage of FEAs. Also, the drain leakage currents in the off-state were shown to be greatly decreased even at a high drain voltage up to 50 V while the subthreshold property was nearly the same as that of conventional poly-Si TFT, resulting in a high ON/OFF ratio of about 10^5 at a drain voltage of 30 V.

The electron emission characteristics of a unit pixel of the AMFEA are shown in Fig. 4 as functions of FEA gate voltage and TFT gate voltage. The fabricated devices were loaded in an ultra-high vacuum test chamber below 5×10^{-7} Torr to measure emission characteristics. Measurements were carried out at room temperature. The anode voltage was kept 450 V with an FEA-to-anode spacing of 500 μm during the measurements. The anode current of the simple poly-Si FEA, denoted as the crossed data in Fig. 4(a), started to be detected at a gate voltage

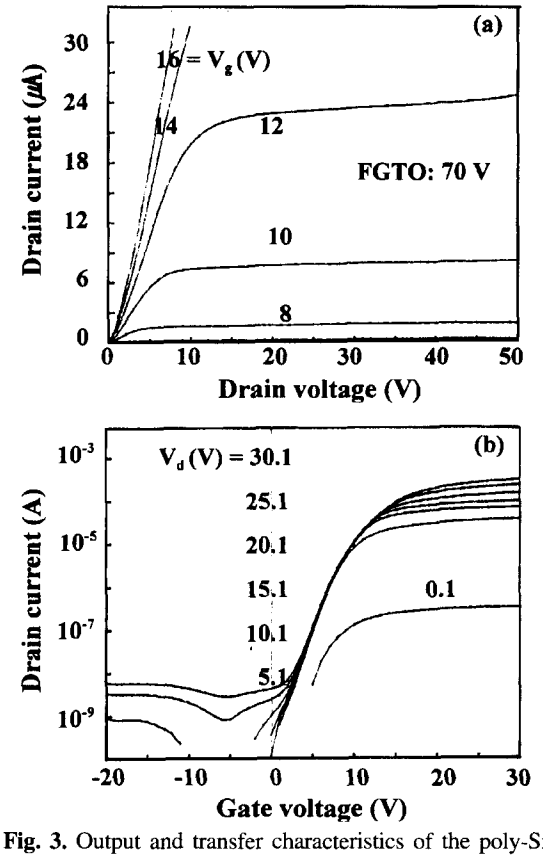

Fig. 3. Output and transfer characteristics of the poly-Si TFT with a gate length of 10 μm, an offset length of 8 μm, and a FGTO length of 6 μm. The V_g and V_d indicate applied voltages to the gate and drain, respectively.

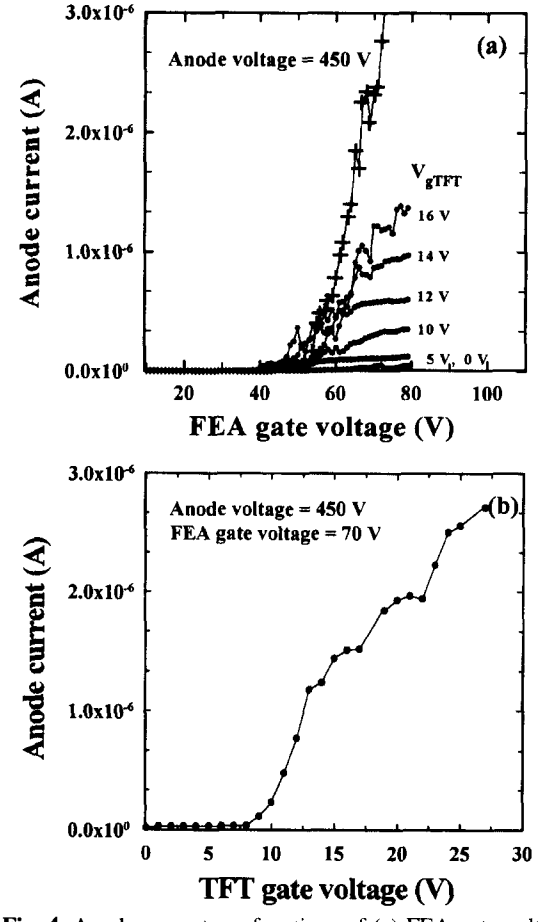

Fig. 4. Anode currents as functions of (a) FEA gate voltage, and (b) TFT gate voltage for the TFT-controlled FEA.

of about 50 V and reached to 2.0 μA (1.0 nA/emitter) at a gate voltage of 65 V while the gate current was remained less than 0.1% of the anode one. The simple FEA showed a typical electron emission performance as previously reported [6].

In the actively controlled-operation mode, the anode currents measured as a function of FEA gate voltage showed saturated behaviors for given TFT gate voltages (V_{gTFT}). Furthermore, the anode current was very well controlled by the TFT with a constant FEA gate voltage of 70 V for electron extraction, as shown in Fig. 4(b). The electron emission was shown to be limited by the drain current of the TFT for gate voltages below 15 V, indicating that reliable and uniform field emissions can be easily obtained by using the developed technology.

Figure 5 shows electron emission fluctuations of the simple and TFT-controlled poly-Si FEAs. The data points in Fig. 5 were taken from the mean values of 5 anode currents measured for one second with constant voltages. The TFT-controlled FEA exhibits a little emission fluctuation with a standard deviation of 22 nA for an average anode current ($I_{A.avg}$) of 324 nA for 650 s, while the simple FEA has a very large fluctuation with a standard deviation of 121 nA for an $I_{A.avg}$ of 290 nA. This result suggests that field emissions can be much stabilized by the integrated TFT. The fairly large emission fluctuation even for the TFT-controlled FEA may be due to a large surface roughness of poly-Si tips compared with c-Si ones, along with its operation point in the linear region of TFTs.

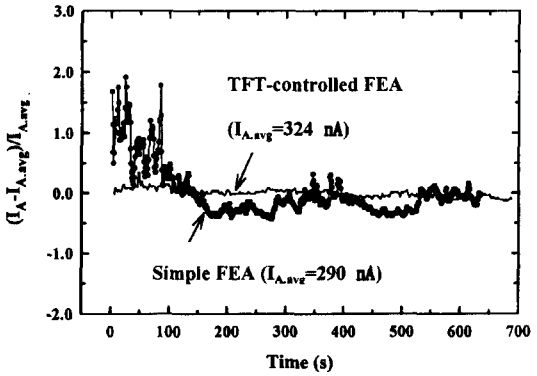

Fig. 5. Electron emission fluctuations of the simple and TFT-controlled FEAs. The I_A and $I_{A.avg}$ indicate the anode currents and their average value, respectively.

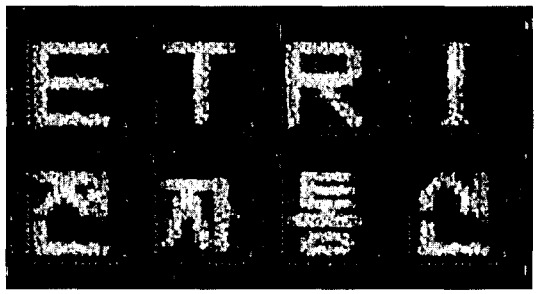

Fig. 6. Displayed characters with the prototype AMFED having 25×25 pixels in a high vacuum chamber.

Two major problems with the practical applications of FEAs are the controllability and reliability of electron emission. A simple solution to these problems is to employ a resistive layer under the emitter tips [8]. This method is a passive technique and further requires a high-voltage control. However, the developed AMFEA with poly-Si FEA and TFT can provide a good control of electron emission with low-voltage complementary metal-oxide-semiconductor (CMOS) circuits.

Figure 6 shows displayed characters of the prototype AMFED with 25×25 pixels in a high vacuum chamber. The anode plate with ZnO phosphor emitting bluish green lights was loaded above the AMFEA cathode plate with a spacing of 3 mm. The display signals of the row and column drivers were addressed to the TFT in each pixel with a pulse amplitude of 15 V while all the FEA gates and the anode plate were kept constant voltages of 70 V and 450 V, respectively. With the prototype device we have displayed character patterns with a relatively high contrast ratio, as shown in Fig. 6. The developed AMFED panel can provide a uniform and reliable display performance with low-voltage CMOS driver circuits even though requiring a constant high voltage for field emission. Also, our developed technology can be applicable to glass-based AMFED by adopting laser annealing and ion shower methods [9] that are employed in poly-Si TFT AMLCD for crystallization of the a-Si and doping, respectively.

IV. Conclusion

The first prototype AMFED was successfully realized by using poly-Si FEA and TFT technologies. The fabricated panel showed character patterns with

a relatively high contrast ratio by low-voltage peripheral driver circuits of 15 V. We can observe the possibility of AMFED, including improvement in the display performances and low-voltage driving irrespective of a required high-voltage for field emission.

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