Journal of Korean Association of Crystal Growth
Vol. 9, No. 6 (1999) 535-541

Low-dislocation-density large-diameter GaAs single crystal grown by vertical Bridgman method

Tomohiro Kawase, Masami Tatsumi and Keiichiro Fujita
Sumitomo Electric Industries, Ltd. 1-1-1, Koya-kita, Itami, Hyogo 664-0016, Japan

(Received June 9, 1999)

Abstract Low-dislocation-density large-diameter GaAs single crystals with low-residual-strain have been strongly required. We have developed dislocation-free 3-inch Si-doped GaAs crystals for photonic devices, and low-dislocation-density low-residual-strain 4-inch to 6-inch semi-insulating GaAs crystals for electronic devices by Vertical Bridgman (VB) technique. We confirmed that VB substrates with low-residual-strain have higher resistance against slip-line generation during MBE process. VB-GaAs single crystals show uniform radial profile of resistivity reflecting to the flat solid-liquid interface during the crystal growth. Uniformity of micro-resistivity of VB-GaAs substrate is much better than that of the LEC-GaAs substrate, which is due to the low-dislocation-density of VB-GaAs single crystals.

1. Introduction

GaAs crystals are used for the substrates of photonic devices, such as LED and LD, and electronic devices, such as MES-FET, HEMT and HBT. Decreasing dislocation density is the strongest requirement for photonic devices, because dislocations deteriorate device performance and shorten their lifetimes. 2-inch wafers have been mainly used for device processes. However, enlargement of wafer diameter of 2.5-inch to 3-inch is demanded by economics. Cost reduction is even more serious in electronic devices, because the chip sizes are much larger than photonic devices. The size of the wafer has been enlarged from 3-inch to 4-inch, and some device manufactures have started to develop the 6-inch wafer process. Slip-line generation and breakage are serious problems in large diameter wafer process. They are related to the residual strain in GaAs substrates, which is caused during the crystal growth [1].

Figure 1 shows the typical growth techniques of GaAs single crystals. Horizontal Bridgman (HB) and Horizontal Gradient Freeze (HGF), and Liquid Encapsulated Czockralski (LEC) are mature growth techniques, which were developed more than twenty years ago. Vertical Bridgman (VB) and Vertical Gradient Freeze (VGF) are classical techniques, but their production had not succeeded for a long time. Poor temperature control made it impossible to grow a single crystal from a seed crystal reproducibly. Direct contact of GaAs melt to the crucible, namely wetting, sometimes caused poly-crystallization. Recent developments of temperature control technique of VB furnace and of suppression of wetting made it possible to grow single crystals reproducibly. VB became the most notable technique for production of GaAs single crystals.

Growth of large diameter GaAs single crystals with low-dislocation-density and low-residual-strain is very difficult because of the physical properties of GaAs, such as low mechanical strength, high dissociation pressure and small thermal conductivity in comparison with Si.

GaAs crystals after growth do not suffer arsenic evaporation in HB and VB techniques. Therefore the growth under a low temperature gradient can be achieved, so that GaAs crystals with low-dislocation-density and low-residual-strain can be obtained. In LEC growth, arsenic evaporation from the surface of the crystal is inevitable, so that the growth under a low temperature gradient would be difficult. Dislocation density and residual strain of LEC crystals are much higher than those of HB and VB crystals.

It is difficult to obtain large diameter GaAs crystals by HB technique, because quartz boat is deformed at the growth temperature, and the thermal environment around the crystal is asymmetric. The thermal environment around the crystal is symmetric in VB and LEC growth. PBN crucible used in VB technique keeps enough strength at the growth temperature. In LEC growth, the solid-liquid interface does not contact with the crucible, so that the crystals are not affected by the deformation of the crucible.

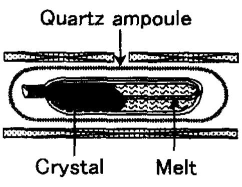
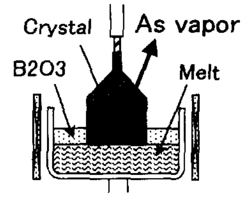
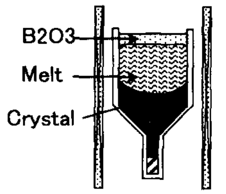
	HB	LEC	VB
			
Evaporation of arsenic	**Non**	**A lot**	**Non**
Temperature gradient	**Low**	**Steep**	**Low**
Crucible/Boat	**Quartz**	**pBN**	**pBN (or Quartz)**
Thermal Environment	**Asymmetric**	**Symmetric**	**Symmetric**
Dislocation-density Residual-strain	**○ (Good)**	×	○
Large diameter	**× (Poor)**	○	○

Fig. 1. Typical growth techniques of GaAs single crystals.

For the reasons mentioned above, VB is the most promising technique to satisfy all requirements of low-dislocation-density, low-residual-strain and large diameter for GaAs substrates. The share of VB is becoming higher in GaAs wafer market. We have developed VB growth of dislocation-free 3-inch Si-doped [2] and low-dislocation-density and low-residual-strain 4-inch to 6-inch semi-insulating GaAs single crystals [3, 4]. Growth and properties of the crystals are reviewed in this paper.

Table 1
Growth conditions of VB technique

	Conductive	Semi-insulating
Dopant	Si	Carbon
Carrier concentration (cm^{-3})	$1\sim40\times10^{17}$	-
Resistivity (Ωcm)	-	$0.5\sim50\times10^{7}$
Diameter (inch)	$2.5\sim3$	$4\sim6$
Weight of the crystal (kg)	$5\sim10$	$10\sim20$
Growth speed (mm/h)	$2\sim5$	$2\sim5$

2. Crystal growth

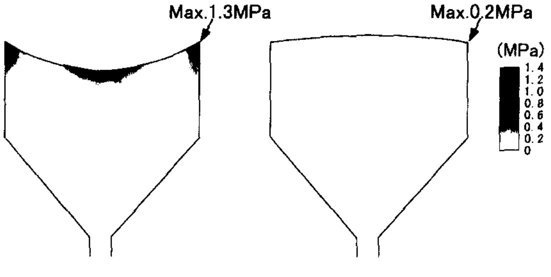
There are two problems to grow GaAs single crystals by VB technique. One of them is wetting. Poly-crystallization is caused at the region where the melt wets the crucible. Inserting a B_2O_3 layer between the crucible and the melt is very effective to prevent wetting. Another problem is a concave solid-liquid interface, which causes large thermal stresses and an increase of dislocation density, sometimes even poly-crystallization.

The growth conditions by VB technique are shown in Table 1. Pre-synthesized GaAs poly-crystals as a raw material and boric oxide are charged in a pBN crucible. The crucible is mounted on a crucible support placed in cylindrical multi-zone heater, which allows to adjust the temperature profile. The temperature of the heater is raised over the melting point, so that the GaAs poly-crystals are melted. The temperature profile of the heater is adjusted and fixed. Then the crucible is moved from higher temperature region to lower temperature region of the heater, so that a GaAs single crystal is grown.

3-inch Si doped conductive GaAs crystals for photonic devices and 4-inch to 6-inch semi-insulating GaAs crystals for electronic devices are manufactured by VB technique.

3. Conductive crystal

Dislocations of Si-doped conductive GaAs substrates are harmful for photonic devices. Dislocation density is mainly increased by the thermal stress. We estimated the relation between the thermal stress and the shape

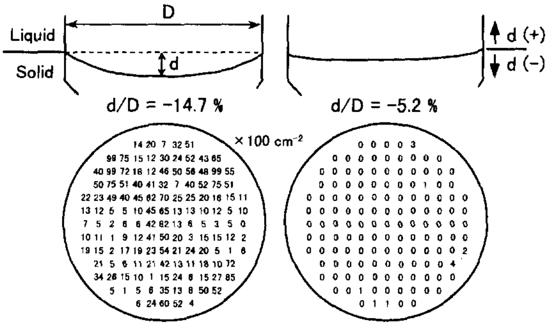


(a) 5°C/cm (b) 15°C/cm

Fig. 2. Distribution of excess shear stress in crystals with (a) concave solid-liquid interface and with (b) flat solid-liquid interface.

of solid-liquid interface according to the Jordans theory [5]. The excess thermal stress is defined as the sum of the positive differences between the absolute value of each of the resolved shear stress components to twelve equivalent <$1\bar{1}0$> slip directions on {111} slip planes and the critical resolved shear stress. Distribution of excess thermal stress calculated using finite element method is shown in Fig. 2. Large thermal stress is caused near the concave solid-liquid interface even under the small axial temperature gradient (5°C/cm) as shown in Fig. 2 (a). Thermal stress is much smaller near the flat interface even under the larger axial temperature gradient (15°C/cm) as shown in Fig. 2 (b).

Figure 3 shows the shapes of solid-liquid interface and the dislocation densities of 3-inch Si-doped GaAs single crystals grown by VB technique. The solid-liquid interface was deduced from striation profiles revealed by photo-chemical etching. Dislocation density of the crystal with flat interface is much lower than that of the crystal with concave interface. Dislocations in a crystal with flat solid-liquid interface were observed by X-ray transmitting topography. Figure 4 shows a X-ray topographic image of a 3-inch Si-doped GaAs substrate with carrier concentration of 8×10^{17} cm^{-3}. There are only a few dislocations in the substrate. This substrate is substantially dislocation-free.



14 20 7 32 51
99 75 15 12 30 24 52 43 65
40 99 72 16 12 46 50 56 48 99 55
50 75 51 40 41 32 7 40 52 75 51
22 23 49 40 45 62 70 25 25 20 16 15 11
13 12 5 5 10 45 65 13 13 10 12 5 10
7 5 2 6 6 42 62 13 6 5 3 5 0
10 11 1 9 12 41 50 20 3 15 15 12 2
19 15 2 17 19 23 54 21 24 20 5 1 6
21 5 6 11 21 42 13 11 18 10 72
34 26 15 10 1 15 24 6 15 27 85
5 1 5 6 35 13 8 50 52
6 24 60 52 4

0 0 0 0 3
0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 1 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 2
0 0 0 0 0 0 0 0 0 0 4
0 0 0 0 0 0 0 0 0 0 0
0 0 1 0 0 0 0 0 0
0 1 1 0 0

EPD Ave. 2700 cm^{-2} EPD Ave. 7 cm^{-2}

Fig. 3. Solid-liquid interface shape and distribution of dislocation density.

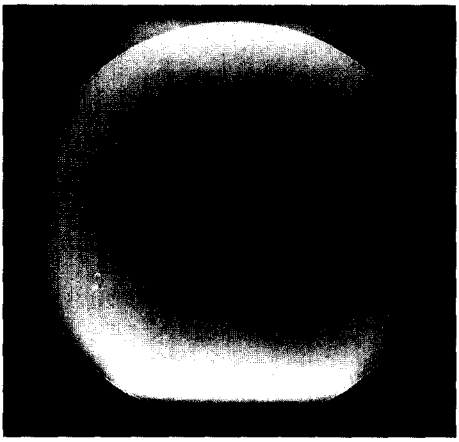


Fig. 4. X-ray topographic image of a 3-inch Si-doped VB-GaAs substrate with carrier concentration of 8×$10^{17}$$cm^{-3}$.

Figure 5 shows the correlation between dislocation density and carrier concentration of Si-doped GaAs crystals grown by HB and VB techniques. EPDs of HB crystals are almost on a curved line. EPDs of VB crystals are much lower than the line. Dislocation-free crystals are obtained even in low-carrier-concentration region. Low EPDs of VB crystals are due to the symmetric shape of solid-liquid interface and symmetric thermal environment.

Residual strains in GaAs crystals were measured by a computer-controlled infrared polariscope [6]. Residual

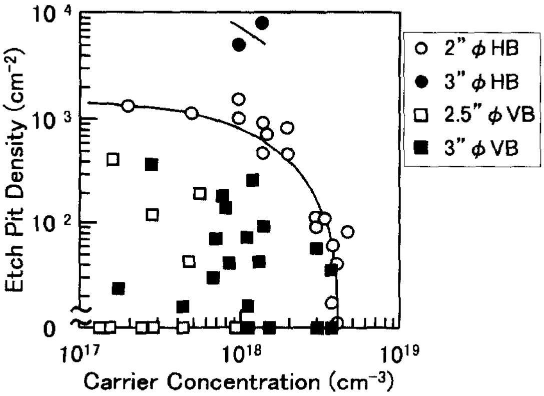


Fig. 5. Dislocation density and carrier concentration of Si-doped GaAs crystals grown by HB and VB techniques.

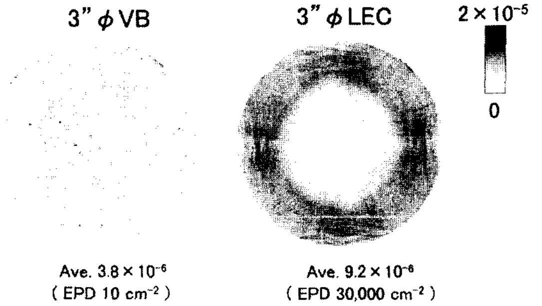


Fig. 6. Residual strains of a 3-inch non-doped LEC-GaAs crystal with high dislocation density of 30,000 cm^{2} and a 3-inch Si-doped dislocation-free VB-GaAs crystal.

strain is related to the density and distribution of dislocations. Figure 6 shows residual strains of a 3-inch non-doped LEC-GaAs crystal with high dislocation density of 30,000 cm^{-2} and a 3-inch Si-doped dislocation-free VB-GaAs crystal. The LEC crystal with high dislocation density shows higher residual strain of 9.2×10^{-6} and 4-fold symmetry which is correlated with the symmetric distribution of dislocations. Dislocation-free VB crystal shows lower residual strain of 3.8×10^{-6} and no symmetry.

4. Semi-insulating crystal

4.1. Dislocation density and residual strain

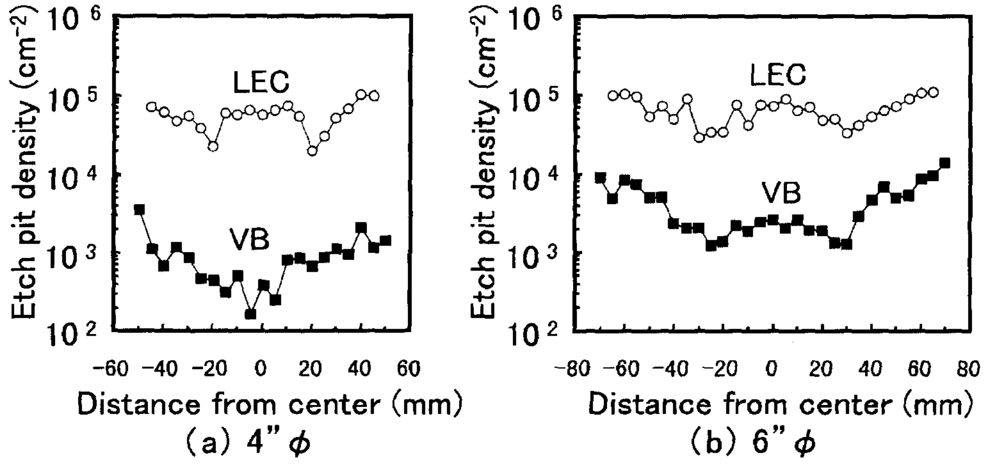
By VB technique we have developed 4-inch to 6-inch semi-insulating GaAs crystals for electronic devices. Keeping flat solid-liquid interface during the crystal growth is most important to suppress lineage formation, which sometimes results in poly-crystallization, and to obtain large-diameter long semi-insulating GaAs single crystals. We applied computer simulation technique to optimize the growth condition, so that 4-inch semi-insulating GaAs single crystals with 20 to 30 cm length, 5-inch and 6-inch single crystals with 15 to 20 cm length have been grown reproducibly.

Figure 7 shows dislocation densities of (a) 4-inch and (b) 6-inch GaAs crystals grown by VB technique. Dislocation density is evaluated by counting the number of etch pits revealed by molten KOH etching. Dislocation densities of both 4-inch and 6-inch VB-GaAs crystals are one order of magnitude lower than that of the LEC crystals.

Residual strains of 4-inch and 6-inch VB and LEC substrates are shown in Figs. 8 and 9. Residual strains of the VB substrates are less than half of that of the LEC substrates in both 4-inch and 6-inch diameter. Though the residual strains in the LEC substrates show 4-fold symmetry, those in VB substrates do not show 4-fold symmetry.

Profiles of dislocation density and residual strain along the growth axis of 4-inch and 6-inch VB crystals are shown in Fig. 10. Dislocation density and residual strain are low enough from the shoulder to the tail in both 4-inch and 6-inch crystals.

We evaluated the resistance against slip-line generation during MBE process. The wafers are heated at 600~650°C for 30 minutes in a MBE chamber. Figure 11 is the sketch of the slip-line on the wafer observed after MBE growth. Though many slip-lines are generated on the 6-inch LEC wafer, no slip-line is generated



(a) 4" φ (b) 6" φ

Fig. 7. Dislocation densities of (a) 4-inch and (b) 6-inch single crystals grown by VB technique.

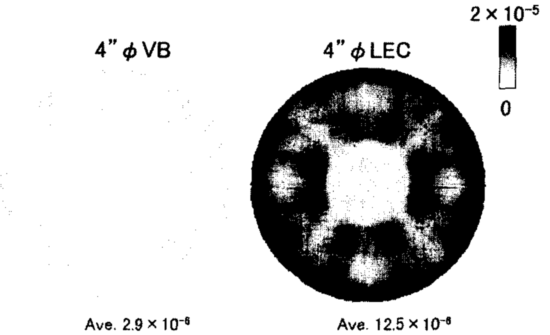


Fig. 8. Residual strains of 4-inch VB and LEC substrates.

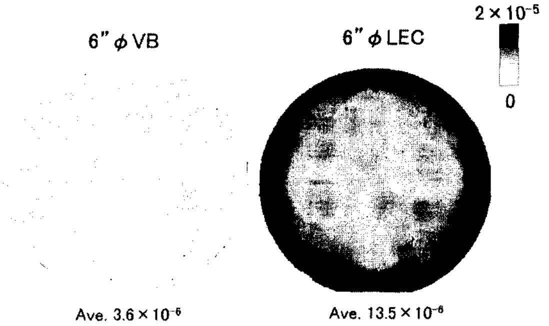


Fig. 9. Residual strains of 6-inch VB and LEC substrates.

on the 6-inch VB wafer. It is thought that slip-lines are generated, when the sum of the residual strain in the substrate and the thermal strain generated during MBE growth becomes larger than the critical resolved shear stress. Therefore, the difference of the slip-line generated during MBE process is attributed to the difference of the residual strain in 6-inch GaAs substrates.

4.2. Electrical properties

Control of resistivity is very important for semi-insulating GaAs substrates, because it affects the performance of electronic devices. Resistivity is dominated by carbon, impurity and EL2 concentrations. The concentration of impurity should be constant in successive growth runs. Therefore, the resistivity is substantially dominated by carbon and EL2 concentrations. Figure 12 shows the relation between carbon concentration and resistivity of VB-GaAs crystals. The control of resistivity in the wide range of 0.5~50×10^7 Ωcm has been achieved by adjusting the carbon concentration. Radial profiles of resistivity, carbon and EL2 concentrations are shown in Fig. 13. Radial profile of resistivity on a 6-inch VB-GaAs substrate is as uniform as that on a 4-inch LEC-GaAs substrate due to uniform radial profile of carbon and EL2 concentrations. EL2 concentration and its profile are adjusted by post-growth annealing. Uniform radial profile of carbon concentration is thought to be due to the flat solid-liquid interface of the VB-GaAs crystal.

Variation of micro-resistivity affects uniformity of device properties, such as the threshold voltage of

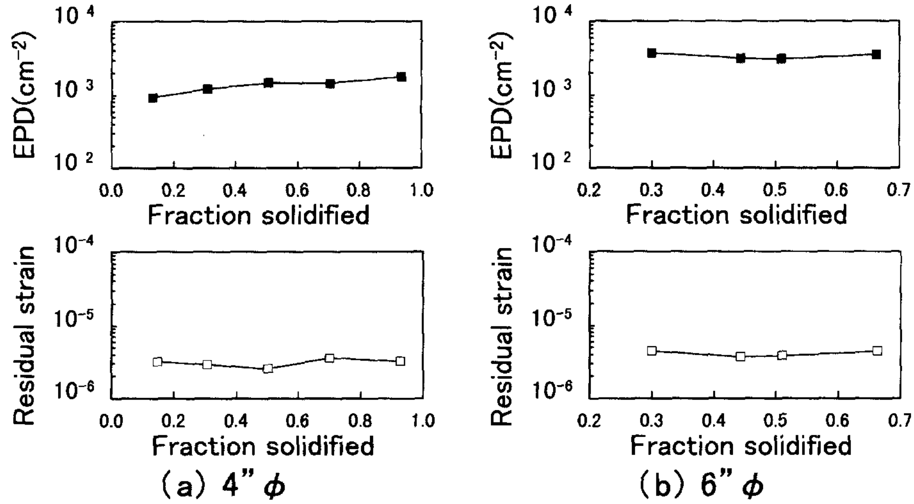


Fig. 10. Profiles of dislocation density and residual strain along the growth axis of (a) 4-inch and (b) 6-inch VB-GaAs crystals.

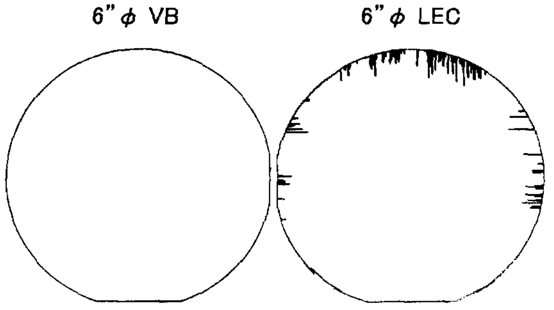


Fig. 11. Sketches of the slip-lines on 6-inch GaAs wafers observed after MBE process.

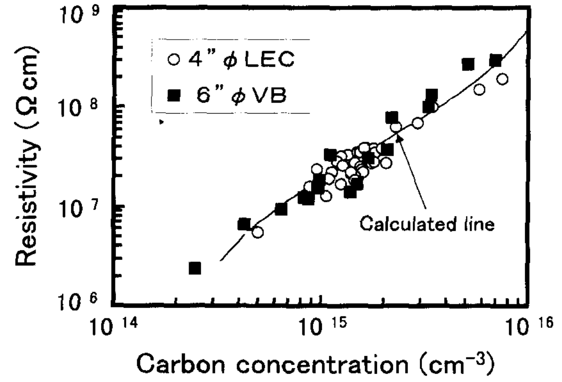


Fig. 12. Carbon concentration and resistivity of GaAs single crystals grown by VB technique.

FET-devices. Therefore, micro-resistivity is one of the most important properties of semi-insulating GaAs substrates. Figure 14 shows the radial profiles of micro-resistivity on 4-inch LEC and 6-inch VB substrates measured at 100 micron-pitches. Normalized standard deviation of the 6-inch VB substrate is less than half of that of the 4-inch LEC substrate. Figure 15 shows two-dimensional maps of micro-resistivity. The micro-photograph shows the distribution of etch pits at the same position of the VB substrate. The distribution of resistivity corresponds to the distribution of etch pit. The value of resistivity is dominated by carbon and EL2 concentrations. Concentration of carbon is not changed around the cell wall. Therefore, variation of micro-resistivity is due to the change of EL2 concentration around the cell wall.

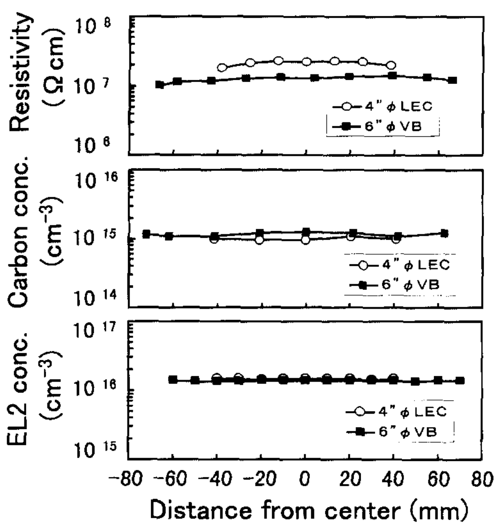


Fig. 13. Radial profiles of resistivity, carbon and EL2 concentrations on 6-inch VB and 4-inch LEC substrates.

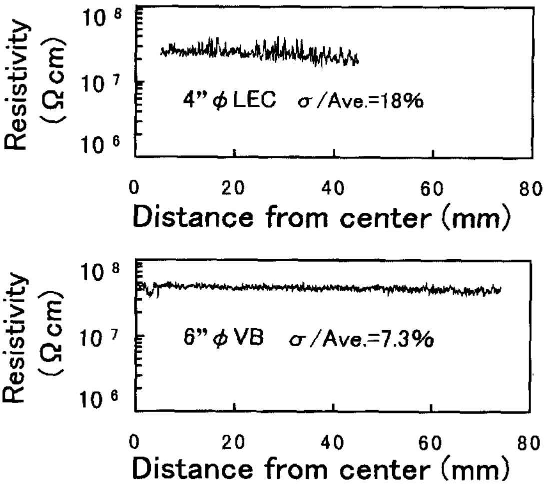


Fig. 14. Radial profiles of micro-resistivity on 6-inch VB and 4-inch LEC substrates measured at 100 micron-pitches.

5. Conclusions

Dislocation-free Si-doped 3-inch GaAs single crystals, and 4-inch to 6-inch large-diameter semi-insulating GaAs single crystals with extremely low dislocation density and low-residual-strain have been developed by VB technique. We applied computer simulation to optimize the growth condition to achieve the flat solid-liquid interface. Re- markable control of resistivity has been achieved by carbon doping. A uniform radial profile of resistivity has been achieved by flattening the solid-liquid interface. Good uniformity of micro-resistivity has been achieved by reducing the dislocation density by VB growth.

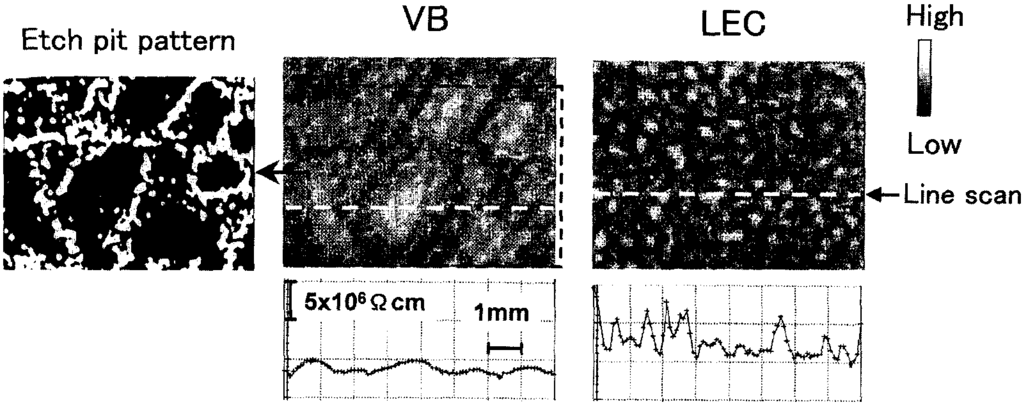


Fig. 15. Two-dimensional maps of micro-resistivity on VB and LEC substrates.

References

[1] T. Kawase, T. Wakamiya, S. Fujiwara, K. Hashio, K. Kimura, M. Tatsumi, T. Shirakawa, K. Tada and M. Yamada, Proc. of Semi-insulating III-V Materials, Ixtapa, Mexico (1992) 85.

[2] Y. Hagi, S. Kawarabayashi, T. Inoue, R. Nakai, J. Kohno, T. Kawase and M. Tatsumi, Proc. of the 9th Conf. on Semiconducting and Insulating Materials, Toulouse, France (1996) 279.

[3] T. Kawase, Y. Hagi, M. Tatsumi, K. Fujita and R. Nakai, Proc. of the 9th Conf. on Semiconducting and Insulating Materials, Toulouse, France (1996) 275.

[4] T. Kawase, H. Yoshida, T. Sakurada, Y. Hagi, K. Kaminaka, H. Miyajima, S. Kawarabayashi, N. Toyoda, M. Kiyama, S. Sawada and R. Nakai, Digest of Papers of 1999 Int. Conf. on GaAs Manufacturing Technology, Vancouver, Canada 125.

[5] A.S. Jordan and E.M. Monberg, J. Appl. Phys. 73 (1993) 4016.

[6] M. Yamada, Rev. Sci. Instrum. 64 (1993) 1815.