〈論文〉 4-5-3

Design Considerations for Auto-Connected Multi-Pulse Rectifiers for High Power AC Motor Drives

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ABSTRACT

Auto-connected multipulse (12/24 pulse) rectifier schemes are cost effective methods for reducing line current harmonics in PWM drive systems. Employing these schemes to enhance utility power quality requires careful attention to several design considerations. In particular, excursion of dc-link voltage at no load, effect of pre-existing voltage distortion, impedance mismatches, unequal diode drops on rectifier current sharing and performance, are fully analyzed. Several corrective measures to improve the performance of 12/24-pulse rectifier systems are also discussed. Finally, experimental results on a 460V, 60Hz, 400kVA commercial ASD, retrofitted with 12/24 pulse rectifier systems are discussed in detail.

Key Words : Multipulse converter, clean power, harmonic reduction, three-phase rectifier.

1. INTRODUCTION

Adjustable speed drives (ASDs) are finding expanding applications in industrial and commercial systems. An ASD controlled process simply results in better efficiency, energy savings, and high performance. Due to the availability of higher voltage and higher current IGBTs, larger VA, ASD applications are increasing at a faster rate. A majority of the commercially available ASDs employs a 6-pulse diode rectifier as an interface to the electric utility. This type of interface results in high harmonic content and poor THD. Reference [1] clearly documents harmonic related problems in a power distribution network due to the proliferation of nonlinear loads. In larger VA, ASD applications, compliance to IEEE 519 and IEC 1000-3 harmonic limits is gaining increased momentum. [2, 3]

Several approaches to reduce line current harmonics in ASD systems are briefly summarized below, along with their merits and demerits:

(a) Add a dc-link inductance (1-5%) and/or ac line chokes (3-5%). With this approach, the input THD can be reduced to.30% (maximum), but the 5th and 7th harmonic levels are still above the limits specified in IEEE 519

(b) Install a 5th and 7th harmonic trap at the input of the ASD.[2, 3] The addition of traps results in a leading power factor, and the potential for resonance conditions is high.[1] Further, the combined VA rating of the traps along with de-coupling ac line reactors to avoid resonance is high.[2, 3]

(c) Replace the diode rectifier with a PWM controlled IGBT rectifier.[10] With this approach, both line current harmonic reduction and regeneration of the ASD load can be achieved. The disadvantages include: higher cost (ASD cost is nearly doubled); increased complexity in control, particularly if optimum performance is desired under pre-existing utility voltage distortions; higher dc-link voltage due to boost operation; outputs twice the common mode

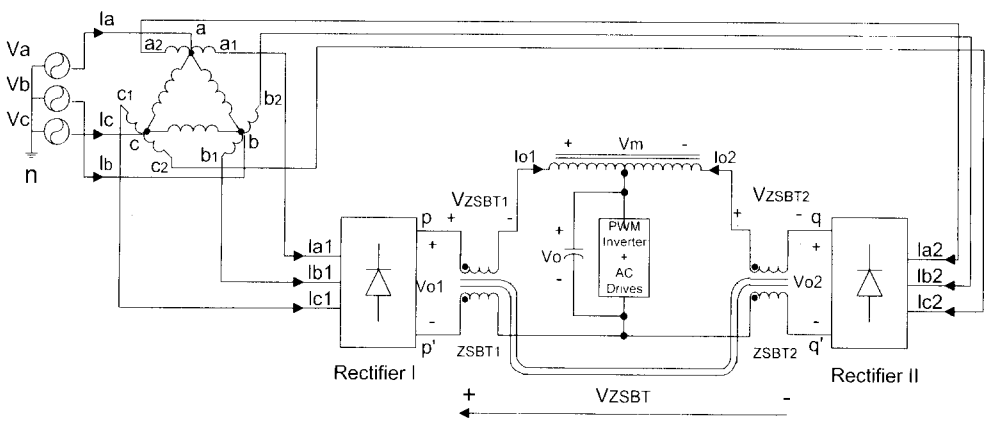


Fig. 1 A new 12-pulse rectifier system with low THD at the input utility supply.

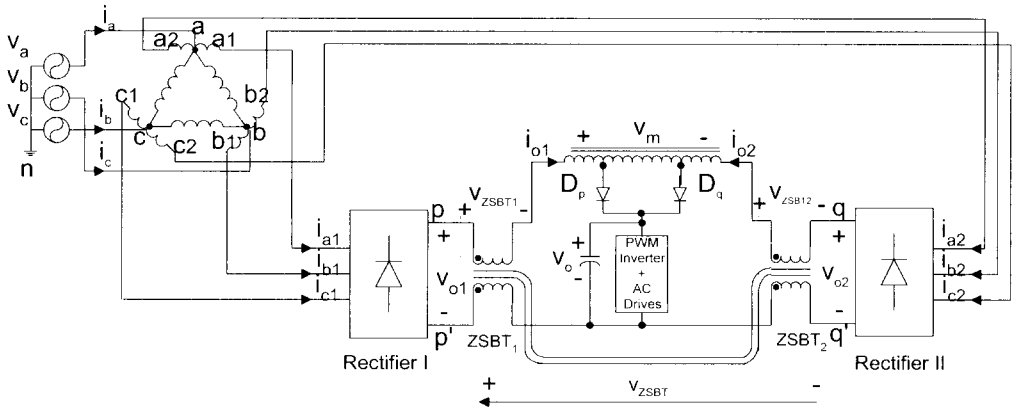


Fig. 2 Proposed auto-connected 24-pulse rectifier system

dv/dt transitions,this can result in accelerated motor bearing degradation and necessitate input/output EMI filters;

(d) Retrofit the ASD with multi-pulse rectifiers.[4-8] These rectifiers are attractive due to their inherent ruggedness and simplicity. Control circuits are not required. In addition, auto-connected multi-pulse rectifiers result in low VA magnetics.[4-8] However, careful attention to several design considerations is necessary to achieve high performance features.

Two high performance low cost/VA auto-connected 12/24 pulse rectifiers were recently introduced [4, 6] and are shown in Fig. 1 and Fig. 2. The autotransformer provides ±15° phase shift to rectifier I and II. Two zero-sequence-blocking transformers (ZSBTs) on a common core are placed symmetrically in series with each rectifier. The ZSBTs offer high impedance to zero sequence currents and thereby ensure independent operation of rectifiers I & II with 120° conduction of diodes. Also symmetrical placement of ZSBTs result in near equal impedance in the two parallel paths formed by rectifiers I & II.

The 12-pulse rectifier system (Fig. 1) can be upgraded to 24-pulse (from the input current standpoint) with the addition of two diodes in the interphase transformer (IPT) and is shown in Fig. 2. The tapped IPT in 24-pulse system (Fig. 2) automatically modulate the rectifier output currents I_{o1} and I_{o2} which results in 24-pulse characteristics in the input current i.e. 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th} harmonics are eliminated. The VA ratings of the magnetics employed in 12/24 pulse rectifier systems are shown in Table 1.[8]

An important design consideration in 12/24-pulse systems shown in Fig. 1 and Fig. 2 is to achieve equal current sharing between rectifiers I & II. In addition, near equal current sharing is mandatory for harmonic cancellation and to achieve low THD levels in the utility line currents. Further, the excursion of no load voltage, effect of unequal diode forward voltage drops, pre-existing voltage distortion on the rectifier performance, need to be considered and is a subject matter of this paper. Several corrective measures are also proposed in this paper to achieve high performance characteristics. Finally, experimental results on a 460V, 60Hz, 400kVA commercial ASDs, retrofitted with 12/24 pulse rectifier systems, are discussed in detail..

Table 1 Ratings of magnetic components for 12/24-pulse rectifier systems

	Polyphase Transformer	ZSBT	IPT
VA ratings for 12-pulse rectifier	0.18 P_o	0.066 P_o	0.02 P_o
VA ratings for 24-pulse rectifier	0.23 P_o	0.075 P_o	0.022 P_o

2. DESIGN CONSIDERATIONS

Fig. 1 and Fig. 2 show the topology of the 12/24 pulse rectifiers. Fig. 3 shows the winding configurations of the magnetic components. In this section, several design considerations are discussed in detail.

2.1 No Load Voltage

In the proposed 12/24-pulse rectifiers (Fig. 1, Fig. 2), the ZSBTs and the interphase transformer (IPT) cannot support harmonic voltage components (which is crucial for independent operation of rectifier I & II) unless an alternating magnetizing current begins to flow in the loop $p^+q^+q^-p^-$ formed by the two parallel rectifier connections. Under normal (load) conditions, I_{o1}, I_{o2} are larger and the flow of alternating magnetizing current for ZSBT/IPT is possible. However, under light load I_{o1}, I_{o2} and I_o are low values and the alternating magnetizing current cannot flow in the loop unless

superimposed on a larger dc-value. Therefore under light load, the dc-link voltage V_o is no longer the average of voltages V_{o1} and V_{o2}.

By examining the vector diagram of the transformer output voltage (Fig. 4) the following can be deduced: under normal (loaded) condition, the voltage sets V_{a1b1}, V_{b1c1}, V_{c1a1}, V_{a2b2}, V_{b2c2}, V_{c2a2} are active. The average dc-link voltage can be shown to be[8]

$$V_{o,dc} = \frac{3}{\pi}\sqrt{2}(1.035)V_{LL} = 1.3975V_{LL} \quad (1)$$

Under light load condition, the ZSBT and IPT are under excited and the voltage sets V_{a2c1}, V_{b1c2}, V_{b2a1}, V_{c1a2}, etc. become dominant. Fig. 5 shows the resultant output voltage under light load. The resultant output voltage under light load can be shown to be [8],

$$V_{o,dc,noload} = \frac{3\sqrt{2}}{\pi}\frac{1.999}{\sqrt{3}}V_{LL} = 1.56V_{LL} \quad (2)$$

Comparing (1) and (2) it can be concluded that the no load voltage can be 11.6% higher than nominal. The rapid decrease in V_o for an increase in I_o from zero to $I_{o,crit}$ is evidenced in Fig. 5 (a) and (b). When $0 < I_o < I_{o,crit}$, the IPT loses control and an over voltage in V_o is experienced.

This over voltage phenomenon coupled with 10% increase in input voltage may cause nuisance tripping of an ASD and also necessitate the design of the dc-link components and the IGBTs to withstand this over voltage situation at no load. This problem can be addressed by keeping $I_{o,crit}$ as low as possible, which in turn implies that the magnetizing current of ZSBT and IPT must be as low as possible. Introducing a small air gap in IPT to avoid saturation under current unbalance is customary and may aggravate the possibility of over voltage. Section 3 discusses additional corrective measures.

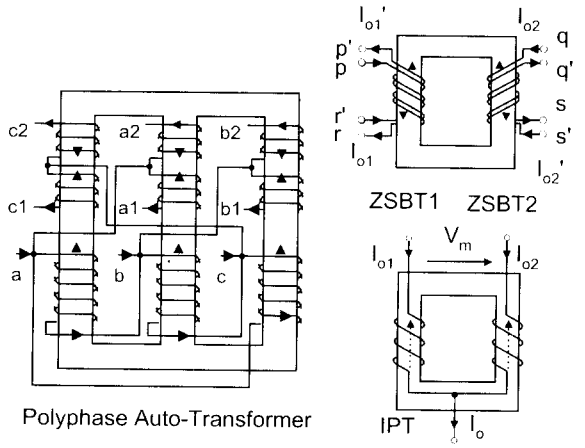


Fig. 3 Winding configurations of transformers

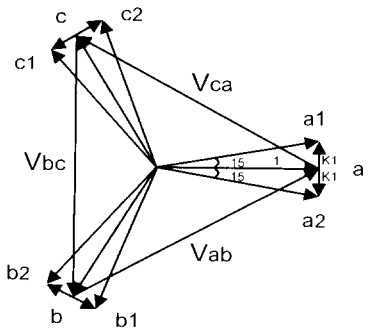


Fig. 4 Vector diagram of the polyphase autotransformer

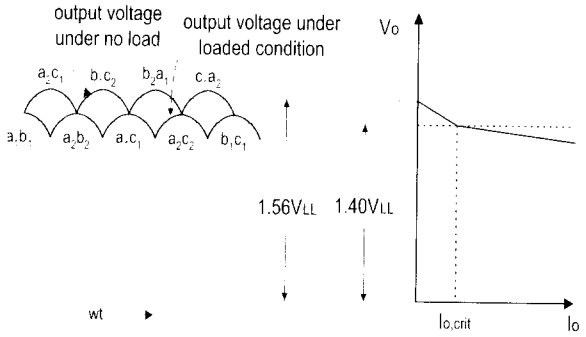


Fig. 5 (a) Output voltage at no load operation

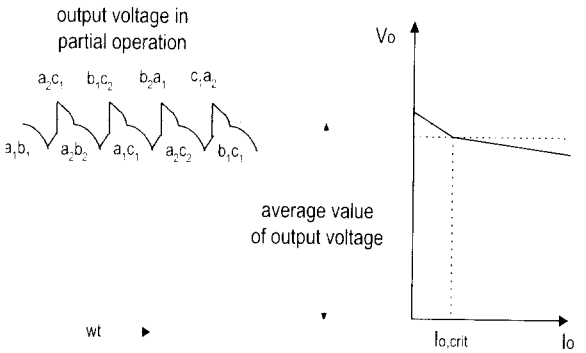


Fig. 5 (b) Output voltage at partial load operation

2.2 Effect Of Unequal Impedance's And Diode Forward Voltage Drops

Fig. 6 (a) shows the dc equivalent circuit of the two rectifier parallel paths along with the load. V_{o1}, V_{o2} represent the dc-output voltages of rectifier I & II respectively. R_{eq1}, R_{eq2} represent the ohmic impedances. $2V_{d1}$, $2V_{d2}$, represent the forward voltage drops of conducting diodes in the two rectifiers I & II. Fig. 6 (b) shows the variation of dc-link voltage V_o as a function of load current. It also demonstrates that I_{o1} and I_{o2} may be unequal if $R_{eq1} \neq R_{eq2}$ and $2V_{d1} \neq 2V_{d2}$.

2.3 Effect Of Pre-Existing Utility Voltage Distortion On Rectifier Performance – Analysis

In many industrial systems with nonlinear loads, it is common to measure 2.5% to 5% pre-existing 5th and 7th harmonic voltage distortion (also termed as background voltage distortion). This can occur when other nonlinear loads such as ASDs and SCR converters are operating in the vicinity. Pre-existing voltage distortion can significantly affect rectifier performance.[9]

From the rectifier topology in Fig. 1 and Fig. 2 it is clear that the pre-existing voltage distortion on the input supply, is processed by the phase-shifting transformer and the rectifier output voltages are altered. This can potentially cause the dc currents I_{o1} and I_{o2} to be unequal.

From vector diagram shown in Fig. 4, the line to neutral voltages are $\bar{V}_a$, $\bar{V}_b$, and $\bar{V}_c$. Further, from Fig. 4,

$$\begin{aligned}\bar{V}_{a1} &= \bar{V}_a - k_1 \bar{V}_{bc}\\ \bar{V}_{b1} &= \bar{V}_b - k_1 \bar{V}_{ca}\\ \bar{V}_{c1} &= \bar{V}_c - k_1 \bar{V}_{ab}\end{aligned} \tag{3}$$

where k_1 is the autotransformer turns ratio. To achieve ±15° phase shift [8],

$$k_1 = 0.268/\sqrt{3} \tag{4}$$

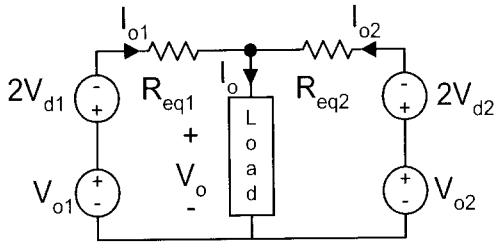


Fig. 6 (a) DC equivalent circuit of parallel rectifier

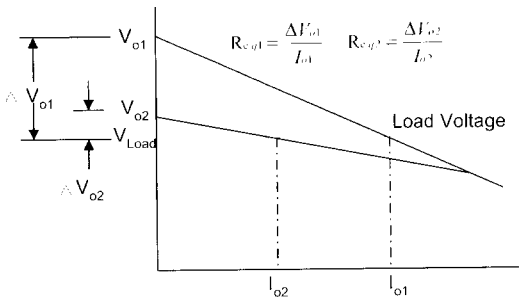


Fig. 6 (b) Voltage regulation diagram

Similarly,

$$\begin{aligned}\bar{V}_{a2} &= \bar{V}_a + k_1 \bar{V}_{bc}\\ \bar{V}_{b2} &= \bar{V}_b + k_1 \bar{V}_{ca}\\ \bar{V}_{c2} &= \bar{V}_c + k_1 \bar{V}_{ab}\end{aligned} \tag{5}$$

Let us now assume that the input utility voltage $\bar{V}_a$, $\bar{V}_b$, and $\bar{V}_c$ contain 5th, 7th harmonic pre-existing voltage distortion.

Let,

$$\begin{aligned}\bar{V}_a &= V_1 \sin(\omega t) + V_5 \sin(5\omega t + \theta_5) + V_7 \sin(7\omega t + \theta_7)\\ \bar{V}_b &= V_1 \sin(\omega t - 120^o) + V_5 \sin(5\omega t + \theta_5 + 120^o)\\ &\quad + V_7 \sin(7\omega t + \theta_7 - 120^o)\\ \bar{V}_c &= V_1 \sin(\omega t + 120^o) + V_5 \sin(5\omega t + \theta_5 - 120^o)\\ &\quad + V_7 \sin(7\omega t + \theta_7 + 120^o)\end{aligned} \tag{6}$$

where V_5, V_7 are magnitudes and θ_5, θ_7 are phase angles of 5th, 7th harmonic voltage distortion, respectively.
Substituting (6) into (3) we have,

$$\begin{aligned}\bar{V}_{a1} &= V_1 \sin(\omega t) - \sqrt{3}k_1 V_1 \sin(\omega t - 90^o) + V_5 \sin(5\omega t + \theta_5)\\ &\quad - \sqrt{3}k_1 V_5 \sin(5\omega t + \theta_5 + 90^o) + V_7 \sin(7\omega t + \theta_7)\\ &\quad - \sqrt{3}k_1 V_7 \sin(7\omega t + \theta_7 - 90^o)\end{aligned} \tag{7}$$

Next, substituting k_1 from (4) into (7) we have,

$$\begin{aligned}\bar{V}_{a1} &= V_1' \sin(\omega t + 15^o) + V_5' \sin(5\omega t + \theta_5 - 15^o)\\ &\quad + V_7' \sin(7\omega t + \theta_7 + 15^o)\end{aligned} \tag{8}$$

where $V_1' = 1.035 V_1$, $V_5' = 1.035 V_5$, $V_7' = 1.035 V_7$. Similarly, V_{b1} and V_{c1} can be found and given by,

$$\begin{aligned}\bar{V}_{b1} &= V_1' \sin(\omega t - 105^o) + V_5' \sin(5\omega t + \theta_5 + 105^o)\\ &\quad + V_7' \sin(7\omega t + \theta_7 - 105^o)\end{aligned} \tag{9}$$

$$\begin{aligned}\bar{V}_{c1} &= V_1' \sin(\omega t + 135^o) + V_5' \sin(5\omega t + \theta_5 - 135^o)\\ &\quad + V_7' \sin(7\omega t + \theta_7 + 135^o)\end{aligned} \tag{10}$$

Now, the rectifier I output voltage V_{o1} (see Fig. 1 and Fig. 2) is given by,[11]

$$V_{o1} = \bar{V}_{a1} SW_1 + \bar{V}_{b1} SW_2 + \bar{V}_{c1} SW_3 \tag{11}$$

where SW_1, SW_2, SW_3 are rectifier switching functions. and the switching functions are given by,

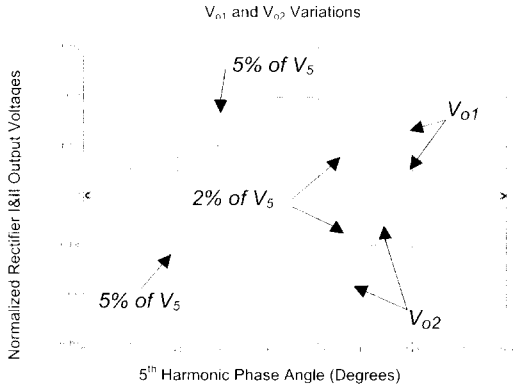


Fig. 7 (a) Variation of rectifier I & II output voltages V_{o1}, V_{o2} as a function of pre-existing 5th harmonic voltage distortion magnitude and phase

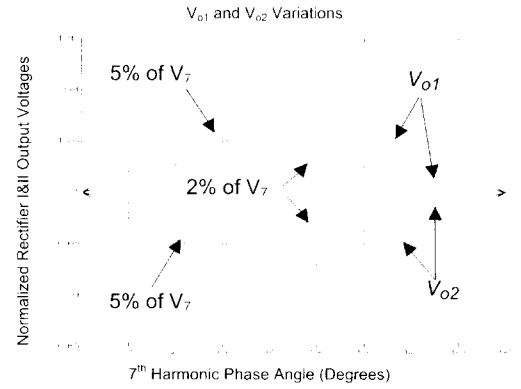


Fig. 7 (b) Variation of rectifier I & II output voltages V_{o1}, V_{o2} as a function of pre-existing 7th harmonic voltage distortion magnitude and phase

$$SW_1 = \sum_{n=odd}^{\infty}\left(\frac{4}{n\pi}\cos\frac{n\pi}{6}\right)\sin n(\omega t + 15^o)$$
$$SW_2 = SW_1(\omega t - 120^o)$$
$$SW_3 = SW_1(\omega t + 120^o) \quad (12)$$

Substituting (8) to (10) into (11) and extracting the dc component from the resulting multiplication yields,

$$V_{o1} = \frac{3\sqrt{3}}{\pi}\left(V_1' - \frac{V_5'}{5}\cos(\theta_5 - 90^o) - \frac{V_7'}{7}\cos(\theta_7 - 90^o)\right) \quad (13)$$

Using the procedure outlined above, the rectifier-II output voltage V_{o2} in the presence of pre-existing voltage distortion in the utility voltage can be shown to be,

$$V_{o2} = \frac{3\sqrt{3}}{\pi}\left(V_1' - \frac{V_5'}{5}\cos(\theta_5 + 90^o) - \frac{V_7'}{7}\cos(\theta_7 + 90^o)\right) \quad (14)$$

We can see from (13) and (14) that the dc output voltage of each rectifier is not only a function of the magnitude of the pre-existing voltage distortion, but also the phase angle θ_5 and θ_7. As θ_5 and θ_7 increase, the dc output voltage, V_{o1}, of rectifier I increases, whereas, the dc output voltage, V_{o2} of rectifier II decreases. As shown in Fig. 7, as θ_5 and θ_7 approach 90°, the difference between V_{o1} and V_{o2} increases resulting in larger voltage unbalance at the rectifier output. As a consequence, the rectifier output currents I_{o1}, I_{o2} can be significantly unbalanced, thus deteriorating the performance. This is demonstrated in the calculation example in the next section.

2.4 Calculation Example

The following example gives a numerical description of the effect of unequal impedance, forward diode drop voltage, and 5% pre-existing 5th and 7th harmonic voltage distortion in the input utility voltage to the unbalance current sharing problem.

Consider the dc-equivalent circuit of the 12/24-pulse rectifier systems shown in Fig. 6(a). Let the nominal line to line rms voltage (V_{LL}) of the three-phase utility supply be 460V. Let us also assume 5% of 5th and 7th harmonic voltage distortions on the utility supply. The output voltages, V_{o1} and V_{o2} can be calculated using (13), (14), and Fig. 7. Assuming $\theta_5 = \theta_7 = 90^o$ for worst case, we have

$$V_{o1} = 1.398V_{LL,RMS}(1 + .01 + .00714) = 654.1V \quad (15)$$

$$V_{o2} = 1.398V_{LL,RMS}(1 - .01 - .00714) = 632.01V \quad (16)$$

Let us assume the diode forward voltage drops $V_{d1} = V_{d2} = 1V$ and $R_{eq1} = R_{eq2} = 0.2\Omega$ and $R_{load} = 1\Omega$ (for 400 kW). Then, the output voltage V_o can be found by (17),

$$V_o = \frac{(V_{o1} - 2V_{d1})R_{eq2}R_{load} + (V_{o2} - 2V_{d2})R_{eq1}R_{load}}{R_{eq1}R_{load} + R_{eq2}R_{load} + R_{eq1}R_{eq2}} = 582.77V \quad (17)$$

Then, the output currents I_{o1} and I_{o2} can be calculated and are shown to be,

$$I_{o1} = \frac{V_{o1} - 2V_{d1} - V_o}{R_{eq1}} = 346.65\ \text{A} \quad (18)$$

$$I_{o2} = \frac{V_{o2} - 2V_{d2} - V_o}{R_{eq2}} = 236.2\ \text{A} \quad (19)$$

$$I_o = I_{o1} + I_{o2} = 582.85\ \text{A} \quad (20)$$

Now, defining percentage unbalance in the current as,

$$\%Current\ Unbalance = \frac{\left|\frac{I_o}{2} - I_{o1}\right|}{\frac{I_o}{2}} x100\% = 18.95\% \qquad (21)$$

From (18) to (21) it is clear that significant current unbalance can result due to pre-existing utility voltage distortion. The above example can be recomputed to evaluate the mismatches in diode forward voltage drop and ohmic impedances. These mismatches may further aggravates the current unbalance situation.

3. PROPOSED CORRECTIVE MEASURES

In this section, several corrective measures to improve the 12/24-pulse rectifier performance are explored. Since the proposed systems are auto-connected for low cost/VA, they must operate in parallel. The previous sections have demonstrated that current sharing is an important aspect that must be addressed.

3.1 Magnetic Components – Design Considerations

For the 12/24 pulse rectifier systems to operate properly, design of magnetic components (auto-transformer, ZSBT & IPT) to exhibit near equal leakage reactance's and ohmic impedance in both of the rectifier parallel paths is vital for current sharing. The magnetic components for the 12/24 pulse rectifier systems must be designed for balanced winding resistance and leakage inductance. Since the components are rich in harmonic components, high-frequency winding technique must be deployed. The optimum design for the autotransformer consists of winding the secondary arms as bifilar or sectioned side by side. To reduce proximity effects and losses, the primary winding should be split with the secondary arms and sandwiched in the center. The ZSBT is primarily sensitive to winding resistance as explained in section 2.2. The dc resistance between two bridges, on both the positive and negative side, should be balanced. The winding sets should be bifilar or sectioned side by side. Since all windings are wound on a common core, the resulting dc component cancels. This allows the ZSBT to be designed for high magnetizing inductance minimizing undesirable, third order harmonic currents. The IPT must be wound using similar methods as the ZSBT. The difference here is that the dc component is non-zero and the magnetic component must support the sixth order harmonic component. The maximum dc offset current must be determined to define the core gap.

3.2 Other Considerations

Current sharing ability can be enhanced by using matched pair of diodes in the rectifier I & II. This however, may not be always possible or preferred in commercial applications. Further, it is imperative that one keep the lead lengths of cables be the same between connections in both the parallel paths. This can help equalize the ohmic impedance. To address the voltage excursion under light load, it s necessary to keep $I_{o,crit}$ as small as possible. This can be achieved by keeping the air-gap in the IPT to be zero or equal to a small value.

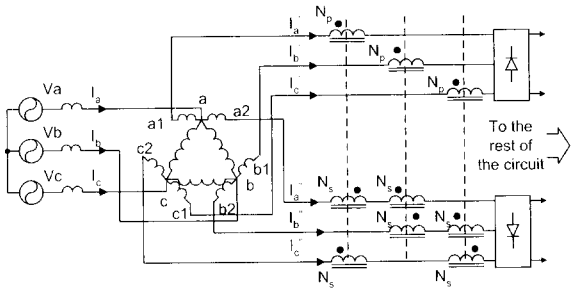


Fig. 8 Application of HBRs in a 12-pulse rectifier system

3.3 Use Of Harmonic Blocking Reactors (HBRs)

If one follows the corrective measures suggested in sections 3.1 & 3.2 and achieve equal impedance in both of the rectifier parallel paths, significant current unbalance can still occur due to the pre-existing voltage distortion. Section 2.3 and the example in section 2.4 demonstrate that pre-existing 5th and 7th harmonic voltage distortion on the electric utility can cause the two rectifier output voltages V_{o1} and V_{o2} to shift in opposite directions (Fig. 7). Small changes in the dc values in V_{o1} and V_{o2} can alter the rectifier I & II current sharing significantly. To counter this effect harmonic-blocking reactors (HBRs) can be employed.[7, 9] Reference [9] details the application and design of HBRs and the connection diagram is shown in Fig. 8.

HBRs are essentially coupled reactors which offer high impedance to 5th, 7th harmonic current components and near zero impedance to fundamental current components. Also HBRs (due to coupling) ensure rectifier I input current to be dependent on rectifier II and vice versa. This action contributes to balanced operation of rectifier I & II.[9]

3.4 Use Of SCRs In 24-Pulse Rectifier Systems

The previous section (3.3) suggested the use of HBRs to balance the rectifier output currents; however, HBRs constitute an additional magnetic component, which could add to weight and complexity of the system. A simple alternative for 24-pulse systems is suggested in the following manner:

Replace the two diodes connected to IPT with two SCRs (Fig. 9). By controlling the firing angle of the SCRs in closed loop, the average rectifier output currents $I_{o1,av}$ and $I_{o2,av}$, can be made equal and current balance can be achieved. In addition to improved current balance with SCR control, the IPT saturation can be avoided. Thus, the IPT design can be further optimized with minimal or no air gap. Thus the modified 24-

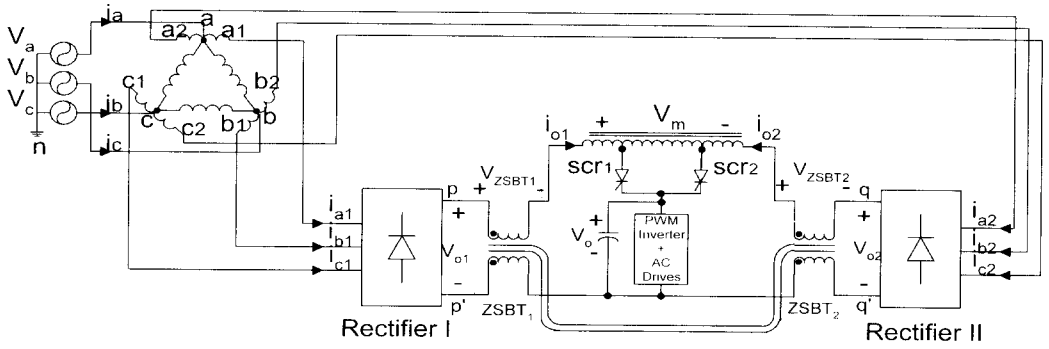


Fig. 9 Proposed 24 -pulse topology with SCR control

pulse scheme with two SCRs (Fig. 9) is a high performance rectifier scheme.

4. EXPERIMENTAL RESULTS

In this section experimental results on a 460V, 60Hz, 400kVA, ASD retrofitted with 12/24-pulse rectifier system are discussed. Two industrial proto-types of the 12/24-pulse systems were constructed with the assistance of an industrial sponsor. Tests were conducted on industrial setting powering an ASD load. The output load was varied from 3% to 90% and the results are tabulated in Tables 2 and 3. Fig. 10(a) to Fig. 10(h) show some of the captured waveforms. In the 12-pulse version, the THD of the input current varied from 53% to 8.31% for an output load variation 3% to 90%. The current unbalance is minimal (4.81%) at 90% load and worst (17.2%) at 20% load. It is also clear from Table 2 that the rectifier output voltage V_{o1} and V_{o2} vary with load condition. Also it was noticed that V_{o1} and V_{o2} were lower at 3% load compared to 20% load (Table 2), this was attributed to somewhat low input line condition at the time when the test was conducted.

Fig. 11(a) to Fig. 11(h) and Table 3 show the results from the 24-pulse configuration (Fig. 2). The ASD load was again varied from 3% to 80%. The resultant input current THD of the 24-pulse system is superior compared to the 12-pulse. Also, there seems to be some improvement in the current sharing ability in 24-pulse configuration. Further, the output voltage V_o at light load (3%) in 12/24-pulse systems did not increase as $I_{o,3\%}>I_{o,crit}$. Overall, the 24-pulse system exhibited superior performance for >50% load from the utility interface point of view.

5. CONCLUSION

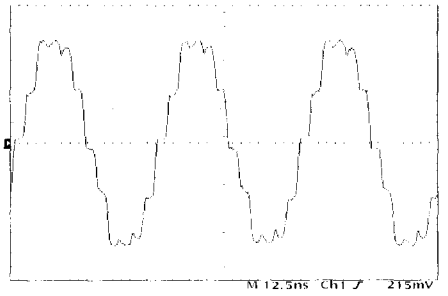
In this paper, deign considerations for 12/24-pulse rectifier systems have been presented. It was shown that design mismatches in impedance, diode drops and pre-existing voltage distortion could significantly affect the performance. Several corrective measures have been proposed to address these issues. Finally, experimental results on a 460V, 400kVA, ASD retrofitted with 12/24-pulse rectifier systems have been presented to demonstrate the feasibility of the proposed schemes to reduce harmonics generated by large VA, ASDs.

Table 2 Measured values from a retrofitted 460V, 400kVA ASD retrofitted with a 12-pulse rectifier system

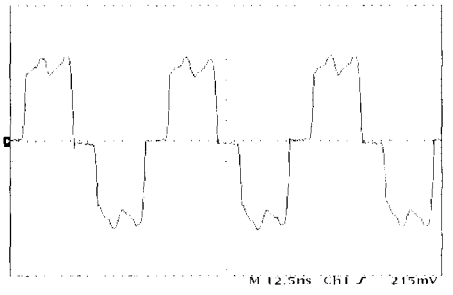
% of Full Load	3%	20%	50%	90%
I_a	28.56A	93.40A	216.0A	378.8A
I_{o1}	11.60A	39.00A	90.70A	171.1A
I_{o2}	15.58A	55.20A	117.1A	188.4A
I_o (I_{o1}+I_{o2})	27.18A	94.20A	207.8A	359.5A
Current Unbalance	14.64%	17.20%	12.70%	4.81%
THD in I_a	53%	18.72%	11.27%	8.31%
V_{o1} (rms)	635.6V	637.2V	629.6V	627.6V
V_{o2} (rms)	638.8V	638.4V	633.6V	626.8V
V_o (rms)	634.0V	636.4V	632.0V	626.8V

Table 3 Measured values from a retrofitted 460V, 400kVA ASD retrofitted with a 24-pulse rectifier system

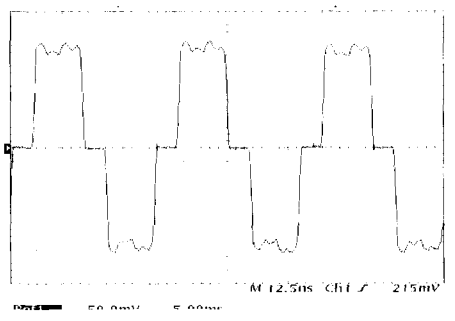
% of Full Load	3%	20%	50%	80%
I_a	30.36A	95.90A	216.8A	339.6A
I_{o1}	10.12A	41.50A	105.0A	177.0A
I_{o2}	8.420A	59.00A	126.6A	186.8A
I_o (I_{o1}+I_{o2})	18.54A	100.5A	232.6A	363.8A
Current Unbalance	9.17%	17.41%	9.72%	2.69%
THD in I_a	52.77%	15.37%	7.36%	5.2%
V_{o1} (rms)	639.2V	635.6V	633.2V	632.2V
V_{o2} (rms)	641.2V	634.8V	630.8V	632.8V
V_o (rms)	649.2V	634.6V	637.6V	642.4V



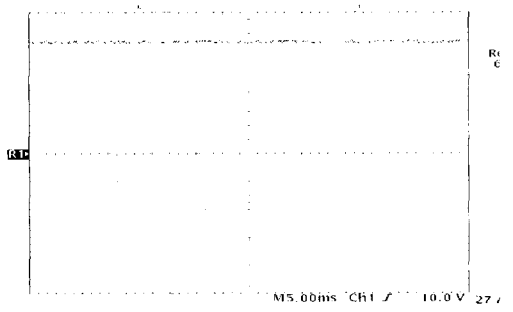
(a) Utility input current, I_a at 50% full load, THD=11.3%, (100A/div).



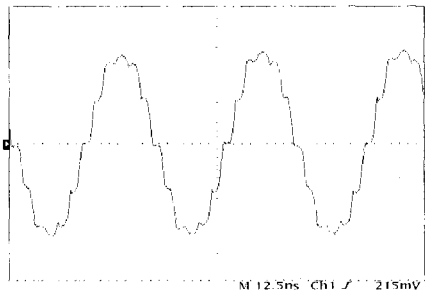
(b) Rectifier I input current, I_{a1} at 50% full load. (100A/div)



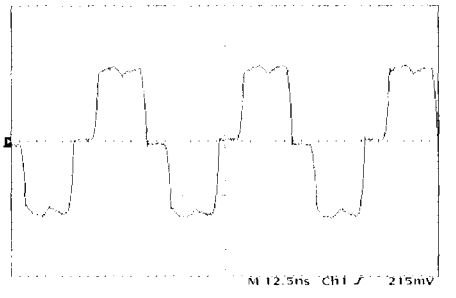
(c) Rectifier II input current, I_{a2} at 50% full load. (100A/div)



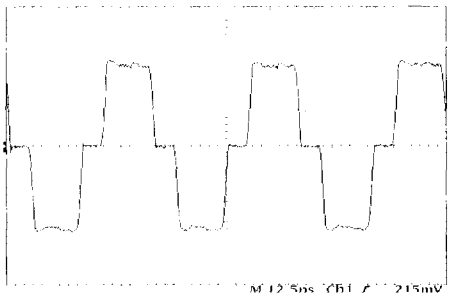
(d) Output voltage, V_o, at 50% full load (200V/div)



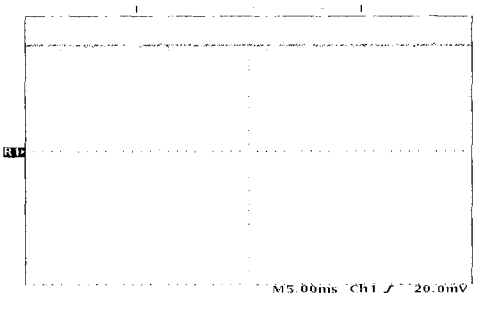
(e) Utility input current, I_a at 90% full load, THD=8.3%, (200A/div).



(f) Rectifier I input current, I_{a1} at 90% full load. (200A/div)

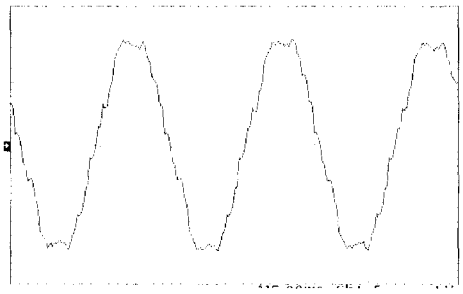


(g) Rectifier II input current, I_{a2} at 90% full load. (200A/div).

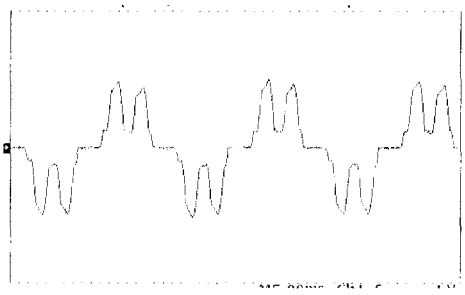


(h) Output voltage, V_o, at 90% full load (200V/div)

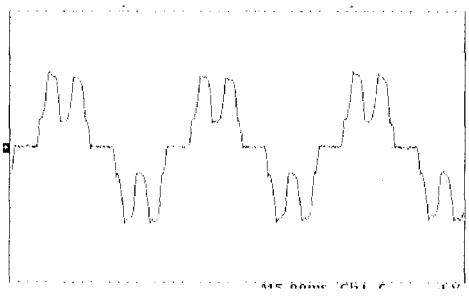
Fig. 10 Experimental Results from a 460V, 400kVA ASD retrofitted with a 12-Pulse Rectifier system



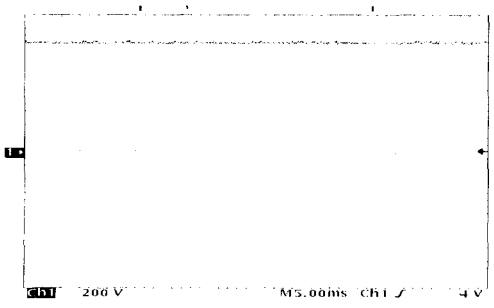
(a) Utility input current, I_a at 50% full load, THD=7.3%, (100A/div).



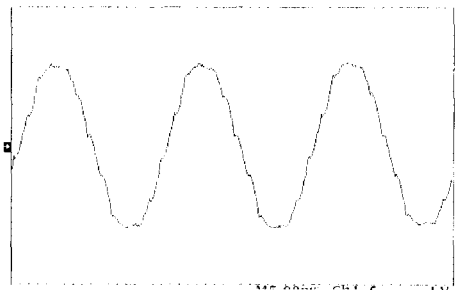
(b) Rectifier I input current I_{a1}, at 50% full load (100A/div)



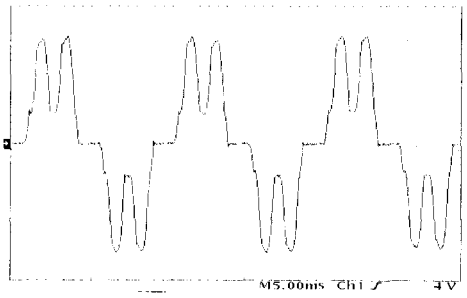
(c) Rectifier II input current I_{a2}, at 50% full load (100A/div)



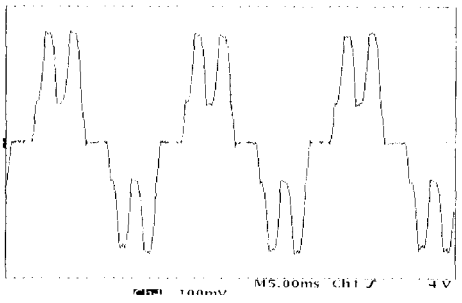
(d) Output voltage, V_o, at 50% full load (200V/div)



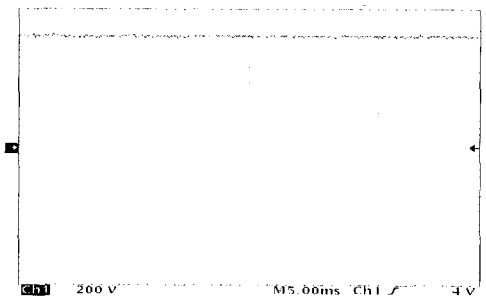
(e) Utility input current, I_a at 80% full load, THD=5.2%, (200A/div).



(f) Rectifier I input current I_{a1}, at 80% full load (100A/div)



(g) Rectifier II input current I_{a2}, at 80% full load (100A/div)



(h) Output voltage, V_o, at 80% full load (200V/div)

Fig. 11 Experimental Results from a 460V, 400kVA ASD retrofitted with a 24-Pulse Rectifier system

Financial support from TAMU Energy Resource Program is acknowledged.

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